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#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	eZ8
Core Size	8-Bit
Speed	5MHz
Connectivity	IrDA, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	6
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/zilog/z8f0813sb005sg

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Flash Code Protection Against Accidental Program and Erasure	. 137
Byte Programming	. 139
Page Erase	. 139
Mass Erase	. 139
Flash Controller Bypass	. 140
Flash Controller Behavior in DEBUG Mode	. 140
Flash Control Register Definitions	. 141
Flash Control Register	. 141
Flash Status Register	. 142
Flash Page Select Register	. 142
Flash Sector Protect Register	. 144
Flash Frequency High and Low Byte Registers	. 144
Flash Option Bits	. 146
Operation	. 146
Option Bit Configuration By Reset	146
Option Bit Types	147
Reading the Flash Information Page	148
Flash Option Bit Control Register Definitions	148
Trim Bit Address Register	148
Trim Bit Data Register	149
Flash Ontion Bit Address Space	149
Trim Bit Address Space	151
Zilog Calibration Data	152
ADC Calibration Data	153
Serialization Data	154
Randomized Lot Identifier	154
	1.5.6
Analite stars	150
Architecture	150
	157
	. 157
	. 158
OCD Data Format	. 159
OCD Autobaud Detector/Generator	. 159
OCD Serial Errors	. 160
OCD Unlock Sequence (8-Pin Devices Only)	. 161
Breakpoints	. 161
Runtime Counter	. 161
On-Chip Debugger Commands	. 162
On-Chip Debugger Control Register Definitions	166

OCD Control Register ...... 166



# List of Tables

Table 1.	F0823 Series Family Part Selection Guide 2
Table 2.	F0823 Series Package Options7
Table 3.	Signal Descriptions
Table 4.	Pin Characteristics (20- and 28-pin Devices)* 11
Table 5.	Pin Characteristics (8-Pin Devices) 12
Table 6.	Z8 Encore! XP F0823 Series Program Memory Maps 14
Table 7.	F0823 Series Flash Memory Information Area Map 15
Table 8.	Register File Address Map 16
Table 9.	Reset and Stop Mode Recovery Characteristics and Latency 21
Table 10.	Reset Sources and Resulting Reset Type
Table 11.	Stop Mode Recovery Sources and Resulting Action 27
Table 12.	Reset Status Register (RSTSTAT)
Table 13.	POR Indicator Values
Table 14.	Power Control Register 0 (PWRCTL0) 32
Table 15.	Port Availability by Device and Package Type
Table 16.	Port Alternate Function Mapping (8-Pin Parts)
Table 17.	Port Alternate Function Mapping (Non 8-Pin Parts)
Table 18.	GPIO Port Registers and Subregisters
Table 19.	Port A–C GPIO Address Registers (PxADDR) 41
Table 20.	PADDR[7:0] Subregister Functions
Table 21.	Port A–C Control Registers (PxCTL) 42
Table 22.	Port A–C Data Direction Subregisters (PxDD) 43
Table 23.	Port A–C Alternate Function Subregisters (PxAF) 44
Table 24.	Port A–C Output Control Subregisters (PxOC) 44
Table 25.	Port A–C High Drive Enable Subregisters (PHDEx) 45
Table 26.	Port A-C Stop Mode Recovery Source Enable Subregisters (PSMREx) 46
Table 27.	Port A–C Pull-Up Enable Subregisters (PPUEx)
Table 28.	Port A–C Alternate Function Set 1 Subregisters (PAFS1x) 48
Table 29.	Port A–C Alternate Function Set 2 Subregisters (PxAFS2) 49
Table 30.	Port A–C Input Data Registers (PxIN) 50
Table 31.	Port A–C Output Data Register (PxOUT) 51
Table 32.	LED Drive Enable (LEDEN) 51
Table 33.	LED Drive Level High Register (LEDLVLH)

#### ilog<sup>°</sup> Embedded in Life 10 An∎IXYS Company

Signal Mnemonic	I/O	Description
COUT	0	Comparator Output. This is the output of the comparator.
Analog		
ANA[7:0]	I	Analog port. These signals are used as inputs to the ADC. The ANA0, ANA1, and ANA2 pins can also access the inputs and output of the integrated transimpedance amplifier.
VREF	I/O	Analog-to-Digital Converter reference voltage input.
Clock Input		
CLKIN	Ι	Clock Input Signal. This pin can be used to input a TTL-level signal to be used as the system clock.
LED Drivers		
LED	0	Direct LED drive capability. All port C pins have the capability to drive an LED without any other external components. These pins have programmable drive strengths set by the GPIO block.
On-Chip Debugger		
DBG	I/O	Debug. This signal is the control and data input and output to and from the OCD. <b>Caution:</b> The DBG pin is open-drain and requires an external pull-up resistor to ensure proper operation.
Reset		
RESET	I/O	RESET. Generates a reset when asserted (driven Low). Also serves as a reset indicator; the Z8 Encore! XP forces this pin Low when in reset. This pin is open-drain and features an enabled internal pull-up resistor.
Power Supply		
V <sub>DD</sub>	I	Digital Power Supply.
AV <sub>DD</sub> <sup>2</sup>	I	Analog Power Supply.
V <sub>SS</sub>	I	Digital Ground.
AV <sub>SS</sub>	I	Analog Ground.
Notes: 1. PB6 and PB7 are	only ava	ailable in 28-pin packages without ADC. In 28-pin packages with ADC, they are

#### Table 3. Signal Descriptions (Continued)

replaced by AV<sub>DD</sub> and AV<sub>SS</sub>.
The AV<sub>DD</sub> and AV<sub>SS</sub> signals are available only in 28-pin packages with ADC. They are replaced by PB6 and PB7 on 28-pin packages without ADC.

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Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 8-pin devices.

Symbol Mnemonic	Direction	Reset Direction	Active Low or Active High	Tristate Output	Internal Pull-up or Pull- down	Schmitt- Trigger Input	Open Drain Output	5V Tolerance
PA0/DBG	I/O	I (but can change during reset if key sequence detected)	N/A	Yes	Program- mable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
PA1	I/O	Ι	N/A	Yes	Program- mable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
RESET/PA2	I/O	I/O (defaults <u>to</u> RESET)	N/A	Yes	Program- mable for PA2; always on for RESET	Yes	Programma- ble for PA2; alw <u>ays on</u> for RESET	Yes, unless pull-ups enabled
PA[5:3]	I/O	I	N/A	Yes	Program- mable Pull-up	Yes	Yes, Programmable	Yes, unless pull-ups enabled
VDD	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
VSS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

#### Table 5. Pin Characteristics (8-Pin Devices)

# Embedded in Life

23

# **Reset Sources**

Table 10 lists the possible sources of a System Reset.

	Table To. Reset Sources an	a Resulting Reset Type		
Operating Mode	Reset Source	Special Conditions		
NORMAL or HALT modes	Power-On Reset/Voltage Brown- Out.	Reset delay begins after supply voltage exceeds POR level.		
	Watchdog Timer time-out when configured for Reset.	None.		
	RESET pin assertion.	All reset pulses less than three system clocks in width are ignored.		
	OCD initiated Reset (OCDCTL[0] set to 1).	System Reset, except the OCD is unaffected by the reset.		
STOP Mode	Power-On Reset/Voltage Brown- Out.	Reset delay begins after supply voltage exceeds POR level.		
	RESET pin assertion.	All reset pulses less than the specified analog delay are ignored. See the <u>Electrical Characteris-</u> tics chapter on page 196.		
	DBG pin driven Low.	None.		

#### Table 10. Reset Sources and Resulting Reset Type

#### **Power-On Reset**

Each device in the Z8 Encore! XP F0823 Series contains an internal POR circuit. The POR circuit monitors the supply voltage and holds the device in the Reset state until the supply voltage reaches a safe operating level. After the supply voltage exceeds the POR voltage threshold ( $V_{POR}$ ), the device is held in the Reset state until the POR Counter has timed out. If the crystal oscillator is enabled by the option bits, this time-out is longer.

After the Z8 Encore! XP F0823 Series device exits the POR state, the eZ8 CPU fetches the Reset vector. Following the POR, the POR status bit in Watchdog Timer Control (WDTCTL) Register is set to 1.

Figure 5 displays POR operation. For the POR threshold voltage ( $V_{POR}$ ), see the <u>Electrical Characteristics</u> chapter on page 196.



Figure 6. Voltage Brown-Out Reset Operation

The POR level is greater than the VBO level by the specified hysteresis value. This ensures that the device undergoes a POR after recovering from a VBO condition.

# Watchdog Timer Reset

If the device is in NORMAL or STOP Mode, the Watchdog Timer can initiate a System Reset at time-out if the WDT\_RES Flash Option Bit is programmed to 1. This is the unprogrammed state of the WDT\_RES Flash Option Bit. If the bit is programmed to 0, it configures the Watchdog Timer to cause an interrupt, not a System Reset, at time-out.

The WDT status bit in the WDT Control Register is set to signify that the reset was initiated by the Watchdog Timer.

### **External Reset Input**

The  $\overline{\text{RESET}}$  pin has a Schmitt-Triggered input and an internal pull-up resistor. Once the  $\overline{\text{RESET}}$  pin is asserted for a minimum of four system clock cycles, the device progresses through the System Reset sequence. Because of the possible asynchronicity of the system

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# HALT Mode

Executing the eZ8 CPU's HALT instruction places the device into HALT Mode, which powers down the CPU but leaves all other peripherals active. In HALT Mode, the operating characteristics are:

- Primary oscillator is enabled and continues to operate
- System clock is enabled and continues to operate
- eZ8 CPU is stopped
- Program counter stops incrementing
- Watchdog Timer's internal RC oscillator continues to operate
- If enabled, the Watchdog Timer continues to operate
- All other on-chip peripherals continue to operate

The eZ8 CPU can be brought out of HALT Mode by any of the following operations:

- Interrupt
- Watchdog Timer time-out (interrupt or reset)
- Power-On Reset
- Voltage Brown-Out reset
- External **RESET** pin assertion

To minimize current in HALT Mode, all GPIO pins that are configured as inputs must be driven to one of the supply rails ( $V_{CC}$  or GND).

# **Peripheral-Level Power Control**

In addition to the STOP and HALT modes, it is possible to disable each peripheral on each of the Z8 Encore! XP F0823 Series devices. Disabling a given peripheral minimizes its power consumption.

# **Power Control Register Definitions**

The following sections describe the power control registers.

#### **Power Control Register 0**

Each bit of the following registers disables a peripheral block, either by gating its system clock input or by removing power from the block.

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40

PC[2:0]. All other signal pins are 5V-tolerant, and can safely handle inputs higher than  $V_{DD}$  even with the pull-ups enabled.

# **External Clock Setup**

For systems using an external TTL drive, PB3 is the clock source for 20- and 28-pin devices. In this case, configure PB3 for alternate function CLKIN. Write the Oscillator Control Register (see the <u>Oscillator Control Register Definitions</u> section on page 171) such that the external oscillator is selected as the system clock. For 8-pin devices, use PA1 instead of PB3.

# **GPIO Interrupts**

Many of the GPIO port pins are used as interrupt sources. Some port pins are configured to generate an interrupt request on either the rising edge or falling edge of the pin input signal. Other port pin interrupt sources generate an interrupt when any edge occurs (both rising and falling). For more information about interrupts using the GPIO pins, see the <u>Interrupt Controller</u> chapter on page 54.

# **GPIO Control Register Definitions**

Four registers for each port provide access to GPIO control, input data, and output data. Table 18 lists these port registers. Use the Port A–D Address and Control registers together to provide access to subregisters for port configuration and control.

Port Register	
Mnemonic	Port Register Name
P <i>x</i> ADDR	Port A–C Address Register (Selects subregisters).
P <i>x</i> CTL	Port A–C Control Register (Provides access to subregisters).
PxIN	Port A–C Input Data Register.
P <i>x</i> OUT	Port A–C Output Data Register.
Port Subregister	
Mnemonic	Port Register Name
P <i>x</i> DD	Data Direction.
P <i>x</i> AF	Alternate Function.
P <i>x</i> OC	Output Control (Open-Drain).

Table 18. GPIO Port Registers and Subregisters

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73

enabled, the Timer Output pin changes state (from Low to High or from High to Low) at timer reload.

Observe the following steps to configure a timer for COUNTER Mode and initiating the count:

- 1. Write to the Timer Control Register to:
  - Disable the timer.
  - Configure the timer for COUNTER Mode.
  - Select either the rising edge or falling edge of the Timer Input signal for the count. This selection also sets the initial logic level (High or Low) for the Timer Output alternate function. However, the Timer Output function is not required to be enabled.
- 2. Write to the Timer High and Low Byte registers to set the starting count value. This only affects the first pass in COUNTER Mode. After the first timer reload in COUNTER Mode, counting always begins at the reset value of 0001H. In COUNTER Mode the Timer High and Low Byte registers must be written with the value 0001H.
- 3. Write to the Timer Reload High and Low Byte registers to set the reload value.
- 4. If appropriate, enable the timer interrupt and set the timer interrupt priority by writing to the relevant interrupt registers.
- 5. Configure the associated GPIO port pin for the Timer Input alternate function.
- 6. If using the Timer Output function, configure the associated GPIO port pin for the Timer Output alternate function.
- 7. Write to the Timer Control Register to enable the timer.

In COUNTER Mode, the number of timer input transitions since the timer start is computed via the following equation:

COUNTER Mode Timer Input Transitions = Current Count Value – Start Value

#### **COMPARATOR COUNTER Mode**

In COMPARATOR COUNTER Mode, the timer counts input transitions from the analog comparator output. The TPOL bit in the Timer Control Register selects whether the count occurs on the rising edge or the falling edge of the comparator output signal. In COMPAR-ATOR COUNTER Mode, the prescaler is disabled.



 $PWM Period (s) = \frac{Reload Value \times Prescale}{System Clock Frequency (Hz)}$ 

If an initial starting value other than 0001H is loaded into the Timer High and Low Byte registers, use the ONE-SHOT Mode equation to determine the first PWM time-out period. If TPOL is set to 0, the ratio of the PWM output High time to the total period is represented by the following equation:

PWM Output High Time Ratio (%) =  $\frac{\text{Reload Value} - \text{PWM Value}}{\text{Reload Value}} \times 100$ 

If TPOL is set to 1, the ratio of the PWM output High time to the total period is represented by the following equation:

PWM Output High Time Ratio (%) =  $\frac{PWM Value}{Reload Value} \times 100$ 

#### **PWM Dual Output Mode**

In PWM DUAL OUTPUT Mode, the timer outputs a PWM output signal pair (basic PWM signal and its complement) through two GPIO port pins. The timer input is the system clock. The timer first counts up to the 16-bit PWM match value stored in the Timer PWM High and Low Byte registers. When the timer count value matches the PWM value, the Timer Output toggles. The timer continues counting until it reaches the reload value stored in the Timer Reload High and Low Byte registers. Upon reaching the reload value, the timer generates an interrupt, the count value in the Timer High and Low Byte registers is reset to 0001H and counting resumes.

If the TPOL bit in the Timer Control Register is set to 1, the Timer Output signal begins as a High (1) and transitions to a Low (0) when the timer value matches the PWM value. The Timer Output signal returns to a High (1) after the timer reaches the reload value and is reset to 0001H.

If the TPOL bit in the Timer Control Register is set to 0, the Timer Output signal begins as a Low (0) and transitions to a High (1) when the timer value matches the PWM value. The Timer Output signal returns to a Low (0) after the timer reaches the reload value and is reset to 0001H.

The timer also generates a second PWM output signal Timer Output Complement. The Timer Output Complement is the complement of the Timer Output PWM signal. A programmable deadband delay can be configured to time delay (0 to 128 system clock cycles) PWM output transitions on these two pins from a low to a high (inactive to active). This ensures a time gap between the deassertion of one PWM output to the assertion of its complement.

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102



## **Receiving Data Using the Interrupt-Driven Method**

The UART Receiver interrupt indicates the availability of new data (as well as error conditions). Observe the following steps to configure the UART receiver for interrupt-driven operation:

- 1. Write to the UART Baud Rate High and Low Byte registers to set the acceptable baud rate.
- 2. Enable the UART pin functions by configuring the associated GPIO port pins for alternate function operation.
- 3. Execute a DI instruction to disable interrupts.
- 4. Write to the Interrupt control registers to enable the UART Receiver interrupt and set the acceptable priority.
- 5. Clear the UART Receiver interrupt in the applicable Interrupt Request register.
- 6. Write to the UART Control 1 Register to enable Multiprocessor (9-bit) mode functions, if appropriate.
  - Set the Multiprocessor Mode Select (MPEN) to Enable MULTIPROCESSOR Mode
  - Set the Multiprocessor Mode Bits, MPMD[1:0], to select the acceptable address matching scheme
  - Configure the UART to interrupt on received data and errors or errors only (interrupt on errors only is unlikely to be useful for Z8 Encore! XP devices without a DMA block)
- 7. Write the device address to the Address Compare Register (automatic MULTIPRO-CESSOR modes only).
- 8. Write to the UART Control 0 Register to:
  - Set the receive enable bit (REN) to enable the UART for data reception
  - Enable parity, if appropriate and if multiprocessor mode is not enabled, and select either even or odd parity
- 9. Execute an EI instruction to enable interrupts.

The UART is now configured for interrupt-driven data reception. When the UART Receiver interrupt is detected, the associated interrupt service routine (ISR) performs the following:

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#### **Transmitter Interrupts**

The transmitter generates a single interrupt when the Transmit Data Register Empty bit (TDRE) is set to 1. This indicates that the transmitter is ready to accept new data for transmission. The TDRE interrupt occurs after the Transmit shift register has shifted the first bit of data out. The Transmit Data Register can now be written with the next character to send. This action provides 7 bit periods of latency to load the Transmit Data Register before the Transmit shift register completes shifting the current character. Writing to the UART Transmit Data Register clears the TDRE bit to 0.

#### **Receiver Interrupts**

The receiver generates an interrupt when any of the following occurs:

• A data byte is received and is available in the UART Receive Data Register. This interrupt can be disabled independently of the other receiver interrupt sources. The received data interrupt occurs after the receive character has been received and placed in the Receive Data Register. To avoid an overrun error, software must respond to this received data available condition before the next character is completely received.

**Note:** In MULTIPROCESSOR Mode (MPEN = 1), the receive data interrupts are dependent on the multiprocessor configuration and the most recent address byte.

- A break is received
- An overrun is detected
- A data framing error is detected

#### **UART Overrun Errors**

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data Register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status 0 Register is updated to indicate the overrun condition (and Break Detect, if applicable). The RDA bit is set to 1 to indicate that the Receive Data Register contains a data byte. However, because the overrun error

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# **UART Transmit Data Register**

Data bytes written to the UART Transmit Data Register (Table 64) are shifted out on the TXDx pin. The Write-only UART Transmit Data Register shares a Register File address with the read-only UART Receive Data Register.

Bit	7	6	5	4	3	2	1	0
Field				T>	(D			
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	W	W	W	W	W	W	W	W
Address				F4	0H			

#### Table 64. UART Transmit Data Register (U0TXD)

Bit	Description
[7:0]	Transmit Data
TXD	UART transmitter data byte to be shifted out through the TXDx pin.

## **UART Receive Data Register**

Data bytes received through the RXD*x* pin are stored in the UART Receive Data Register (Table 65). The read-only UART Receive Data Register shares a Register File address with the Write-only UART Transmit Data Register.

Bit	7	6	5	4	3	2	1	0
Field	RXD							
RESET	Х	Х	Х	Х	Х	Х	Х	Х
R/W	R	R	R	R	R	R	R	R
Address				F4	0H			

Table 65	. UART	Receive	Data	Register	(U0RXD)
----------	--------	---------	------	----------	---------

Bit	Description
[7:0]	Receive Data
RXD	UART receiver data byte from the RXDx pin.



# **Analog-to-Digital Converter**

The Analog-to-Digital Converter (ADC) converts an analog input signal to its digital representation. The features of this sigma-delta ADC include:

- 10-bit resolution
- Eight single-ended analog input sources are multiplexed with general-purpose I/O ports
- Interrupt upon conversion complete
- Bandgap generated internal voltage reference generator with two selectable levels
- Factory offset and gain calibration

# Architecture

Figure 19 displays the major functional blocks of the ADC. An analog multiplexer network selects the ADC input from the available analog pins, ANA0 through ANA7.



Bit	Description								
[7:5]	Reserved								
	These bits are reserved and must be programmed to 111 during writes and to 111 when read.								
[4]	State of Crystal Oscillator at Reset								
XTLDIS	This bit only enables the crystal oscillator. Its selection as a system clock must be performed manually.								
	0 = The crystal oscillator is enabled during reset, resulting in longer reset timing.								
	1 = The crystal oscillator is disabled during reset, resulting in shorter reset timing.								
	<b>Caution:</b> Programming the XTLDIS bit to zero on 8-pin versions of F0823 Series devices prevents any further communication via the debug pin due to the $X_{IN}$ and DBG functions being shared on pin 2 of the 8-pin package. Do not program this bit to zero on 8-pin devices unless no further debugging or Flash programming is required.								
[3:0]	<b>Reserved</b> These bits are reserved and must be programmed to 1111 during writes and to 1111 when read.								

# Trim Bit Address Space

All available trim bit addresses and their functions are listed in Tables 91 through 93.

Bit	7	6	5	4	3	2	1	0	
Field	Reserved								
RESET	U	U	U	U	U	U	U	U	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Address	Information Page Memory 0020H								
Note: U = Unchanged by Reset. R/W = Read/Write.									

#### Table 91. Trim Options Bits at Address 0000H

Bit	Description
[7:0]	Reserved
	These bits are reserved. Altering this register may result in incorrect device operation.

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171

conditions, do not enable the clock failure circuitry (POFEN must be deasserted in the OSCCTL Register).

#### Watchdog Timer Failure

In the event of a Watchdog Timer oscillator failure, a similar non-maskable interrupt-like event is issued. This event does not trigger an attendant clock switch-over, but alerts the CPU of the failure. After a Watchdog Timer failure, it is no longer possible to detect a primary oscillator failure. The failure detection circuitry does not function if the Watchdog Timer is used as the primary oscillator or if the Watchdog Timer oscillator has been disabled. For either of these cases, it is necessary to disable the detection circuitry by deasserting the WDFEN bit of the OSCCTL Register.

The Watchdog Timer oscillator failure detection circuit counts system clocks while searching for a Watchdog Timer clock. The logic counts 8004 system clock cycles before determining that a failure has occurred. The system clock rate determines the speed at which the Watchdog Timer failure can be detected. A very slow system clock results in very slow detection times.

**Caution:** It is possible to disable the clock failure detection circuitry as well as all functioning clock sources. In this case, the Z8 Encore! XP F0823 Series device ceases functioning and can only be recovered by Power-On Reset.

# **Oscillator Control Register Definitions**

The following section provides the bit definitions for the Oscillator Control Register.

#### **Oscillator Control Register**

The Oscillator Control Register (OSCCTL) enables/disables the various oscillator circuits, enables/disables the failure detection/recovery circuitry and selects the primary oscillator, which becomes the system clock.

The Oscillator Control Register must be unlocked before writing. Writing the two step sequence E7H followed by 18H to the Oscillator Control Register unlocks it. The register is locked at successful completion of a register write to the OSCCTL.



# eZ8 CPU Instruction Set

This chapter describes the following features of the eZ8 CPU instruction set: <u>Assembly Language Programming Introduction</u>: see page 174 <u>Assembly Language Syntax</u>: see page 175

eZ8 CPU Instruction Notation: see page 176

eZ8 CPU Instruction Classes: see page 178

eZ8 CPU Instruction Summary: see page 182

# **Assembly Language Programming Introduction**

The eZ8 CPU assembly language provides a means for writing an application program without concern for actual memory addresses or machine instruction formats. A program written in assembly language is called a source program. Assembly language allows the use of symbolic addresses to identify memory locations. It also allows mnemonic codes (opcodes and operands) to represent the instructions themselves. The opcodes identify the instruction while the operands represent memory locations, registers, or immediate data values.

Each assembly language program consists of a series of symbolic commands called *statements*. Each statement can contain labels, operations, operands, and comments.

Labels are assigned to a particular instruction step in a source program. The label identifies that step in the program as an entry point for use by other instructions.

The assembly language also includes assembler directives that supplement the machine instruction. The assembler directives, or pseudo-ops, are not translated into a machine instruction. Rather, the pseudo-ops are interpreted as directives that control or assist the assembly process.

The source program is processed (assembled) by the assembler to obtain a machine language program called the object code. The object code is executed by the eZ8 CPU. An example segment of an assembly language program is detailed in the following example.

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187

Assombly		Address Mode		Opende (c)	Flags						Fotob	Instr
Mnemonic	Symbolic Operation	dst	src	(Hex)	С	Ζ	S	۷	D	Н	Cycles	Cycles
LDX dst, src	dst ← src	r	ER	84	-	_	-	-	-	_	3	2
		lr	ER	85	-						3	3
		R	IRR	86	-						3	4
		IR	IRR	87	-						3	5
		r	X(rr)	88	-						3	4
		X(rr)	r	89	-						3	4
		ER	r	94	-						3	2
		ER	lr	95	-						3	3
		IRR	R	96	-						3	4
		IRR	IR	97	-						3	5
		ER	ER	E8	-						4	2
		ER	IM	E9	-						4	2
LEA dst, X(src)	$dst \gets src + X$	r	X(r)	98	_	_	_	_	_	_	3	3
		rr	X(rr)	99	-						3	5
MULT dst	dst[15:0] ← dst[15:8] * dst[7:0]	RR		F4	-	_	-	-	-	_	2	8
NOP	No operation			0F	-	_	_	-	_	_	1	2
OR dst, src	$dst \gets dst \ OR \ src$	r	r	42	_	*	*	0	_	_	2	3
		r	lr	43	-						2	4
		R	R	44	-						3	3
		R	IR	45	-						3	4
		R	IM	46	-						3	3
		IR	IM	47	-						3	4
ORX dst, src	$dst \gets dst \ OR \ src$	ER	ER	48	_	*	*	0	_	_	4	3
		ER	IM	49	-						4	3
POP dst	dst ← @SP	R		50	-	_	-	-	-	_	2	2
	$SP \leftarrow SP + 1$	IR		51	-						2	3

#### Table 118. eZ8 CPU Instruction Summary (Continued)

Note: Flags Notation:

\* = Value is a function of the result of the operation.

- = Unaffected.

X = Undefined.

0 = Reset to 0.

1 = Set to 1.



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read OCD revision (00H) 163 read OCD status register (02H) 163 read program counter (07H) 164 read program memory (0BH) 164 read program memory CRC (0EH) 165 read register (09H) 164 read runtime counter (03H) 163 step instruction (10H) 165 stuff instruction (11H) 166 write data memory (0CH) 165 write OCD control register (04H) 163 write program counter (06H) 163 write program memory (0AH) 164 write register (08H) 164 on-chip debugger (OCD) 156 on-chip debugger signals 10 ONE-SHOT mode 88 opcode map abbreviations 193 cell description 192 first 194 second after 1FH 195 Operational Description 21, 30, 33, 69, 91, 97, 117, 121, 132, 134, 146, 156, 169, 173 OR 181 ordering information 211 **ORX 181** 

### Ρ

p 176 Packaging 210 part selection guide 2 PC 177 peripheral AC and DC electrical characteristics 201 pin characteristics 11 Pin Descriptions 7 polarity 176 POP 180 pop using extended addressing 180 POPX 180 port availability, device 33 port input timing (GPIO) 205 port output timing, GPIO 206 power supply signals 10
Power-on and Voltage Brownout electrical characteristics and timing 201
Power-On Reset (POR) 23
program control instructions 181
program counter 177
program memory 13
PUSH 180
push using extended addressing 180
PUSHX 180
PWM mode 89
PxADDR register 41
PxCTL register 42

# R

R 176 r 176 RA register address 177 RCF 179. 180 receive IrDA data 119 receiving UART data-interrupt-driven method 102 receiving UART data-polled method 101 register 176 ADC control (ADCCTL) 126, 129 ADC data high byte (ADCDH) 130 ADC data low bits (ADCDL) 131 flash control (FCTL) 141, 148, 149 flash high and low byte (FFREQH and FRE-EQL) 144 flash page select (FPS) 142, 144 flash status (FSTAT) 142 GPIO port A-H address (PxADDR) 41 GPIO port A-H alternate function sub-registers 44 GPIO port A-H control address (PxCTL) 42 GPIO port A-H data direction sub-registers 43 OCD control 166 OCD status 168 UARTx baud rate high byte (UxBRH) 115 UARTx baud rate low byte (UxBRL) 115 UARTx Control 0 (UxCTL0) 112, 115



228

ONE-SHOT mode 70, 88 operating mode 70 PWM mode 75, 76, 89 reading the timer count values 83 reload high and low byte registers 84 timer control register definitions 83 timer output signal operation 83 timers 0-3 control registers 86, 87 high and low byte registers 83, 86 TM 179 **TMX 179** tools, hardware and software 220 transmit IrDA data 118 transmitting UART data-polled method 99 transmitting UART dat-interrupt-driven method 100 **TRAP 181** 

# U

UART 4 architecture 97 baud rate generator 108 control register definitions 108 controller signals 9 interrupts 105 MULTIPROCESSOR mode 103 receiving data using interrupt-driven method 102 receiving data using the polled method 101 transmitting data using the interrupt-driven method 100 transmitting data using the polled method 99 x baud rate high and low registers 115 x control 0 and control 1 registers 112 x status 0 and status 1 registers 110, 111 UxBRH register 115 **UxBRL** register 115 UxCTL0 register 112, 115 UxCTL1 register 113 UxRXD register 109 UxSTAT0 register 110

UxSTAT1 register 111 UxTXD register 109

# V

vector 177 Voltage Brownout reset (VBR) 24

## W

Watchdog Timer approximate time-out delay 91 CNTL 24 control register 94, 171 electrical characteristics and timing 202, 204 interrupt in normal operation 92 interrupt in STOP mode 92 refresh 92, 180 reload unlock sequence 93 reload upper, high and low registers 94 reset 25 reset in normal operation 93 reset in STOP mode 93 time-out response 92 Watchdog Timer Control Register (WDTCTL) 94 WDTCTL register 94, 133, 172 WDTH register 95 WDTL register 95 WDTU register 95 working register 176 working register pair 177

# Χ

X 177 XOR 181 XORX 181

# Ζ

Z8 Encore! block diagram 3 features 1