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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | eZ8 |
| Core Size | 8-Bit |
| Speed | 5MHz |
| Connectivity | IrDA, UART/USART |
| Peripherals | Brown-out Detect/Reset, LED, POR, PWM, WDT |
| Number of I/O | 22 |
| Program Memory Size | 8KB (8K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 2.7V ~ 3.6V |
| Data Converters | A/D 8x10b |
| Oscillator Type | Internal |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 28-SSOP (0.209", 5.30mm Width) |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/zilog/z8f0823hj005sg |

# Overview

Zilog's Z8 Encore! XP microcontroller unit (MCU) family of products are the first Zilog microcontroller products based on the 8-bit eZ8 CPU core. Z8 Encore! XP F0823 Series products expand upon Zilog's extensive line of 8-bit microcontrollers. The Flash in-circuit programming capability allows for faster development time and program changes in the field. The new eZ8 CPU is upward compatible with existing Z8 instructions. The rich peripheral set of Z8 Encore! XP F0823 Series makes it suitable for a variety of applications including motor control, security systems, home appliances, personal electronic devices, and sensors.

## Features

The key features of Z8 Encore! XP F0823 Series include:

- 5MHz eZ8 CPU
- 1KB, 2KB, 4KB, or 8KB Flash memory with in-circuit programming capability
- 256B, 512B, or 1KB register RAM
- 6 to 24 I/O pins depending upon package
- Internal precision oscillator (IPO)
- Full-duplex UART
- The universal asynchronous receiver/transmitter (UART) baud rate generator (BRG) can be configured and used as a basic 16-bit timer
- Infrared data association (IrDA)-compliant infrared encoder/decoders, integrated with UART
- Two enhanced 16-bit timers with capture, compare, and PWM capability
- Watchdog Timer (WDT) with dedicated internal RC oscillator
- On-Chip Debugger (OCD)
- Optional 8-channel, 10-bit Analog-to-Digital Converter (ADC)
- On-Chip analog comparator
- Up to 20 vectored interrupts
- Direct LED drive with programmable drive strengths
- Voltage Brown-Out (VBO) protection
- Power-On Reset (POR)

# Pin Description

Z8 Encore! XP F0823 Series products are available in a variety of package styles and pin configurations. This chapter describes the signals and pin configurations available for each of the package styles. For information about physical package specifications, see the Packaging chapter on page 210.

## Available Packages

Table 2 lists the package styles that are available for each device in the F0823 Series product line.

**Table 2. F0823 Series Package Options**

| Part Number | ADC | 8-pin PDIP | 8-pin SOIC | 20-pin PDIP | 20-pin SOIC | 20-pin SSOP | 28-pin PDIP | 28-pin SOIC | 28-pin SSOP | 8-pin QFN/ MLF-S |
|---|---|---|---|---|---|---|---|---|---|---|
| Z8F0823 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0813 | No | X | X | X | X | X | X | X | X | X |
| Z8F0423 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0413 | No | X | X | X | X | X | X | X | X | X |
| Z8F0223 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0213 | No | X | X | X | X | X | X | X | X | X |
| Z8F0123 | Yes | X | X | X | X | X | X | X | X | X |
| Z8F0113 | No | X | X | X | X | X | X | X | X | X |

## Pin Configurations

Figures 2 through 4 display the pin configurations for all packages available in the F0823 Series. For description of signals, see Table 3. The analog input alternate functions (ANA*x*) are not available on the Z8F0x13 devices. The analog supply pins ($AV_{DD}$ and $AV_{SS}$) are also not available on these parts, and are replaced by PB6 and PB7.

At reset, all pins of Ports A, B, and C default to an input state. In addition, any alternate functionality is not enabled, so the pins function as general-purpose input ports until programmed otherwise.

The pin configurations listed are preliminary and subject to change based on manufacturing limitations.

Table 5 provides detailed information about the characteristics for each pin available on Z8 Encore! XP F0823 Series 8-pin devices.

**Table 5. Pin Characteristics (8-Pin Devices)**

| Symbol Mnemonic | Direction | Reset Direction | Active Low or Active High | Tristate Output | Internal Pull-up or Pull-down | Schmitt-Trigger Input | Open Drain Output | 5V Tolerance |
|---|---|---|---|---|---|---|---|---|
| PA0/DBG | I/O | I (but can change during reset if key sequence detected) | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| PA1 | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| $\overline{\text{RESET}}$/PA2 | I/O | I/O (defaults to $\overline{\text{RESET}}$) | N/A | Yes | Programmable for PA2; always on for $\overline{\text{RESET}}$ | Yes | Programmable for PA2; always on for $\overline{\text{RESET}}$ | Yes, unless pull-ups enabled |
| PA[5:3] | I/O | I | N/A | Yes | Programmable Pull-up | Yes | Yes, Programmable | Yes, unless pull-ups enabled |
| VDD | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| VSS | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |

**Table 8. Register File Address Map (Continued)**

| Address (Hex) | Register Description | Mnemonic | Reset (Hex) | Page No. |
|---|---|---|---|---|
| **eZ8 CPU** | | | | |
| FFC | Flags | — | XX | Refer to the eZ8 CPU Core User Manual (UM0128) |
| FFD | Register Pointer | RP | XX | |
| FFE | Stack Pointer High Byte | SPH | XX | |
| FFF | Stack Pointer Low Byte | SPL | XX | |

Note: XX=Undefined.

During a System Reset or Stop Mode Recovery, the IPO requires 4 µs to start up. Then the Z8 Encore! XP F0823 Series device is held in Reset for 66 cycles of the Internal Precision Oscillator. If the crystal oscillator is enabled in the Flash option bits, this reset period is increased to 5000 IPO cycles. When a reset occurs because of a low voltage condition or Power-On Reset, this delay is measured from the time that the supply voltage first exceeds the POR level. If the external pin reset remains asserted at the end of the reset period, the device remains in reset until the pin is deasserted.

At the beginning of Reset, all GPIO pins are configured as inputs with pull-up resistor disabled.

During Reset, the eZ8 CPU and on-chip peripherals are idle; however, the on-chip crystal oscillator and Watchdog Timer oscillator continue to run.

Upon Reset, control registers within the Register File that have a defined Reset value are loaded with their reset values. Other control registers (including the Stack Pointer, Register Pointer, and Flags) and general-purpose RAM are undefined following Reset. The eZ8 CPU fetches the Reset vector at Program Memory addresses `0002H` and `0003H` and loads that value into the Program Counter. Program execution begins at the Reset vector address.

When the control registers are re-initialized by a system reset, the system clock after reset is always the IPO. The software must reconfigure the oscillator control block, such that the correct system clock source is enabled and selected.

## LED Drive Level High Register

The LED Drive Level registers contain two control bits for each Port C pin (Table 33). These two bits select between four programmable drive levels. Each pin is individually programmable.

**Table 33. LED Drive Level High Register (LEDLVLH)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | LEDLVLH[7:0] | | | | | | | |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F83H | | | | | | | |

| Bit | Description |
|---|---|
| [7:0] LEDLVLH | **LED Level High Bit**<br>{LEDLVLH, LEDLVLL} select one of four programmable current drive levels for each Port C pin.<br>00 = 3mA.<br>01= 7mA.<br>10= 13mA.<br>11= 20mA. |

# Architecture

Figure 8 displays the interrupt controller block diagram.

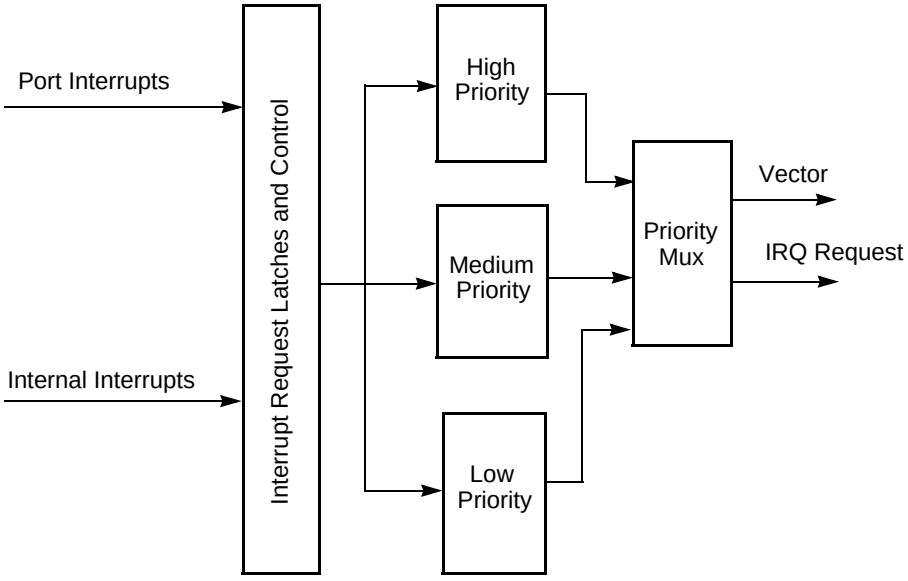


**Figure 8. Interrupt Controller Block Diagram**

# Operation

This section describes the operational aspects of the following functions.

Master Interrupt Enable: see page 56

Interrupt Vectors and Priority: see page 57

Interrupt Assertion: see page 57

Software Interrupt Assertion: see page 58

Watchdog Timer Interrupt Assertion: see page 58

## Master Interrupt Enable

The master interrupt enable bit (IRQE) in the Interrupt Control Register globally enables and disables interrupts.

Interrupts are globally enabled by any of the following actions:

- Execution of an Enable Interrupt (EI) instruction

# Universal Asynchronous Receiver/ Transmitter

The universal asynchronous receiver/transmitter (UART) is a full-duplex communication channel capable of handling asynchronous data transfers. The UART uses a single 8-bit data mode with selectable parity. The features of UART include:

- 8-bit asynchronous data transfer
- Selectable even- and odd-parity generation and checking
- Option of one or two STOP bits
- Separate transmit and receive interrupts
- Framing, parity, overrun, and break detection
- Separate transmit and receive enables
- 16-bit baud rate generator (BRG)
- Selectable MULTIPROCESSOR (9-bit) Mode with three configurable interrupt schemes
- BRG can be configured and used as a basic 16-bit timer
- Driver Enable output for external bus transceivers

## Architecture

The UART consists of three primary functional blocks: transmitter, receiver, and baud rate generator. The UART's transmitter and receiver function independently, but employ the same baud rate and data format. Figure 10 displays the UART architecture.

## UART Status 0 Register

The UART Status 0 and Status 1 registers (Table 66 and Table 67) identify the current UART operating configuration and status.

**Table 66. UART Status 0 Register (U0STAT0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | RDA | PE | OE | FE | BRKD | TDRE | TXE | CTS |
| RESET | 0 | 0 | 0 | 0 | 0 | 1 | 1 | X |
| R/W | R | R | R | R | R | R | R | R |
| Address | F41H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>RDA | **Receive Data Available**<br>This bit indicates that the UART Receive Data Register has received data. Reading the UART Receive Data Register clears this bit.<br>0 = The UART Receive Data Register is empty.<br>1 = There is a byte in the UART Receive Data Register. |
| [6]<br>PE | **Parity Error**<br>This bit indicates that a parity error has occurred. Reading the UART Receive Data register clears this bit.<br>0 = No parity error has occurred.<br>1 = A parity error has occurred. |
| [5]<br>OE | **Overrun Error**<br>This bit indicates that an overrun error has occurred. An overrun occurs when new data is received and the UART Receive Data Register has not been read. If the RDA bit is reset to 0, reading the UART Receive Data Register clears this bit.<br>0 = No overrun error occurred.<br>1 = An overrun error occurred. |
| [4]<br>FE | **Framing Error**<br>This bit indicates that a framing error (no Stop bit following data reception) was detected. Reading the UART Receive Data Register clears this bit.<br>0 = No framing error occurred.<br>1 = A framing error occurred. |
| [3]<br>BRKD | **Break Detect**<br>This bit indicates that a break occurred. If the data bits, parity/multiprocessor bit, and Stop bit(s) are all 0s this bit is set to 1. Reading the UART Receive Data Register clears this bit.<br>0 = No break occurred.<br>1 = A break occurred. |

## UART Control 0 and Control 1 Registers

The UART Control 0 and Control 1 registers (Table 68 and Table 69) configure the properties of the UART's transmit and receive operations. The UART Control registers must not be written while the UART is enabled.

**Table 68. UART Control 0 Register (U0CTL0)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | TEN | REN | CTSE | PEN | PSEL | SBRK | STOP | LBEN |
| RESET | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F42H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>TEN | **Transmit Enable**<br>This bit enables or disables the transmitter. The enable is also controlled by the $\overline{\text{CTS}}$ signal and the CTSE bit. If the $\overline{\text{CTS}}$ signal is low and the CTSE bit is 1, the transmitter is enabled.<br>0 = Transmitter disabled.<br>1 = Transmitter enabled. |
| [6]<br>REN | **Receive Enable**<br>This bit enables or disables the receiver.<br>0 = Receiver disabled.<br>1 = Receiver enabled. |
| [5]<br>CTSE | **CTSE—$\overline{\text{CTS}}$ Enable**<br>0 = The $\overline{\text{CTS}}$ signal has no effect on the transmitter.<br>1 = The UART recognizes the $\overline{\text{CTS}}$ signal as an enable control from the transmitter. |
| [4]<br>PEN | **Parity Enable**<br>This bit enables or disables parity. Even or odd is determined by the PSEL bit.<br>0 = Parity is disabled.<br>1 = The transmitter sends data with an additional parity bit and the receiver receives an additional parity bit . |
| [3]<br>PSEL | **Parity Select**<br>0 = Even parity is transmitted and expected on all received data.<br>1 = Odd parity is transmitted and expected on all received data. |
| [2]<br>SBRK | **Send Break**<br>This bit pauses or breaks data transmission. Sending a break interrupts any transmission in progress, so ensure that the transmitter has finished sending data before setting this bit.<br>0 = No break is sent.<br>1 = Forces a break condition by setting the output of the transmitter to zero. |

The UART data rate is calculated using the following equation:

$$\text{UART Baud Rate (bits/s)} = \frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Baud Rate Divisor Value}}$$

For a given UART data rate, calculate the integer baud rate divisor value using the following equation:

$$\text{UART Baud Rate Divisor Value (BRG)} = \text{Round}\left(\frac{\text{System Clock Frequency (Hz)}}{16 \times \text{UART Data Rate (bits/s)}}\right)$$

The baud rate error relative to the acceptable baud rate is calculated using the following equation:

$$\text{UART Baud Rate Error (\%)} = 100 \times \left(\frac{\text{Actual Data Rate} - \text{Desired Data Rate}}{\text{Desired Data Rate}}\right)$$

For reliable communication, the UART baud rate error must never exceed five percent. Table 73 provides information about data rate errors for a 5.5296 MHz System Clock.

**Table 73. UART Baud Rates**

| 5.5296 MHz System Clock | | | |
|---|---|---|---|
| **Acceptable Rate (kHz)** | **BRG Divisor (Decimal)** | **Actual Rate (kHz)** | **Error (%)** |
| 1250.0 | N/A | N/A | N/A |
| 625.0 | N/A | N/A | N/A |
| 250.0 | 1 | 345.6 | 38.24 |
| 115.2 | 3 | 115.2 | 0.00 |
| 57.6 | 6 | 57.6 | 0.00 |
| 38.4 | 9 | 38.4 | 0.00 |
| 19.2 | 18 | 19.2 | 0.00 |
| 9.60 | 36 | 9.60 | 0.00 |
| 4.80 | 72 | 4.80 | 0.00 |
| 2.40 | 144 | 2.40 | 0.00 |
| 1.20 | 288 | 1.20 | 0.00 |
| 0.60 | 576 | 0.60 | 0.00 |
| 0.30 | 1152 | 0.30 | 0.00 |

## Receiving IrDA Data

Data received from the infrared transceiver using the IR_RXD signal through the RXD pin is decoded by the infrared endec and passed to the UART. The UART's baud rate clock is used by the infrared endec to generate the demodulated signal (RXD) that drives the UART. Each UART/Infrared data bit is 16-clocks wide. Figure 18 displays data reception. When the infrared endec is enabled, the UART's RXD signal is internal to the Z8 Encore! XP F0823 Series products while the IR_RXD signal is received through the RXD pin.

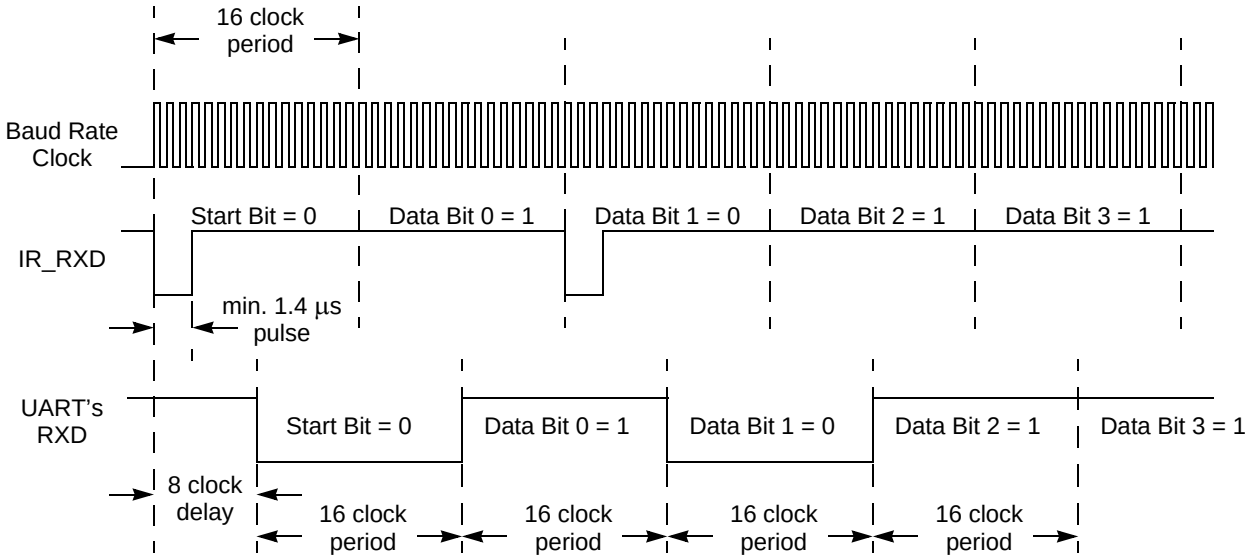


**Figure 18. IrDA Data Reception**

### Infrared Data Reception

**Caution:** The system clock frequency must be at least 1.0MHz to ensure proper reception of the 1.4µs minimum width pulses allowed by the IrDA standard.

### Endec Receiver Synchronization

The IrDA receiver uses a local baud rate clock counter (0 to 15 clock periods) to generate an input stream for the UART and to create a sampling window for detection of incoming pulses. The generated UART input (UART RXD) is delayed by 8 baud rate clock periods with respect to the incoming IrDA data stream. When a falling edge in the input data stream is detected, the endec counter is reset. When the count reaches a value of 8, the UART RXD value is updated to reflect the value of the decoded data. When the count reaches 12 baud clock periods, the sampling window for the next incoming pulse opens.

## ADC Control/Status Register 1

The second ADC Control Register contains the voltage reference level selection bit.

**Table 75. ADC Control/Status Register 1 (ADCCTL1)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | REFSELH | Reserved | | | | | | |
| RESET | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | F71H | | | | | | | |

| Bit | Description |
|---|---|
| [7]<br>REFSELH | **Voltage Reference Level Select High Bit**<br>In conjunction with the Low bit (REFSELL) in ADC Control Register 0, this bit determines the level of the internal voltage reference; the following details the effects of {REFSELH, REFSELL}; this reference is independent of the Comparator reference.<br>00 = Internal Reference Disabled, reference comes from external pin.<br>01 = Internal Reference set to 1.0V.<br>10 = Internal Reference set to 2.0V (default). |
| [6:0] | **Reserved**<br>These bits are reserved and must be programmed to 0000000. |

# Operation

The following section describes the operation of the OCD.

## OCD Interface

The OCD uses the DBG pin for communication with an external host. This one-pin interface is a bidirectional open-drain interface that transmits and receives data. Data transmission is half-duplex, in that transmit and receive cannot occur simultaneously. The serial data on the DBG pin is sent using the standard asynchronous data format defined in RS-232. This pin creates an interface from the F0823 Series products to the serial port of a host PC using minimal external hardware.Two different methods for connecting the DBG pin to an RS-232 interface are displayed in Figure 23 and Figure 24. The recommended method is the buffered implementation depicted in Figure 24. The DBG pin has a internal pull-up resistor which is sufficient for some applications (for more details about the pull-up current, see the Electrical Characteristics chapter on page 196). For OCD operation at higher data rates or in noisy systems, Zilog recommends an external pull-up resistor.

**! Caution:** For operation of the OCD, all power pins ($V_{DD}$ and $AV_{DD}$) must be supplied with power, and all ground pins ($V_{SS}$ and $AV_{SS}$) must be properly grounded. The DBG pin is open-drain and may require an external pull-up resistor to ensure proper operation.

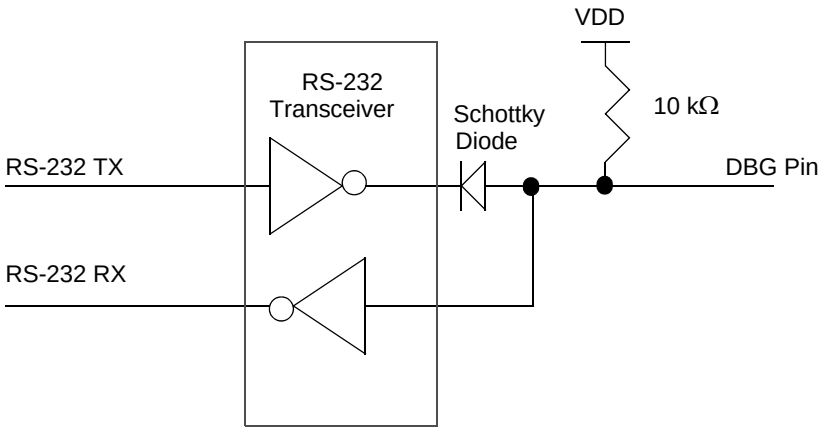


**Figure 23. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, # 1 of 2**

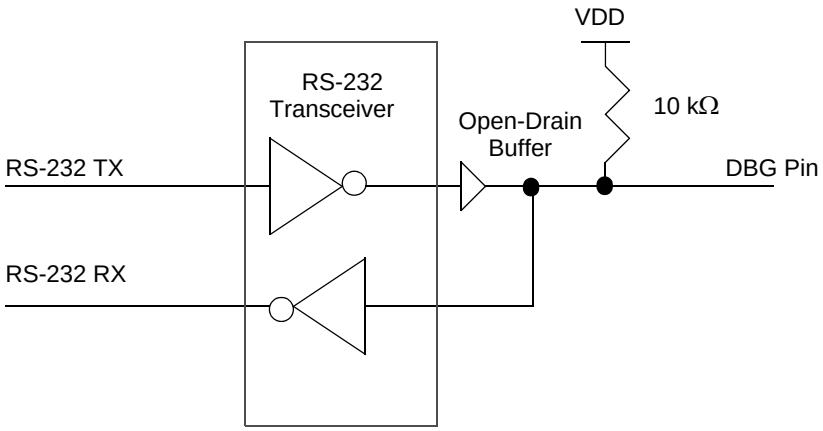


**Figure 24. Interfacing the On-Chip Debugger's DBG Pin with an RS-232 Interface, # 2 of 2**

## DEBUG Mode

The operating characteristics of the devices in DEBUG Mode are:

- The eZ8 CPU fetch unit stops, idling the eZ8 CPU, unless directed by the OCD to execute specific instructions
- The system clock operates unless in STOP Mode
- All enabled on-chip peripherals operate unless in STOP Mode
- Automatically exits HALT Mode
- Constantly refreshes the Watchdog Timer, if enabled.

### Entering DEBUG Mode

The device enters DEBUG Mode following the operations below:

- The device enters DEBUG Mode after the eZ8 CPU executes a BRK (breakpoint) instruction
- If the DBG pin is held Low during the most recent clock cycle of System Reset, the part enters DEBUG Mode upon exiting System Reset

**Note:** Holding the DBG pin Low for an additional 5000 (minimum) clock cycles after reset (making sure to account for any specified frequency error if using an internal oscillator) prevents a false interpretation of an autobaud sequence (see the OCD Autobaud Detector/ Generator section on page 159).

**Stuff Instruction (11H).** The Stuff command steps one assembly instruction and allows specification of the first byte of the instruction. The remaining 0–4 bytes of the instruction are read from Program Memory. This command is useful for stepping over instructions where the first byte of the instruction has been overwritten by a Breakpoint. If the device is not in DEBUG Mode or the Flash Read Protect Option bit is enabled, the OCD ignores this command.

```
DBG ← 11H
DBG ← opcode[7:0]
```

**Execute Instruction (12H).** The Execute command allows sending an entire instruction to be executed to the eZ8 CPU. This command can also step over breakpoints. The number of bytes to send for the instruction depends on the opcode. If the device is not in DEBUG Mode or the Flash Read Protect Option bit is enabled, this command reads and discards one byte.

```
DBG ← 12H
DBG ← 1–5 byte opcode
```

# On-Chip Debugger Control Register Definitions

This section describes the features of the On-Chip Debugger Control and Status registers.

## OCD Control Register

The OCD Control Register controls the state of the OCD. This register is used to enter or exit DEBUG Mode and to enable the BRK instruction. It also resets Z8 Encore! XP F0823 Series device.

A reset and stop function can be achieved by writing 81H to this register. A reset and go function can be achieved by writing 41H to this register. If the device is in DEBUG Mode, a run function can be implemented by writing 40H to this register.

**Table 107. Assembly Language Syntax Example 2**

| | | | | |
|---|---|---|---|---|
| **Assembly Language Code** | ADD | 43H, | R8 | (ADD dst, src) |
| **Object Code** | 04 | E8 | 43 | (OPC src, dst) |

See the device-specific Z8 Encore! XP Product Specification to determine the exact register file range available. The register file size varies, depending on the device type.

# eZ8 CPU Instruction Notation

In the eZ8 CPU Instruction Summary and Description sections, the operands, condition codes, status flags, and address modes are represented by a notational shorthand that is noted in Table 108.

**Table 108. Notational Shorthand**

| Notation | Description | Operand | Range |
|---|---|---|---|
| b | Bit | b | b represents a value from 0 to 7 (000B to 111B). |
| cc | Condition Code | — | See the Condition Codes overview in the eZ8 CPU Core User Manual (UM0128). |
| DA | Direct Address | Addrs | Addrs represents a number in the range of 0000H to FFFFH. |
| ER | Extended Addressing Register | Reg | Reg represents a number in the range of 000H to FFFH. |
| IM | Immediate Data | #Data | Data is a number between 00H to FFH. |
| Ir | Indirect Working Register | @Rn | n = 0–15. |
| IR | Indirect Register | @Reg | Reg. represents a number in the range of 00H to FFH. |
| Irr | Indirect Working Register Pair | @RRp | p = 0, 2, 4, 6, 8, 10, 12, or 14. |
| IRR | Indirect Register Pair | @Reg | Reg represents an even number in the range 00H to FEH |
| p | Polarity | p | Polarity is a single bit binary value of either 0B or 1B. |
| r | Working Register | Rn | n = 0–15. |
| R | Register | Reg | Reg. represents a number in the range of 00H to FFH. |

**Table 121. DC Characteristics (Continued)**

| | | $T_A$ = –40°C to +105°C (unless otherwise specified) | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $I_{LED}$ | Controlled Current Drive | 1.8 | 3 | 4.5 | mA | {AFS2,AFS1} = {0,0}. |
| | | 2.8 | 7 | 10.5 | mA | {AFS2,AFS1} = {0,1}. |
| | | 7.8 | 13 | 19.5 | mA | {AFS2,AFS1} = {1,0}. |
| | | 12 | 20 | 30 | mA | {AFS2,AFS1} = {1,1}. |
| $C_{PAD}$ | GPIO Port Pad Capacitance | – | 8.0[2] | – | pF | |
| $C_{XIN}$ | $X_{IN}$ Pad Capacitance | – | 8.0[2] | – | pF | |
| $C_{XOUT}$ | $X_{OUT}$ Pad Capacitance | – | 9.5[2] | – | pF | |
| $I_{PU}$ | Weak Pull-up Current | 30 | 100 | 350 | µA | $V_{DD}$ = 3.0V–3.6V. |
| $V_{RAM}$ | RAM Data Retention Voltage | TBD | | | V | Voltage at which RAM retains static values; no reading or writing is allowed. |

Notes:
1. This condition excludes all pins that have on-chip pull-ups, when driven Low.
2. These values are provided for design guidance only and are not tested in production.

# AC Characteristics

The section provides information about the AC characteristics and timing. All AC timing information assumes a standard load of 50 pF on all outputs.

**Table 123. AC Characteristics**

| | | $V_{DD}$ = 2.7V to 3.6V<br>$T_A$ = –40°C to +105°C<br>(unless otherwise stated) | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Maximum** | **Units** | **Conditions** |
| $F_{SYSCLK}$ | System Clock Frequency | – | 20.0* | MHz | Read-only from Flash memory. |
| | | 0.032768 | 20.0[1] | MHz | Program or erasure of the Flash memory. |
| $T_{XIN}$ | System Clock Period | 50 | – | ns | $T_{CLK} = 1/F_{SYSCLK}$. |
| $T_{XINH}$ | System Clock High Time | 20 | 30 | ns | $T_{CLK}$ = 50ns. |
| $T_{XINL}$ | System Clock Low Time | 20 | 30 | ns | $T_{CLK}$ = 50ns. |
| $T_{XINR}$ | System Clock Rise Time | – | 3 | ns | $T_{CLK}$ = 50ns. |
| $T_{XINF}$ | System Clock Fall Time | – | 3 | ns | $T_{CLK}$ = 50ns. |

Note: *System Clock Frequency is limited by the Internal Precision Oscillator on the Z8 Encore! XP F0823 Series. See Table 124 on page 200.

**Table 124. Internal Precision Oscillator Electrical Characteristics**

| | | $V_{DD}$ = 2.7V to 3.6V<br>$T_A$ = –40°C to +105°C<br>(unless otherwise stated) | | | | |
|---|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Minimum** | **Typical** | **Maximum** | **Units** | **Conditions** |
| $F_{IPO}$ | Internal Precision Oscillator Frequency (High Speed) | | 5.53 | | MHz | $V_{DD}$ = 3.3V<br>$T_A$ = 30°C |
| $F_{IPO}$ | Internal Precision Oscillator Frequency (Low Speed) | | 32.7 | | kHz | $V_{DD}$ = 3.3V<br>$T_A$ = 30°C |
| $F_{IPO}$ | Internal Precision Oscillator Error | | ±1 | ±4 | % | |
| $T_{IPOST}$ | Internal Precision Oscillator Startup Time | | 3 | | µs | |

## Part Number Suffix Designations

Zilog part numbers consist of a number of components, as indicated in the following example.

**Example.** Part number Z8F0423SH005SG is an 8-bit 20MHz Flash MCU with 4KB of Program Memory and equipped with 6–22 I/O lines and 4–8 ADC channels in a 20-pin SOIC package, operating within a 0ºC to +70ºC temperature range and built using lead-free solder.