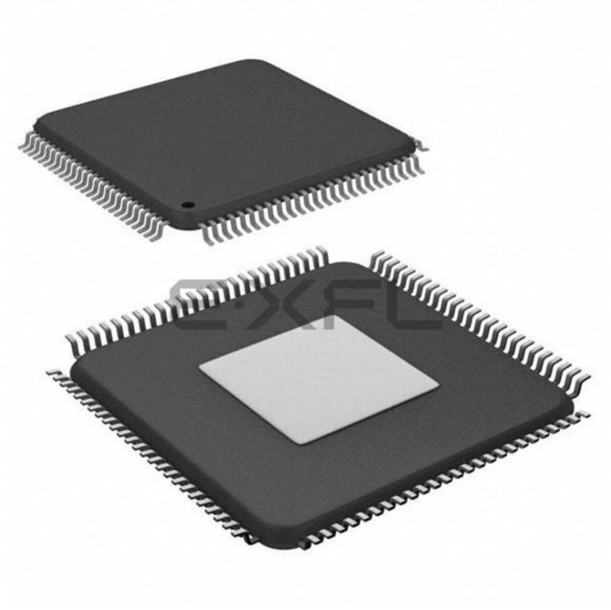
Infineon Technologies - XMC4300F100K256AAXUMA1 Datasheet



Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	144MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, MMC/SD, SPI, UART/USART, USB OTG, USIC
Peripherals	DMA, I²S, LED, POR, Touch-Sense, WDT
Number of I/O	75
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	3.13V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-25
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xmc4300f100k256aaxuma1

About this Document

This Data Sheet is addressed to embedded hardware and software developers. It provides the reader with detailed descriptions about the ordering designations, available features, electrical and physical characteristics of the XMC4300 series devices.

The document describes the characteristics of a superset of the XMC4300 series devices. For simplicity, the various device types are referred to by the collective term XMC4300 throughout this manual.

XMC4000 Family User Documentation

The set of user documentation includes:

- **Reference Manual**
  - decribes the functionality of the superset of devices.
- **Data Sheets**
  - list the complete ordering designations, available features and electrical characteristics of derivative devices.
- **Errata Sheets**
  - list deviations from the specifications given in the related Reference Manual or Data Sheets. Errata Sheets are provided for the superset of devices.

Attention: Please consult all parts of the documentation set to attain consolidated knowledge about your device.

Application related guidance is provided by **Users Guides** and **Application Notes**.

Please refer to **http://www.infineon.com/xmc4000** to get access to the latest versions of those documents.

Table 9 Package Pin Mapping (cont'd)

Function	**LQFP-100**	**Pad Type**	**Notes**
P1.0	79	A1+	
P1.1	78	A1+	
P1.2	77	A2	
P1.3	76	A2	
P1.4	75	A1+	
P1.5	74	A1+	
P1.6	83	A2	
P1.7	82	A2	
P1.8	81	A2	
P1.9	80	A2	
P1.10	73	A1+	
P1.11	72	A1+	
P1.12	71	A2	
P1.13	70	A2	
P1.14	69	A2	
P1.15	68	A2	
P2.0	52	A2	
P2.1	51	A2	After a system reset, via HWSEL this pin selects the DB.TDO function.
P2.2	50	A2	
P2.3	49	A2	
P2.4	48	A2	
P2.5	47	A2	
P2.6	54	A1+	
P2.7	53	A1+	
P2.8	46	A2	
P2.9	45	A2	
P2.10	44	A2	
P2.14	41	A2	
P2.15	40	A2	
P3.0	7	A2	
P3.1	6	A2	

2.3 Power Connection Scheme

Figure 5. shows a reference power connection scheme for the XMC4300.

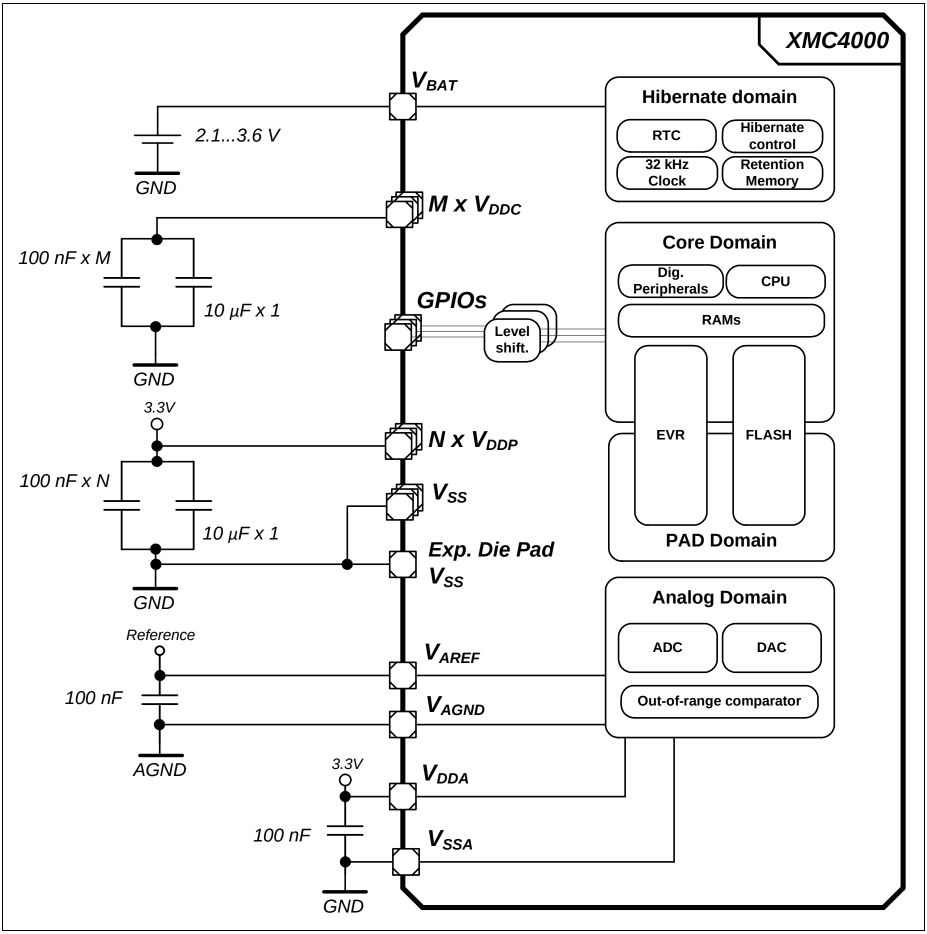


Figure 5 Power Connection Scheme

Every power supply pin needs to be connected. Different pins of the same supply need also to be externally connected. As example, all V_{DDP} pins must be connected externally to one V_{DDP} net. In this reference scheme one 100 nF capacitor is connected at each supply pin against V_{SS}. An additional 10 µF capacitor is connected to the V_{DDP} nets and an additional 10 uF capacitor to the V_{DDC} nets.

The XMC4300 has a common ground concept, all V_{SS}, V_{SSA} and V_{SSO} pins share the same ground potential. In packages with an exposed die pad it must be connected to the common ground as well.
V_{AGND} is the low potential to the analog reference V_{AREF}. Depending on the application it can share the common ground or have a different potential. In devices with shared V_{DDA}/V_{AREF} and V_{SSA}/V_{AGND} pins the reference is tied to the supply. Some analog channels can optionally serve as “Alternate Reference”; further details on this operating mode are described in the Reference Manual.

When V_{DDP} is supplied, V_{BAT} must be supplied as well. If no other supply source (e.g. battery) is connected to V_{BAT}, the V_{BAT} pin can also be connected directly to V_{DDP}.

3.1.2 Absolute Maximum Ratings

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol		Values			Unit	Note / Test Con dition
			Min.	Typ.	Max.		
Storage temperature	T_{ST}	SR	-65	–	150	°C	–
Junction temperature	T_J	SR	-40	–	150	°C	–
Voltage at 3.3 V power supply pins with respect to V_{SS}	V_{DDP}	SR	–	–	4.3	V	–
Voltage on any Class A and dedicated input pin with respect to V_{SS}	V_{IN}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Voltage on any analog input pin with respect to V_{AGND}	V_{AIN} V_{AREF}	SR	-1.0	–	V_{DDP} + 1.0 or max. 4.3	V	whichever is lower
Input current on any pin during overload condition	I_{IN}	SR	-10	–	+10	mA	
Absolute maximum sum of all input circuit currents for one port group during overload condition[1]	ΣI_{IN}	SR	-25	–	+25	mA	
Absolute maximum sum of all input circuit currents during overload condition	ΣI_{IN}	SR	-100	–	+100	mA	

[1] The port groups are defined in **Table 16**.

Figure 6 explains the input voltage ranges of V_{IN} and V_{AIN} and its dependency to the supply level of V_{DDP}.The input voltage must not exceed 4.3 V, and it must not be more than 1.0 V above V_{DDP}. For the range up to V_{DDP} + 1.0 V also see the definition of the overload conditions in **Section 3.1.3**.

3.1.4 Pad Driver and Pad Classes Summary

This section gives an overview on the different pad driver classes and their basic characteristics.

Table 17 Pad Driver and Pad Classes Overview

Class	Power Supply	Type	Sub-Class	Speed Grade	Load	Termination
A	3.3 V	LVTTL I/O	**A1** (e.g. GPIO)	6 MHz	100 pF	No
			A1+ (e.g. serial I/Os)	25 MHz	50 pF	Series termination recommended
			A2 (e.g. ext. Bus)	80 MHz	15 pF	Series termination recommended

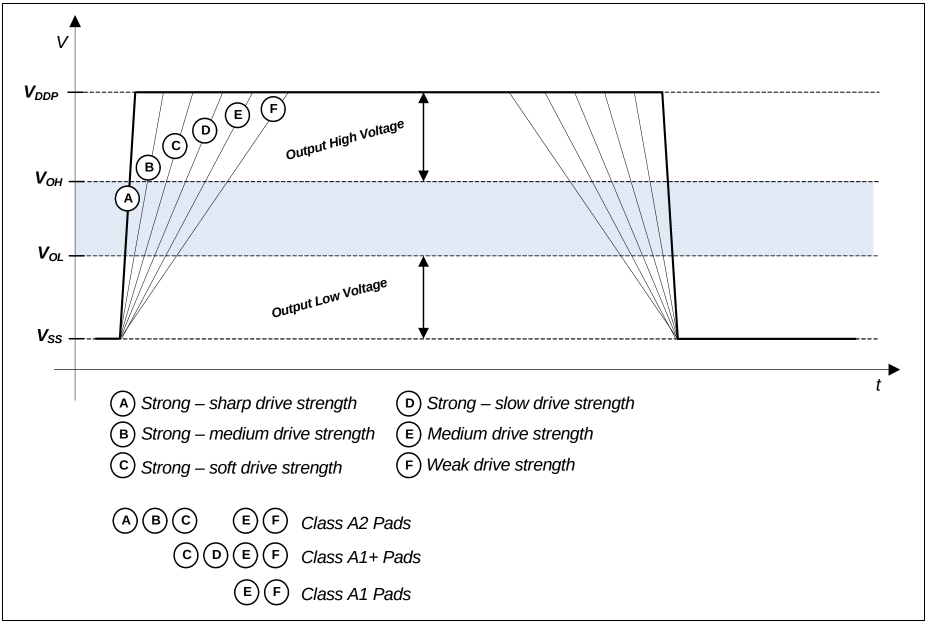


Figure 8 Output Slopes with different Pad Driver Modes

Figure 8 is a qualitative display of the resulting output slope performance with different output driver modes. The detailed input and output characteristics are listed in **Section 3.2.1**.

3.1.5 Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the XMC4300. All parameters specified in the following sections refer to these operating conditions, unless noted otherwise.

Table 18 Operating Conditions Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Ambient Temperature	T_A SR	-40	–	85	°C	Temp. Range F
		-40	–	125	°C	Temp. Range K
Digital supply voltage	V_{DDP} SR	3.13[1]	3.3	3.63 [2]	V	
Core Supply Voltage	V_{DDC} CC	–[1]	1.3	–	V	Generated internally
Digital ground voltage	V_{SS} SR	0	–	–	V	
ADC analog supply voltage	V_{DDA} SR	3.0	3.3	3.6[2]	V	
Analog ground voltage for V_{DDA}	V_{SSA} SR	-0.1	0	0.1	V	
Battery Supply Voltage for Hibernate Domain	V_{BAT} SR	1.95[3]	–	3.63	V	When V_{DDP} is supplied V_{BAT} has to be supplied as well.
System Frequency	f_{SYS} SR	–	–	144	MHz	
Short circuit current of digital outputs	I_{SC} SR	-5	–	5	mA	
Absolute sum of short circuit currents per pin group[4]	ΣI_{SC_PG} SR	–	–	20	mA	
Absolute sum of short circuit currents of the device	ΣI_{SC_D} SR	–	–	100	mA	

[1] See also the Supply Monitoring thresholds, **Section 3.3.2**.

[2] Voltage overshoot to 4.0 V is permissible at Power-Up and $\overline{\text{PORST}}$ low, provided the pulse duration is less than 100 µs and the cumulated sum of the pulses does not exceed 1 h over lifetime.

[3] To start the hibernate domain it is required that $V_{BAT} \geq 2.1$ V, for a reliable start of the oscillation of RTC_XTAL in crystal mode it is required that $V_{BAT} \geq 3.0$ V.

[4] The port groups are defined in **Table 16**.

Table 20 Standard Pads Class_A1

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZA1} CC	-500		500	nA	$0 \mathrm{~V} \le V_{\mathrm{IN}} \le V_{\mathrm{DDP}}$
Input high voltage	V_{IHA1} SR	$0.6 \times V_{\mathrm{DDP}}$		$V_{\mathrm{DDP}} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILA1} SR	-0.3		$0.36 \times V_{\mathrm{DDP}}$	V	
Output high voltage, POD[1] = weak	V_{OHA1} CC	V_{DDP} - 0.4		–	V	$I_{\mathrm{OH}} \ge -400~\mu\mathrm{A}$
		2.4		–	V	$I_{\mathrm{OH}} \ge -500~\mu\mathrm{A}$
Output high voltage, POD[1] = medium		V_{DDP} - 0.4		–	V	$I_{\mathrm{OH}} \ge -1.4 \mathrm{~mA}$
		2.4		–	V	$I_{\mathrm{OH}} \ge -2 \mathrm{~mA}$
Output low voltage	V_{OLA1} CC	–		0.4	V	$I_{\mathrm{OL}} \le 500~\mu\mathrm{A}$; POD[1] = weak
		–		0.4	V	$I_{\mathrm{OL}} \le 2 \mathrm{~mA}$; POD[1] = medium
Fall time	t_{FA1} CC	–		150	ns	$C_{\mathrm{L}} = 20 \mathrm{~pF}$; POD[1] = weak
		–		50	ns	$C_{\mathrm{L}} = 50 \mathrm{~pF}$; POD[1] = medium
Rise time	t_{RA1} CC	–		150	ns	$C_{\mathrm{L}} = 20 \mathrm{~pF}$; POD[1] = weak
		–		50	ns	$C_{\mathrm{L}} = 50 \mathrm{~pF}$; POD[1] = medium

[1] POD = Pin Out Driver

Table 21 Standard Pads Class_A1+

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	$I_{\mathrm{OZA1+}}$ CC	-1		1	µA	$0 \mathrm{~V} \le V_{\mathrm{IN}} \le V_{\mathrm{DDP}}$
Input high voltage	$V_{\mathrm{IHA1+}}$ SR	$0.6 \times V_{\mathrm{DDP}}$		$V_{\mathrm{DDP}} + 0.3$	V	max. 3.6 V
Input low voltage	$V_{\mathrm{ILA1+}}$ SR	-0.3		$0.36 \times V_{\mathrm{DDP}}$	V	

Table 23 HIB_IO Class_A1 special Pads

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.		Max.		
Input leakage current	I_{OZHIB} CC	-500		500	nA	$0 V \leq V_{IN} \leq V_{BAT}$
Input high voltage	V_{IHHIB} SR	$0.6 \times V_{BAT}$		$V_{BAT} + 0.3$	V	max. 3.6 V
Input low voltage	V_{ILHIB} SR	-0.3		$0.36 \times V_{BAT}$	V	
Input Hysteresis for HIB_IO pins[1]	$HYSHIB$ CC	$0.1 \times V_{BAT}$		–	V	$V_{BAT} \geq 3.13$ V
		$0.06 \times V_{BAT}$		–	V	$V_{BAT} < 3.13$ V
Output high voltage, POD[1] = medium	V_{OHHIB} CC	V_{BAT} - 0.4		–	V	$I_{OH} \geq -1.4$ mA
Output low voltage	V_{OLHIB} CC	–		0.4	V	$I_{OL} \leq 2$ mA
Fall time	t_{FHIB} CC	–		50	ns	$V_{BAT} \geq 3.13$ V $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V $C_L = 50$ pF
Rise time	t_{RHIB} CC	–		50	ns	$V_{BAT} \geq 3.13$ V $C_L = 50$ pF
		–		100	ns	$V_{BAT} < 3.13$ V $C_L = 50$ pF

[1] Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It can not be guaranteed that it suppresses switching due to external system noise.

3.2.2 Analog to Digital Converters (VADC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 24 VADC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	**Typ.**	**Max.**		
Analog reference voltage[5]	V_{AREF} SR	$V_{\text{AGND}} + 1$	–	$V_{\text{DDA}} + 0.05$[1]	V	
Analog reference ground[5]	V_{AGND} SR	$V_{\text{SSM}} - 0.05$	–	$V_{\text{AREF}} - 1$	V	
Analog reference voltage range[2][5]	$V_{\text{AREF}} - V_{\text{AGND}}$ SR	1	–	$V_{\text{DDA}} + 0.1$	V	
Analog input voltage	V_{AIN} SR	V_{AGND}	–	V_{DDA}	V	
Input leakage at analog inputs[3]	I_{OZ1} CC	-100	–	200	nA	$0.03 \times V_{\text{DDA}} < V_{\text{AIN}} < 0.97 \times V_{\text{DDA}}$
		-500	–	100	nA	$0\text{ V} \leq V_{\text{AIN}} \leq 0.03 \times V_{\text{DDA}}$
		-100	–	500	nA	$0.97 \times V_{\text{DDA}} \leq V_{\text{AIN}} \leq V_{\text{DDA}}$
Input leakage current at VAREF	I_{OZ2} CC	-1	–	1	µA	$0\text{ V} \leq V_{\text{AREF}} \leq V_{\text{DDA}}$
Input leakage current at VAGND	I_{OZ3} CC	-1	–	1	µA	$0\text{ V} \leq V_{\text{AGND}} \leq V_{\text{DDA}}$
Internal ADC clock	f_{ADCI} CC	2	–	36	MHz	$V_{\text{DDA}} = 3.3\text{ V}$
Switched capacitance at the analog voltage inputs[4]	C_{AINSW} CC	–	4	6.5	pF	
Total capacitance of an analog input	C_{AINTOT} CC	–	12	20	pF	
Switched capacitance at the positive reference voltage input[5][6]	C_{AREFSW} CC	–	15	30	pF	
Total capacitance of the voltage reference inputs[5]	C_{AREFTOT} CC	–	20	40	pF	

3.2.3 Digital to Analog Converters (DAC)

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 26 DAC Parameters (Operating Conditions apply)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RMS supply current	I_{DD} CC	–	2.5	4	mA	per active DAC channel, without load currents of DAC outputs
Resolution	RES CC	–	12	–	Bit	
Update rate	f_{URATE_A}CC	–		2	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 1LSB accuracy
Update rate	f_{URATE_F} CC	–		5	Msample/s	data rate, where DAC can follow 64 LSB code jumps to ± 4 LSB accuracy
Settling time	t_{SETTLE} CC	–	1	2	µs	at full scale jump, output voltage reaches target value ± 20 LSB
Slew rate	SR CC	2	5	–	V/µs	
Minimum output voltage	V_{OUT_MIN} CC	–	0.3	–	V	code value unsigned: 000_H; signed: 800_H
Maximum output voltage	V_{OUT_MAX} CC	–	2.5	–	V	code value unsigned: FFF_H; signed: $7FF_H$
Integral non-linearity	INL CC	-5.5	±2.5	5.5	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF
Differential non-linearity	DNL CC	-2	±1	2	LSB	$R_L \geq 5$ kOhm, $C_L \leq 50$ pF

Table 26 DAC Parameters (Operating Conditions apply) (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Offset error	ED_{OFF} CC		±20		mV	
Gain error	$ED_{\mathrm{G\_IN}}$ CC	-6.5	-1.5	3	%	
Startup time	t_{STARTUP} CC	–	15	30	µs	time from output enabling till code valid ±16 LSB
3dB Bandwidth of Output Buffer	f_{C1} CC	2.5	5	–	MHz	verified by design
Output sourcing current	$I_{\mathrm{OUT\_SOURCE}}$ CC	–	-30	–	mA	
Output sinking current	$I_{\mathrm{OUT\_SINK}}$ CC	–	0.6	–	mA	
Output resistance	R_{OUT} CC	–	50	–	Ohm	
Load resistance	R_{L} SR	5	–	–	kOhm	
Load capacitance	C_{L} SR	–	–	50	pF	
Signal-to-Noise Ratio	*SNR* CC	–	70	–	dB	examination bandwidth < 25 kHz
Total Harmonic Distortion	*THD* CC	–	70	–	dB	examination bandwidth < 25 kHz
Power Supply Rejection Ratio	*PSRR* CC	–	56	–	dB	to V_{DDA} verified by design

Conversion Calculation

Unsigned:
DACxDATA = $4095 \times (V_{\mathrm{OUT}} - V_{\mathrm{OUT\_MIN}}) / (V_{\mathrm{OUT\_MAX}} - V_{\mathrm{OUT\_MIN}})$

Signed:
DACxDATA = $4095 \times (V_{\mathrm{OUT}} - V_{\mathrm{OUT\_MIN}}) / (V_{\mathrm{OUT\_MAX}} - V_{\mathrm{OUT\_MIN}}) - 2048$

3.3.8 Peripheral Timing

3.3.8.1 Synchronous Serial Interface (USIC SSC) Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test, but verified by design and/or characterization.

Table 43 USIC SSC Master Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SCLKOUT master clock period	t_{CLK} CC	33.3	–	–	ns	
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{PB} - 6.5[1]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{PB} - 8.5[1]	–	–	ns	
Data output DOUT[3:0] valid time	t_3 CC	-6	–	8	ns	
Receive data input DX0/DX[5:3] setup time to SCLKOUT receive edge	t_4 SR	23	–	–	ns	
Data input DX0/DX[5:3] hold time from SCLKOUT receive edge	t_5 SR	1	–	–	ns	

[1] $t_{PB} = 1 / f_{PB}$

Table 44 USIC SSC Slave Mode Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
DX1 slave clock period	t_{CLK} SR	66.6	–	–	ns	
Select input DX2 setup to first clock input DX1 transmit edge[1]	t_{10} SR	3	–	–	ns	

Table 44 USIC SSC Slave Mode Timing

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
Select input DX2 hold after last clock input DX1 receive edge¹⁾	t_{11}	SR	4	–	–	ns	
Receive data input DX0/DX[5:3] setup time to shift clock receive edge¹⁾	t_{12}	SR	6	–	–	ns	
Data input DX0/DX[5:3] hold time from clock input DX1 receive edge¹⁾	t_{13}	SR	4	–	–	ns	
Data output DOUT[3:0] valid time	t_{14}	CC	0	–	24	ns	

1) This input timing is valid for asynchronous input signal handling of slave select input, shift clock input, and receive data input (bits DXnCR.DSEN = 0).

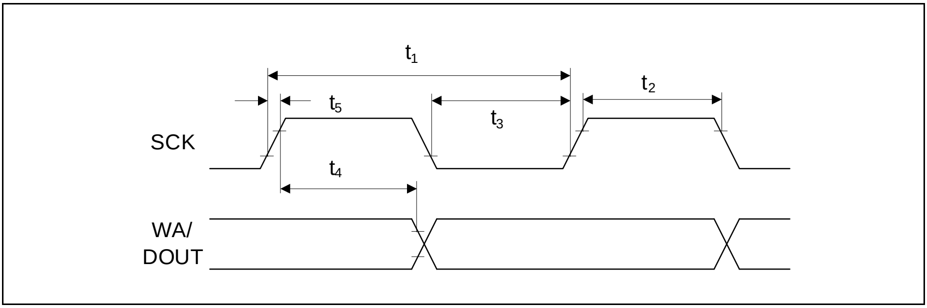


Figure 28 USIC IIS Master Transmitter Timing

Table 48 USIC IIS Slave Receiver Timing

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Clock period	t_6 SR	66.6	–	–	ns	
Clock high time	t_7 SR	0.35 x $t_{6\mathrm{min}}$	–	–	ns	
Clock low time	t_8 SR	0.35 x $t_{6\mathrm{min}}$	–	–	ns	
Set-up time	t_9 SR	0.2 x $t_{6\mathrm{min}}$	–	–	ns	
Hold time	t_{10} SR	0	–	–	ns	

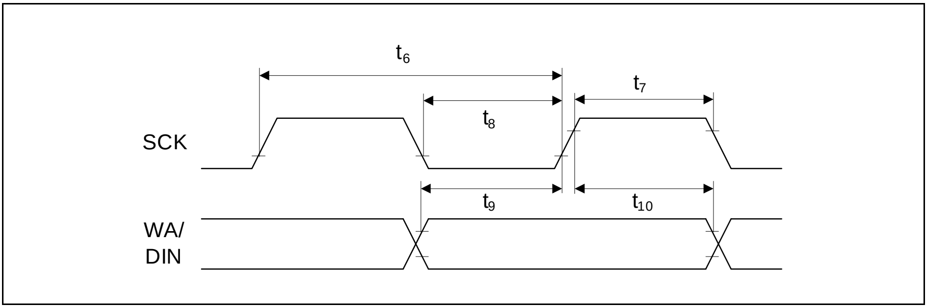


Figure 29 USIC IIS Slave Receiver Timing

No clock delay:

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} \tag{7}$$

With clock delay:

$$t_{ODLY\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ISU} < t_{WL} + t_{CLK\_DELAY} \tag{8}$$

$$t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{CLK\_DELAY} < t_{WL} - t_{ISU} - t_{ODLY\_H} \tag{9}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < t_{WL} - t_{ISU} - t_{ODLY\_H} - t_{TAP\_DELAY}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < 10 - 6 - 14 - t_{TAP\_DELAY}$$

$$t_{DATA\_DELAY} - t_{CLK\_DELAY} < -10 - t_{TAP\_DELAY}$$

The data delay is less than the clock delay by at least 10 ns in the ideal case where t_{WL}= 10 ns.

High-Speed Write Meeting Hold (Minimum Delay)

The following equations show how to calculate the allowed skew range between the SD_CLK and SD_DAT/CMD signals on the PCB.

$$t_{CLK\_DELAY} < t_{WL} + t_{OH\_H} + t_{DATA\_DELAY} + t_{TAP\_DELAY} - t_{IH} \tag{10}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < t_{WL} + t_{OH\_H} + t_{TAP\_DELAY} - t_{IH}$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + 2 + t_{TAP\_DELAY} - 2$$

$$t_{CLK\_DELAY} - t_{DATA\_DELAY} < 10 + t_{TAP\_DELAY}$$

The clock can be delayed versus data up to 13.2 ns (external delay line) in ideal case of t_{WL}= 10 ns, with maximum t_{TAP_DELAY} = 3.2 ns programmed.

High-Speed Input Path (Read)

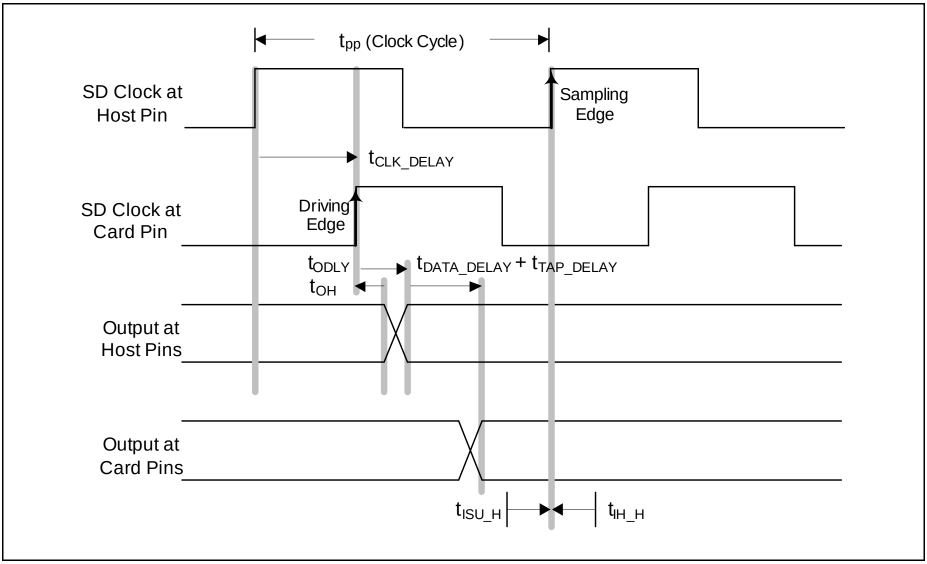


Figure 33 High-Speed Input Path

High-Speed Read Meeting Setup (Maximum Delay)

The following equations show how to calculate the allowed combined propagation delay range of the SD_CLK and SD_DAT/CMD signals on the PCB.

(11)

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} + t_{TAP\_DELAY} + t_{ODLY} + t_{ISU\_H} < t_{pp}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < t_{pp} - t_{ODLY} - t_{ISU\_H} - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 20 - 14 - 2 - t_{TAP\_DELAY}$$

$$t_{CLK\_DELAY} + t_{DATA\_DELAY} < 4 - t_{TAP\_DELAY}$$

The data + clock delay can be up to 4 ns for a 20 ns clock cycle.

3.3.10.3 ETH RMII Parameters

In the following, the parameters of the RMII (Reduced Media Independent Interface) are described.

Table 55 ETH RMII Signal Timing Parameters

Parameter	Symbol		Values			Unit	Note / Test Condition
			Min.	Typ.	Max.		
ETH_RMII_REF_CL clock period	t_{13}	SR	20	–	–	ns	C_L = 25 pF; 50 ppm
ETH_RMII_REF_CL clock high time	t_{14}	SR	7	–	13	ns	C_L = 25 pF
ETH_RMII_REF_CL clock low time	t_{15}	SR	7	–	13	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS setup time	t_{16}	SR	4	–	–	ns	
ETH_RMII_RXD[1:0], ETH_RMII_CRS hold time	t_{17}	SR	2	–	–	ns	
ETH_RMII_TXD[1:0], ETH_RMII_TXEN data valid	t_{18}	CC	4	–	15	ns	

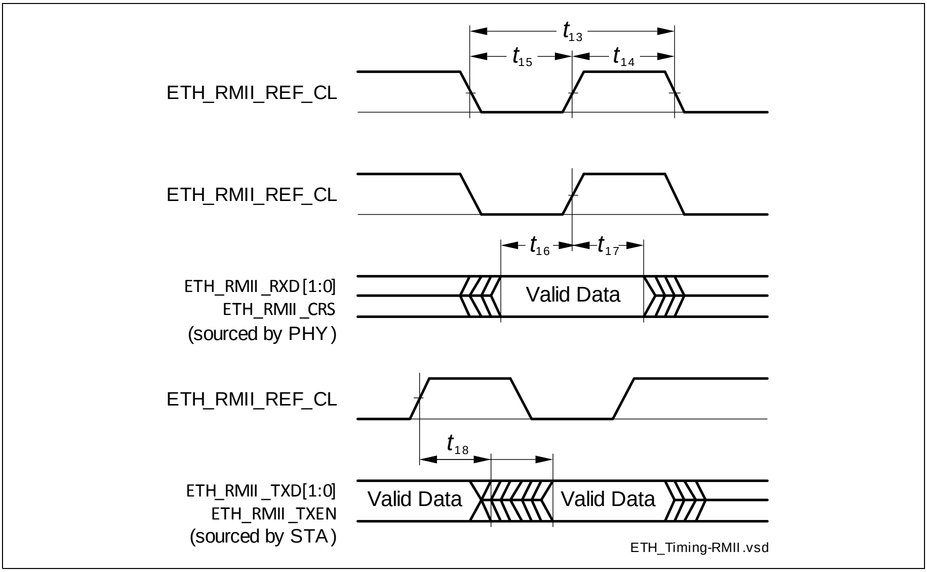


Figure 37 ETH RMII Signal Timing

3.3.11.4 MII Timing RX Characteristics

Table 58 ETH MII RX Signal Timing Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
RX_CLK period	t_{RX_CLK} SR	–	40	–	ns	C_L = 25 pF, IEEE802.3 requirement
RX_DV/RX_DV/RXD[3:0] valid before rising edge of RX_CLK	t_{RX_setup} SR	10	–	–	ns	
RX_DV/RX_DV/RXD[3:0] valid after rising edge of RX_CLK	t_{RX_hold} SR	10	–	–	ns	

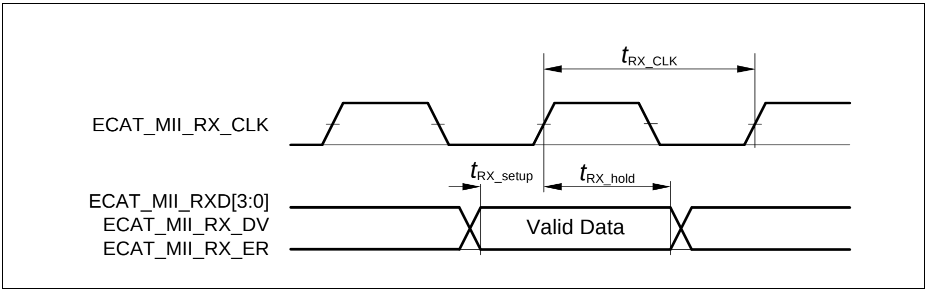


Figure 41 MII RX characteristics

4.2 Package Outlines

The exposed die pad dimensions are listed in **Table 60**.

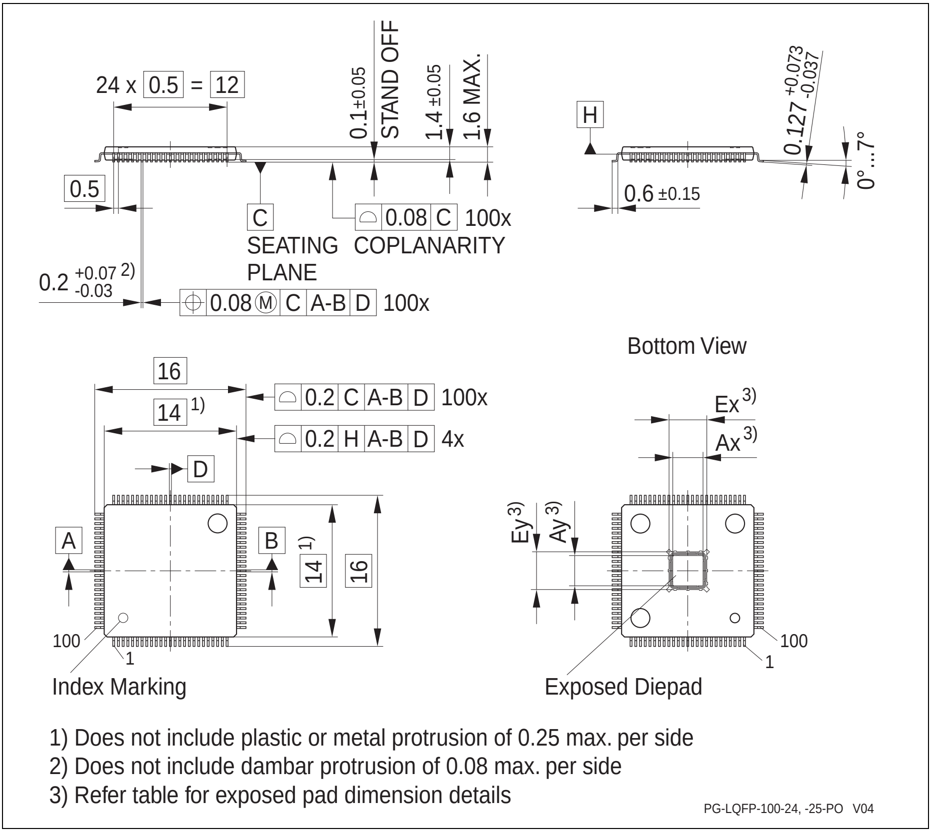


Figure 43 **PG-LQFP-100-25** (Plastic Green Low Profile Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page “Packages”: **http://www.infineon.com/packages**