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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

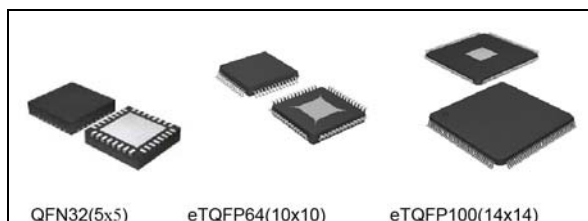
### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	e200z2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I <sup>2</sup> C, LINbus, SPI
Peripherals	DMA, WDT
Number of I/O	48
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	3.3V, 5V
Data Converters	A/D 27x12b SAR
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP Exposed Pad
Supplier Device Package	64-eTQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/spc582b60e1mh00y">https://www.e-xfl.com/product-detail/stmicroelectronics/spc582b60e1mh00y</a>

## A scalable approach to your body, networking and security platforms

Data brief



### Features

- Package availability ranges from QFN32 up to the eTQFP100
- Core: single z2d core up to 80 MHz
- Code: 512 Kbytes to 1 Mbytes Flash
- Data: 64 kbytes data Flash
- RAM: up to 96 kbytes RAM
- Timer: 32ch, 16-bit counter timed I/O
- ADC: 32ch 1x 12-bit
- Networking: Up to 6xLIN, 7 x ISO CAN FD
- Low Power: HALT, STOP and STBY Smart Standby Unit
- Safety: ASIL-B, CRC unit, FCCU
- Other: MPU, eDMA, 4xSPI, I2C, Cross Triggering Unit, PIT, RTC/API, STM
- Package: QFN32, 2TQFP64, eTQFP100
- Supply: 5V or 3.3V with internal regulator
- Temperature: -40°C / +105°C or +125°C

### Description

The SPC58 2B-Line constitutes a general-purpose MCU family targeting Body, Networking and Security applications. Built on the legacy of successful 90nm products, SPC56xB/C/D, this new product generation in 40nm offers the widest range of compatible devices from 512k up to 6M bytes Flash combined with the latest communication interfaces like ISO CAN FD and Ethernet with AVB capability.

Designed according to ISO 26262, the SPC58 B/C/G-Lines family supports ASIL-B (optional ASIL-D) as well as a high Security level according to EVITA medium.

The SPC58 2B-Line offers a high integrated, high performance devices available in high-efficiency pin count packages like eTQFP100 featuring an e200z2 core with seven ISO CAN FD. The 2B-Line is fully scalable and compatible up to eLQFP100. The 40nm technology allows to further reduce the power consumption in RUN mode, while the advanced low power modes manage even complex contact monitoring sequences in STANDBY mode and without CPU intervention.

**Table 1. Device summary**

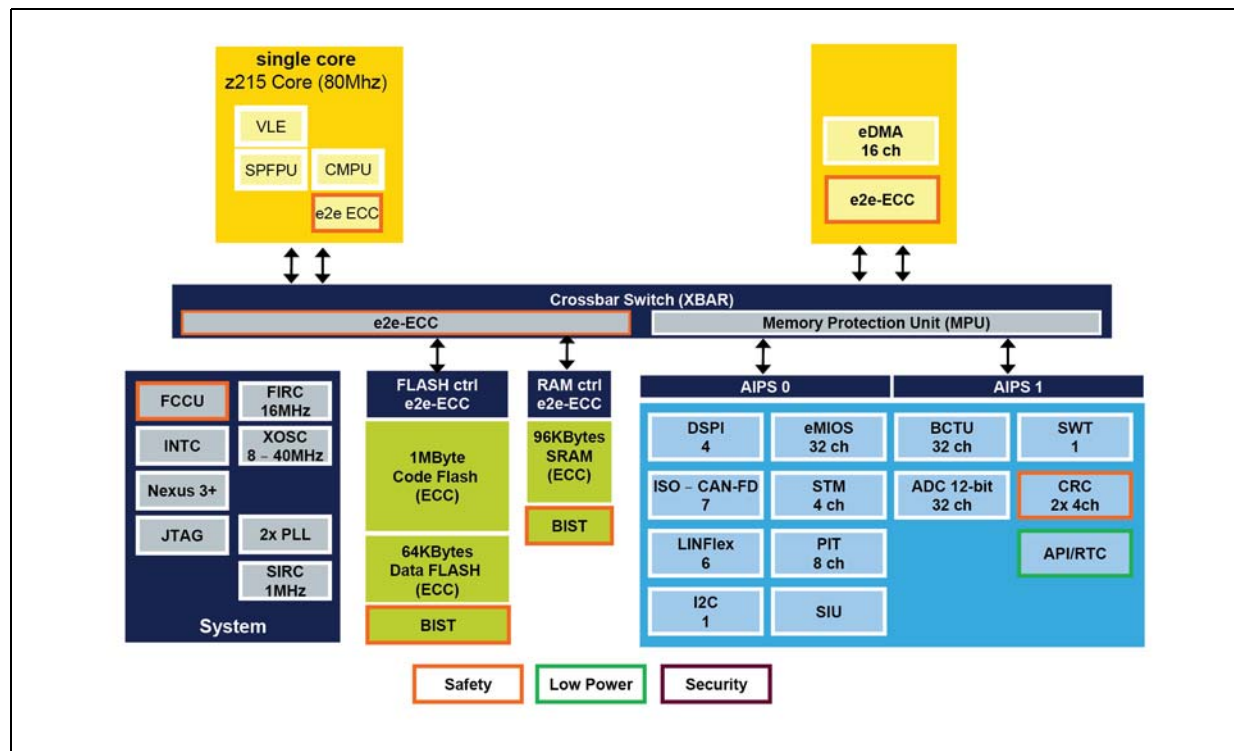
Part number			Package	References
512 KByte	768 KByte	1 mByte		
SPC582B50Q2	SPC582B54Q2	SPC582B60Q2	QFN32	SPC582BXX
SPC582B50E1	SPC582B54E1	SPC582B60E1	eTQFP64	
SPC582B50E3	SPC582B54E3	SPC582B60E3	eTQFP100	

# 1 Overview

## 1.1 Block diagram

Functional blocks diagram of SPC58 2B-Line MCU.

Figure 1. Block diagram



## 2 Software library

The product family is provided with a set of software libraries downloadable by ST web, registration is required, to facilitate application development.

- The offer includes:
- Flash drivers for run-time and off-line device programming
- MCAL developed and distributed by ST
- Core Self Test
- Safety adapted MCAL
- RTOS/Kernel RTOS from ETAS, Vector and Green Hills products
- AS BSW from Vector Informatik GmbH

### 2.1 Tools

A set of ST and third parties tools are available to explore the product family starting from budgetary cost evaluation boards to top class solutions.

**Figure 2. Third parties tools**



### 3 Revision history

**Table 2. Document revision history**

Date	Revision	Changes
06-Mar-2017	1	Initial release.

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