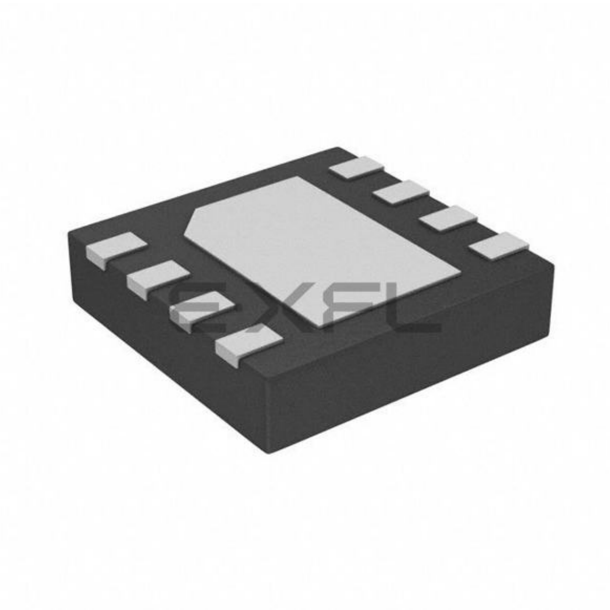

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12f1612-e-mf

TABLE 1: PIC12/16(L)F161X FAMILY TYPES

Device	Data Sheet Index	Program Memory Flash (W)	Program Memory Flash (kB)	Data SRAM (bytes)	High Endurance Flash (bytes)	I/O Pins	8-bit Timer with HLT	16-bit Timer	Angular Timer	Windowed Watchdog Timer	24-bit SMT	Comparators	10-bit ADC (ch)	Zero-Cross Detect	CCP/10-bit PWM	CWG	CLC	CRC with Memory Scan	Math Accelerator with PID	High-Current I/O 100mA	PPS	EUSART	I^2C/SPI
PIC12(L)F1612	**(A)**	2048	3.5	256	128	6	4	1	0	Y	1	1	4	1	2/0	1	0	Y	0	0	N	0	0
PIC16(L)F1613	**(A)**	2048	3.5	256	128	12	4	1	0	Y	2	2	8	1	2/0	1	0	Y	0	0	N	0	0
PIC16(L)F1614	**(B)**	4096	7	512	128	12	4	3	1	Y	2	2	8	1	2/2	1	2	Y	1	2	Y	1	1
PIC16(L)F1615	**(C)**	8192	14	1024	128	12	4	3	1	Y	2	2	8	1	2/2	1	4	Y	1	2	Y	1	1
PIC16(L)F1618	**(B)**	4096	7	512	128	18	4	3	1	Y	2	2	12	1	2/2	1	2	Y	1	2	Y	1	1
PIC16(L)F1619	**(C)**	8192	14	1024	128	18	4	3	1	Y	2	2	12	1	2/2	1	4	Y	1	2	Y	1	1

Note 1: Debugging Methods: (I) – Integrated on Chip; (H) – via ICD Header; E – using Emulation Product

Data Sheet Index:

- **A.** DS40001737 PIC12(L)F1612/16(L)F1613 Data Sheet, 8/14-Pin, 8-bit Flash Microcontrollers
- **B.** DS40001769 PIC16(L)F1614/8 Data Sheet, 14/20-Pin, 8-bit Flash Microcontrollers
- **C.** DS40001770 PIC16(L)F1615/9 Data Sheet, 14/20-Pin, 8-bit Flash Microcontrollers

Note:	For other small form-factor package availability and marking information, please visit **http://www.microchip.com/packaging** or contact your local sales office.

TABLE 3-4: PIC12(L)F1612/16(L)F1613 MEMORY MAP, BANK 8-23

	BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15
400h–40Bh	Core Registers (Table 3-1)	480h–48Bh	Core Registers (Table 3-1)	500h–50Bh	Core Registers (Table 3-1)	580h–58Bh	Core Registers (Table 3-1)	600h–60Bh	Core Registers (Table 3-1)	680h–68Bh	Core Registers (Table 3-1)	700h–70Bh	Core Registers (Table 3-1)	780h–78Bh	Core Registers (Table 3-1)
40Ch	—	48Ch	—	50Ch	—	58Ch	—	60Ch	—	68Ch	—	70Ch	—	78Ch	—
40Dh	—	48Dh	—	50Dh	—	58Dh	—	60Dh	—	68Dh	—	70Dh	—	78Dh	—
40Eh	—	48Eh	—	50Eh	—	58Eh	—	60Eh	—	68Eh	—	70Eh	—	78Eh	—
40Fh	—	48Fh	—	50Fh	—	58Fh	—	60Fh	—	68Fh	—	70Fh	—	78Fh	—
410h	—	490h	—	510h	—	590h	—	610h	—	690h	—	710h	—	790h	—
411h	—	491h	—	511h	—	591h	—	611h	—	691h	CWG1DBR	711h	WDTCON0	791h	CRCDATL
412h	—	492h	—	512h	—	592h	—	612h	—	692h	CWG1DBF	712h	WDTCON1	792h	CRCDATH
413h	TMR4	493h	—	513h	—	593h	—	613h	—	693h	CWG1AS0	713h	WDTPSL	793h	CRCACCL
414h	PR4	494h	—	514h	—	594h	—	614h	—	694h	CWG1AS1	714h	WDTPSH	794h	CRCACCH
415h	T4CON	495h	—	515h	—	595h	—	615h	—	695h	CWG1OCON0	715h	WDTTMR	795h	CRCSHIFTL
416h	T4HLT	496h	—	516h	—	596h	—	616h	—	696h	CWG1CON0	716h	—	796h	CRCSHIFTH
417h	T4CLKCON	497h	—	517h	—	597h	—	617h	—	697h	CWG1CON1	717h	—	797h	CRCXORL
418h	T4RST	498h	—	518h	—	598h	—	618h	—	698h	CWG1OCON1	718h	SCANLADRL	798h	CRCXORH
419h	—	499h	—	519h	—	599h	—	619h	—	699h	CWG1CLKCON	719h	SCANLADRH	799h	CRCCON0
41Ah	TMR6	49Ah	—	51Ah	—	59Ah	—	61Ah	—	69Ah	CWG1ISM	71Ah	SCANHADRL	79Ah	CRCCON1
41Bh	PR6	49Bh	—	51Bh	—	59Bh	—	61Bh	—	69Bh	—	71Bh	SCANHADRH	79Bh	—
41Ch	T6CON	49Ch	—	51Ch	—	59Ch	—	61Ch	—	69Ch	—	71Ch	SCANCON0	79Ch	—
41Dh	T6HLT	49Dh	—	51Dh	—	59Dh	—	61Dh	—	69Dh	—	71Dh	SCANTRIG	79Dh	—
41Eh	T6CLKCON	49Eh	—	51Eh	—	59Eh	—	61Eh	—	69Eh	—	71Eh	—	79Eh	—
41Fh	T6RST	49Fh	—	51Fh	—	59Fh	—	61Fh	—	69Fh	—	71Fh	—	79Fh	—
420h–46Fh	Unimplemented Read as ‘0’	4A0h–4EFh	Unimplemented Read as ‘0’	520h–56Fh	Unimplemented Read as ‘0’	5A0h–5EFh	Unimplemented Read as ‘0’	620h–66Fh	Unimplemented Read as ‘0’	6A0h–6EFh	Unimplemented Read as ‘0’	720h–76Fh	Unimplemented Read as ‘0’	7A0h–7EFh	Unimplemented Read as ‘0’
470h–47Fh	Accesses 70h – 7Fh	4F0h–4FFh	Accesses 70h – 7Fh	570h–57Fh	Accesses 70h – 7Fh	5F0h–5FFh	Accesses 70h – 7Fh	670h–67Fh	Accesses 70h – 7Fh	6F0h–6FFh	Accesses 70h – 7Fh	770h–77Fh	Accesses 70h – 7Fh	7F0h–7FFh	Accesses 70h – 7Fh

	BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23
800h–80Bh	Core Registers (Table 3-1)	880h–88Bh	Core Registers (Table 3-1)	900h–90Bh	Core Registers (Table 3-1)	980h–98Bh	Core Registers (Table 3-1)	A00h–A0Bh	Core Registers (Table 3-1)	A80h–A8Bh	Core Registers (Table 3-1)	B00h–B0Bh	Core Registers (Table 3-1)	B80h–B8Bh	Core Registers (Table 3-1)
80Ch–86Fh	Unimplemented Read as ‘0’	88Ch–8EFh	Unimplemented Read as ‘0’	90Ch–96Fh	Unimplemented Read as ‘0’	98Ch–9EFh	Unimplemented Read as ‘0’	A0Ch–A6Fh	Unimplemented Read as ‘0’	A8Ch–AEFh	Unimplemented Read as ‘0’	B0Ch–B6Fh	Unimplemented Read as ‘0’	B8Ch–BEFh	Unimplemented Read as ‘0’
870h–87Fh	Accesses 70h – 7Fh	8F0h–8FFh	Accesses 70h – 7Fh	970h–97Fh	Accesses 70h – 7Fh	9F0h–9FFh	Accesses 70h – 7Fh	A70h–A7Fh	Accesses 70h – 7Fh	AF0h–AFFh	Accesses 70h – 7Fh	B70h–B7Fh	Accesses 70h – 7Fh	BF0h–BFFh	Accesses 70h – 7Fh

Legend: (shaded) = Unimplemented data memory locations, read as ‘0’.

TABLE 3-9: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 29-30											
x0Ch/ x8Ch — x1Fh/ x9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as ‘0’.

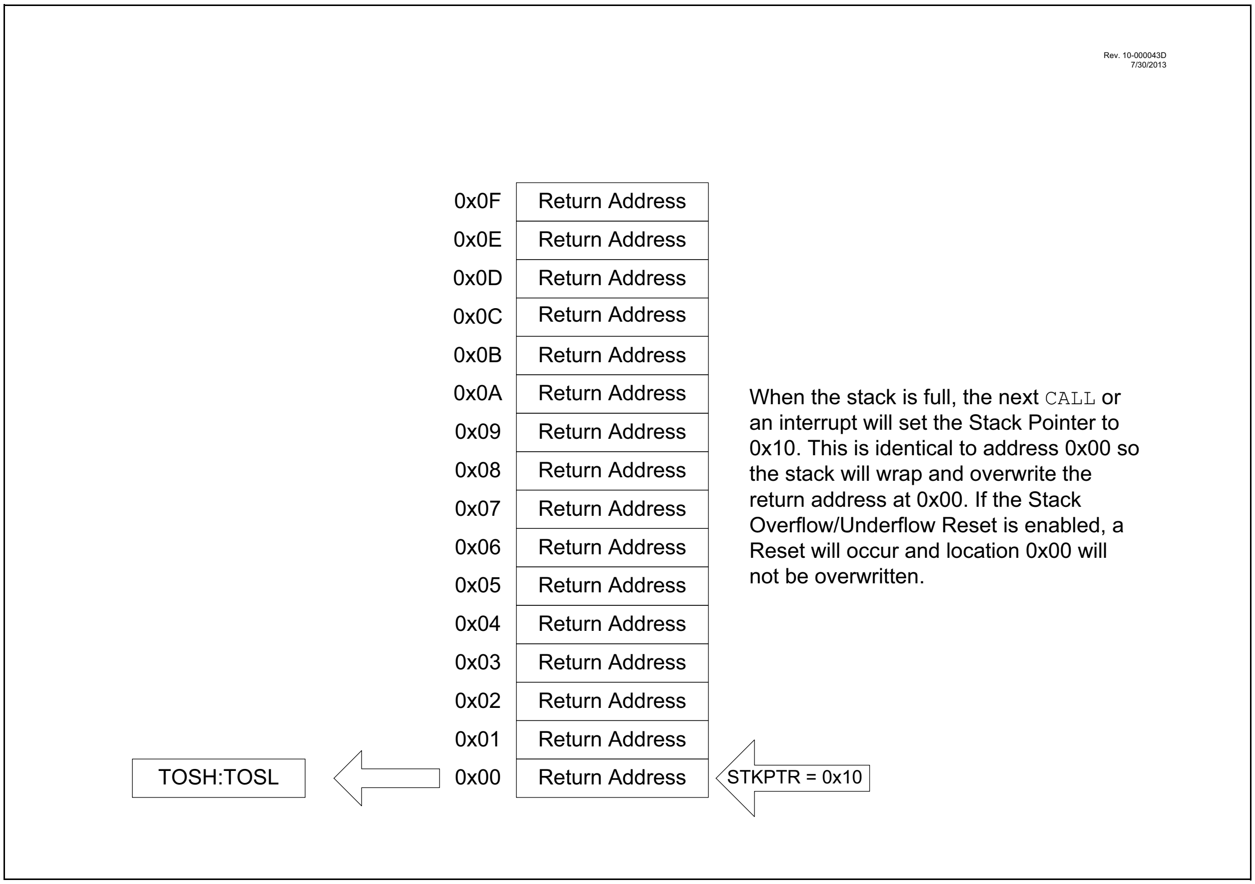
Note 1: PIC12F1612/16F1613 only.

2: Unimplemented, read as ‘1’.

3: PIC12(L)F1612 only.

4: PIC16(L)F1613 only.

FIGURE 3-7: ACCESSING THE STACK EXAMPLE 4



3.5.2 OVERFLOW/UNDERFLOW RESET

If the STVREN bit in Configuration Words is programmed to '1', the device will be reset if the stack is PUSHed beyond the sixteenth level or POPed beyond the first level, setting the appropriate bits (STKOVF or STKUNF, respectively) in the PCON register.

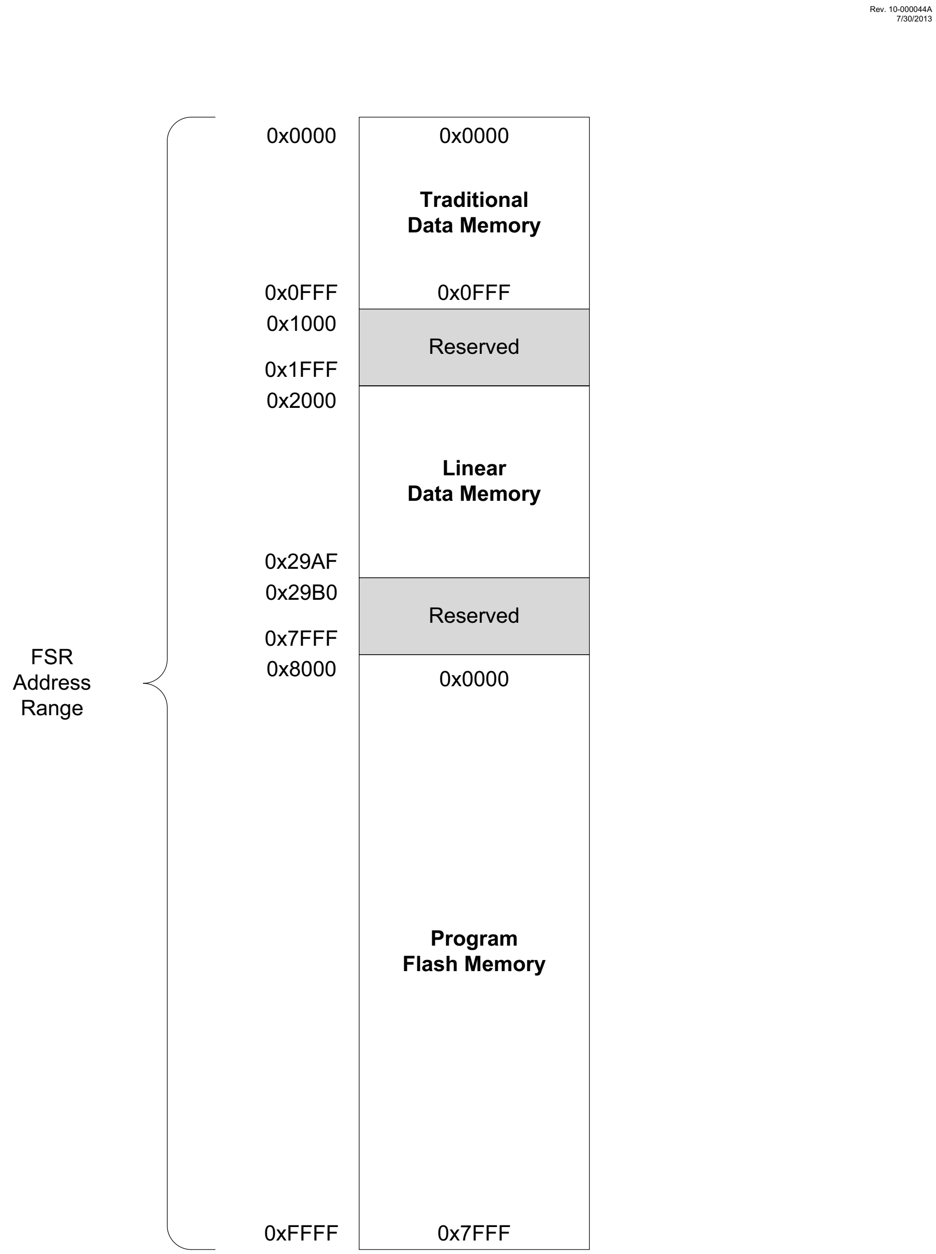
3.6 Indirect Addressing

The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the File Select Registers (FSR). If the FSRn address specifies one of the two INDFn registers, the read will return '0' and the write will not occur (though Status bits may be affected). The FSRn register value is created by the pair FSRnH and FSRnL.

The FSR registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory

FIGURE 3-8: INDIRECT ADDRESSING



Note: Not all memory regions are completely implemented. Consult device memory tables for memory limits.

5.2.2 INTERNAL CLOCK SOURCES

The device may be configured to use the internal oscillator block as the system clock by performing one of the following actions:

- Program the FOSC<1:0> bits in Configuration Words to select the INTOSC clock source, which will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to the internal oscillator during run-time. See **Section5.3 “Clock Switching”**for more information.

In **INTOSC** mode, CLKIN is available for general purpose I/O. CLKOUT is available for general purpose I/O or CLKOUT.

The function of the OSC2/CLKOUT pin is determined by the $\overline{\text{CLKOUTEN}}$ bit in Configuration Words.

The internal oscillator block has two independent oscillators and a dedicated Phase Lock Loop, HFPLL that can produce one of three internal system clock sources.

1. The **HFINTOSC** (High-Frequency Internal Oscillator) is factory calibrated and operates at 16 MHz. The HFINTOSC source is generated from the 500 kHz MFINTOSC source and the dedicated Phase Lock Loop, HFPLL. The frequency of the HFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
2. The **MFINTOSC** (Medium-Frequency Internal Oscillator) is factory calibrated and operates at 500 kHz. The frequency of the MFINTOSC can be user-adjusted via software using the OSCTUNE register (Register 5-3).
3. The **LFINTOSC** (Low-Frequency Internal Oscillator) is uncalibrated and operates at 31 kHz.

5.2.2.1 HFINTOSC

The High-Frequency Internal Oscillator (HFINTOSC) is a factory calibrated 16 MHz internal clock source. The frequency of the HFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the HFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of multiple frequencies derived from the HFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section5.2.2.8 “Internal Oscillator Clock Switch Timing”** for more information.

The HFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<1:0> = `00`, or
- Set the System Clock Source (SCS) bits of the OSCCON register to ‘`1x`’.

A fast start-up oscillator allows internal circuits to power up and stabilize before switching to HFINTOSC.

The High-Frequency Internal Oscillator Ready bit (HFIOFR) of the OSCSTAT register indicates when the HFINTOSC is running.

The High-Frequency Internal Oscillator Status Locked bit (HFIOFL) of the OSCSTAT register indicates when the HFINTOSC is running within 2% of its final value.

The High-Frequency Internal Oscillator Stable bit (HFIOFS) of the OSCSTAT register indicates when the HFINTOSC is running within 0.5% of its final value.

5.2.2.2 MFINTOSC

The Medium-Frequency Internal Oscillator (MFINTOSC) is a factory calibrated 500 kHz internal clock source. The frequency of the MFINTOSC can be altered via software using the OSCTUNE register (Register 5-3).

The output of the MFINTOSC connects to a postscaler and multiplexer (see Figure 5-1). One of nine frequencies derived from the MFINTOSC can be selected via software using the IRCF<3:0> bits of the OSCCON register. See **Section5.2.2.8 “Internal Oscillator Clock Switch Timing”** for more information.

The MFINTOSC is enabled by:

- Configure the IRCF<3:0> bits of the OSCCON register for the desired HF frequency, and
- FOSC<1:0> = `00`, or
- Set the System Clock Source (SCS) bits of the OSCCON register to ‘`1x`’

The Medium-Frequency Internal Oscillator Ready bit (MFIOFR) of the OSCSTAT register indicates when the MFINTOSC is running.

REGISTER 10-6: PMCON2: PROGRAM MEMORY CONTROL 2 REGISTER

W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0	W-0/0
Program Memory Control Register 2							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
S = Bit can only be set	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **Flash Memory Unlock Pattern bits**
To unlock writes, a 55h must be written first, followed by an AAh, before setting the WR bit of the PMCON1 register. The value written to this register is used to unlock the writes. There are specific timing requirements on these writes.

TABLE 10-3: SUMMARY OF REGISTERS ASSOCIATED WITH FLASH PROGRAM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	82
PMCON1	—(1)	CFGS	LWLO	FREE	WRERR	WREN	WR	RD	117
PMCON2	Program Memory Control Register 2								118
PMADRL	PMADRL<7:0>								116
PMADRH	—(1)	PMADRH<6:0>							116
PMDATL	PMDATL<7:0>								116
PMDATH	—	—	PMDATH<5:0>						116

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by Flash program memory.
Note 1: Unimplemented, read as ‘1’.

TABLE 10-4: SUMMARY OF CONFIGURATION WORD WITH FLASH PROGRAM MEMORY

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	—	—	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—	52
	7:0	$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	—	—	—	FOSC<1:0>		
CONFIG2	13:8	—	—	LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	PLLEN	53
	7:0	$\overline{\text{ZCD}}$	—	—	—	—	—	WRT<1:0>		
CONFIG3	13:8	—	—	WDTCCS<2:0>			WDTCWS<2:0>			53
	7:0	—	WDTE<1:0>		WDTCPS<4:0>					

Legend: — = unimplemented location, read as ‘0’. Shaded cells are not used by Flash program memory.

REGISTER 12-14: WPUC: WEAK PULL-UP PORTC REGISTER(1),(2)

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **WPUC<5:0>**: Weak Pull-up Register bits
1 = Pull-up enabled
0 = Pull-up disabled

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 12-15: ODCONC: PORTC OPEN-DRAIN CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **ODC<5:0>:** PORTC Open Drain Enable bits
For RC<5:0> pins, respectively
1 = Port pin operates as open-drain drive (sink current only)
0 = Port pin operates as standard push-pull drive (source and sink current)

13.0 INTERRUPT-ON-CHANGE

The PORTA and PORTC pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

13.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

13.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

13.3 Interrupt Flags

The IOCAFx and IOCCFx bits located in the IOCAF and IOCCF registers, respectively, are status flags that correspond to the interrupt-on-change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAFx and IOCCFx bits.

13.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx and IOCCFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 13-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW   0xff
XORWF   IOCAF, W
ANDWF   IOCAF, F
```

13.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.

TABLE 18-3: SUMMARY OF REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	136
CM1CON0	C1ON	C1OUT	C1OE	C1POL	—	C1SP	C1HYS	C1SYNC	179
CM1CON1	C1INTP	C1INTN	C1PCH<1:0>		—	C1NCH<2:0>			180
CM2CON0(2)	C2ON	C2OUT	C2OE	C2POL	—	C2SP	C2HYS	C2SYNC	179
CM2CON1(2)	C2INTP	C2INTN	C2PCH<1:0>		—	C2NCH<2:0>			180
CMOUT	—	—	—	—	—	—	MC2OUT(2)	MC1OUT	180
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		153
DAC1CON0	DAC1EN	—	DAC1OE1	—	DAC1PSS<1:0>		—	—	173
DAC1CON1	DAC1R<7:0>								173
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	82
PIE2	OSFIE	C2IE	C1IE	—	BCL1IE	TMR6IE	TMR4IE	CCP2IE	84
PIR2	OSFIF	C2IF	C1IF	—	BCL1IF	TMR6IF	TMR4IF	CCP2IF	88
TRISA	—	—	TRISA5	TRISA4	—(1)	TRISA2	TRISA1	TRISA0	135
TRISC(2)	TRISC7(2)	TRISC6(2)	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	142

Legend: — = unimplemented location, read as '0'. Shaded cells are unused by the comparator module.

Note 1: Unimplemented, read as '1'.

2: PIC16(L)F1613 only.

21.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4 or 8 divisions of the clock input. The T1CKPS bits of the T1CON register control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

21.4 Timer1 Operation in Asynchronous Counter Mode

If control bit $\overline{\text{T1SYNC}}$ of the T1CON register is set, the external clock input is not synchronized. The timer increments asynchronously to the internal phase clocks. If the external clock source is selected then the timer will continue to run during Sleep and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (see **Section21.4.1 "Reading and Writing Timer1 in Asynchronous Counter Mode"**).

Note:	When switching from synchronous to asynchronous operation, it is possible to skip an increment. When switching from asynchronous to synchronous operation, it is possible to produce an additional increment.

21.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L while the timer is running from an external asynchronous clock will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the TMR1H:TMR1L register pair.

TABLE 21-4: TIMER1 GATE SOURCES

T1GSS	Timer1 Gate Source
00	Timer1 Gate pin (T1G)
01	Overflow of Timer0 (T0_overflow) (TMR0 increments from FFh to 00h)
10	Comparator 1 Output (C1_OUT_sync)(1)
11	Comparator 2 Output (C2_OUT_sync)(1,2)

Note 1: Optionally synchronized comparator output.
2: PIC16(L)F1613 only.

21.5 Timer1 Gate

Timer1 can be configured to count freely or the count can be enabled and disabled using Timer1 gate circuitry. This is also referred to as Timer1 Gate Enable.

Timer1 gate can also be driven by multiple selectable sources.

21.5.1 TIMER1 GATE ENABLE

The Timer1 Gate Enable mode is enabled by setting the TMR1GE bit of the T1GCON register. The polarity of the Timer1 Gate Enable mode is configured using the T1GPOL bit of the T1GCON register.

When Timer1 Gate Enable mode is enabled, Timer1 will increment on the rising edge of the Timer1 clock source. When Timer1 Gate Enable mode is disabled, no incrementing will occur and Timer1 will hold the current count. See Figure 21-3 for timing details.

TABLE 21-3: TIMER1 GATE ENABLE SELECTIONS

T1CLK	T1GPOL	T1G	Timer1 Operation
↑	0	0	Counts
↑	0	1	Holds Count
↑	1	0	Holds Count
↑	1	1	Counts

21.5.2 TIMER1 GATE SOURCE SELECTION

Timer1 gate source selections are shown in Table 21-4. Source selection is controlled by the T1GSS<1:0> bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

TABLE 21-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	—	—	—	ANSA4	—	ANSA2	ANSA1	ANSA0	136
APFCON	—	CWGASEL(2)	CWGBSEL(2)	—	T1GSEL	—	CCP2SEL(3)	CCP1SEL(2)	132
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	82
PIE1	TMR1GIE	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	83
PIR1	TMR1GIF	ADIF	—	—	—	CCP1IF	TMR2IF	TMR1IF	87
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Count								196*
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Count								196*
TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Count								196*
TMR3L	Holding Register for the Least Significant Byte of the 16-bit TMR3 Count								196*
TMR5H	Holding Register for the Most Significant Byte of the 16-bit TMR5 Count								196*
TMR5L	Holding Register for the Least Significant Byte of the 16-bit TMR5 Count								196*
TRISA	—	—	TRISA5	TRISA4	—(1)	TRISA2	TRISA1	TRISA0	135
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		—	$\overline{\text{T1SYNC}}$	—	TMR1ON	200
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		201
T3CON	TMR3CS<1:0>		T3CKPS<1:0>		—	T3SYNC	—	TMR3ON	200
T3GCON	TMR3GE	T3GPOL	T3GTM	T3GSPM	T3GGO/$\overline{\text{DONE}}$	T3GVAL	T3GSS<1:0>		201
T5CON	TMR5CS<1:0>		T5CKPS<1:0>		—	T5SYNC	—	TMR5ON	200
T5GCON	TMR5GE	T5GPOL	T5GTM	T5GSPM	T5GGO/$\overline{\text{DONE}}$	T5GVAL	T5GSS<1:0>		201

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.
* Page provides register information.

Note 1: Unimplemented, read as '1'.
2: PIC12(L)F1612 only.
3: PIC16(L)F1613 only.

REGISTER 22-4: TxRST: TIMER2 EXTERNAL RESET SIGNAL SELECTION REGISTER

U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	RSEL<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-4 **Unimplemented:** Read as ‘0’

bit 3-0 **RSEL<3:0>:** Timer2 External Reset Signal Source Selection bits
See Table 22-3.

TABLE 22-3: EXTERNAL RESET SOURCES

RSEL<4:0>	Timer2	Timer4	Timer6
1111	Reserved	Reserved	Reserved
1110	PWM4_out	PWM4_out	PWM4_out
1101	PWM3_out	PWM3_out	PWM3_out
1100	LC4_out	LC4_out	LC4_out
1011	LC3_out	LC3_out	LC3_out
1010	LC2_out	LC2_out	LC2_out
1001	LC1_out	LC1_out	LC1_out
1000	ZCD1_out	ZCD1_out	ZCD1_out
0111	TMR6_postscaled	TMR6_postscaled	Reserved
0110	TMR4_postscaled	Reserved	TMR4_postscaled
0101	Reserved	TMR2_postscaled	TMR2_postscaled
0100	CCP2_out	CCP2_out	CCP2_out
0011	CCP1_out	CCP1_out	CCP1_out
0010	C2OUT_sync	C2OUT_sync	C2OUT_sync
0001	C1OUT_sync	C1OUT_sync	C1OUT_sync
0000	Pin selected by T2INPPS	Pin selected by T2INPPS	Pin selected by T2INPPS

TABLE 22-4: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP1CON	EN	OE	OUT	FMT	MODE<3:0>				232
CCP2CON	EN	OE	OUT	FMT	MODE<3:0>				232
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	82
PIE1	TMR1GIE	ADIE	—	—	—	CCP1IE	TMR2IE	TMR1IE	83
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	87
PR2	Timer2 Module Period Register								205*
TMR2	Holding Register for the 8-bit TMR2 Register								205*
T2CON	ON	CKPS<2:0>			OUTPS<3:0>				219
T2CLKCON	—	—	—	—	CS<3:0>				218
T2RST	—	—	—	—	RSEL<3:0>				221
T2HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					220
PR4	Timer4 Module Period Register								205*
TMR4	Holding Register for the 8-bit TMR4 Register								205*
T4CON	ON	CKPS<2:0>			OUTPS<3:0>				219
T4CLKCON	—	—	—	—	CS<3:0>				218
T4RST	—	—	—	—	RSEL<3:0>				221
T4HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					220
PR6	Timer6 Module Period Register								205*
TMR6	Holding Register for the 8-bit TMR6 Register								205*
T6CON	ON	CKPS<2:0>			OUTPS<3:0>				219
T6CLKCON	—	—	—	—	—	T6CS<2:0>			218
T6RST	—	—	—	—	RSEL<3:0>				221
T6HLT	PSYNC	CKPOL	CKSYNC	MODE<4:0>					220

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.
* Page provides register information.

23.2.2 TIMER1 MODE RESOURCE

In Compare mode, Timer1 must be running in either Timer mode or Synchronized Counter mode. The compare operation may not work in Asynchronous Counter mode.

See **Section21.0 "Timer1/3/5 Module with Gate Control"** for more information on configuring Timer1.

Note:	Clocking Timer1 from the system clock (FOSC) should not be used in Compare mode. In order for Compare mode to recognize the trigger event on the CCPx pin, TImer1 must be clocked from the instruction clock (FOSC/4) or from an external clock source.

23.2.3 SOFTWARE INTERRUPT MODE

When Generate Software Interrupt mode is chosen (MODE<3:0> = `1010`), the CCPx module does not assert control of the CCPx pin (see the CCPxCON register).

23.2.4 COMPARE DURING SLEEP

The Compare mode is dependent upon the system clock (FOSC) for proper operation. Since FOSC is shut down during Sleep mode, the Compare mode will not function properly during Sleep.

23.2.5 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section12.1 "Alternate Pin Function"** for more information.

23.2.6 CAPTURE OUTPUT

When in Compare mode, the CCP will provide an output upon the 16-bit value of the CCPRxH:CCPRxL register pair matching the TMR1H:TMR1L register pair. The compare output depends on which Compare mode the CCP is configured as. If the MODE bits of CCPxCON register are equal to '`1011`' or '`1010`', the CCP module will output high, while TMR1 is equal to CCPRxH:CCPRxL register pair. This means that the pulse width is determined by the TMR1 prescaler. If the MODE bits of CCPxCON are equal to '`0001`' or '`0010`', the output will toggle upon a match, going from '`0`' to '`1`' or vice-versa. If the MODE bits of CCPxCON are equal to '`1001`', the output is cleared on a match, and if the MODE bits are equal to '`1000`', the output is set on a match. This output is available as an input signal to the CWG, as an auto-conversion trigger for the ADC, as an external Reset signal for the TMR2 modules, as a window input to the SMT, and as an input to the CLC module.

REGISTER 25-6: SMT1SIG: SMT1 SIGNAL INPUT SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	—	—	—	SSEL<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	q = Value depends on condition

bit 7-3 **Unimplemented**: Read as ‘0’

bit 2-0 **SSEL<2:0>:** SMT1 Signal Selection bits
111 = Reserved
110 = TMR6_postscaled
101 = TMR4_postscaled
100 = TMR2_postscaled
011 = ZCD1_out
010 = C2OUT_sync(1)
001 = C1OUT_sync
000 = SMTxSIG pin

Note 1: PIC16(L)F1613 only. Reserved on PIC12(L)F1612.

28.0 ELECTRICAL SPECIFICATIONS

28.1 Absolute Maximum Ratings(†)

Ambient temperature under bias .... -40°C to +125°C
Storage temperature .... -65°C to +150°C
Voltage on pins with respect to V_{SS}
 on V_{DD} pin
  PIC12F1612/16F1613 .... -0.3V to +6.5V
  PIC12LF1612/16F1613 .... -0.3V to +4.0V
 on $\overline{MCLR}$ pin .... -0.3V to +9.0V
 on all other pins .... -0.3V to (V_{DD} + 0.3V)
Maximum current
 on V_{SS} pin(1)
  -40°C ≤ T_A ≤ +85°C .... 250 mA
  +85°C ≤ T_A ≤ +125°C .... 85 mA
 on V_{DD} pin(1)
  -40°C ≤ T_A ≤ +85°C .... 250 mA
  +85°C ≤ T_A ≤ +125°C .... 85 mA
 Sunk by any standard I/O pin .... 50 mA
 Sourced by any standard I/O pin .... 50 mA
 Sunk by any High Current I/O pin .... 100 mA
 Sourced by any High Current I/O pin .... 100 mA
Clamp current, I_K (V_{PIN} < 0 or V_{PIN} > V_{DD}) .... ±20 mA
Total power dissipation(2) .... 800 mW

Note 1: Maximum current rating requires even load distribution across I/O pins. Maximum current rating may be limited by the device package power dissipation characterizations, see Table 28-6: "Thermal Characteristics" to calculate device specifications.

2: Power dissipation is calculated as follows: $P_{DIS} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD} - V_{OH}) \times I_{OH}\} + \sum(V_{Ol} \times I_{OL})$.

.

† NOTICE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure above maximum rating conditions for extended periods may affect device reliability.

28.2 Standard Operating Conditions

The standard operating conditions for any device are defined as:

Operating Voltage: $V_{DDMIN} \le V_{DD} \le V_{DDMAX}$
Operating Temperature: $T_{A\_MIN} \le T_A \le T_{A\_MAX}$

VDD — Operating Supply Voltage[1]

PIC12LF1612/16F1613

- VDDMIN (Fosc ≤ 16 MHz) .... +1.8V
- VDDMIN (Fosc ≤ 32 MHz) .... +2.5V
- VDDMAX .... +3.6V

PIC12F1612/16F1613

- VDDMIN (Fosc ≤ 16 MHz) .... +2.3V
- VDDMIN (Fosc ≤ 32 MHz) .... +2.5V
- VDDMAX .... +5.5V

TA — Operating Ambient Temperature Range

Industrial Temperature

- TA_MIN .... -40°C
- TA_MAX .... +85°C

Extended Temperature

- TA_MIN .... -40°C
- TA_MAX .... +125°C

Note 1: See Parameter D001, DS Characteristics: Supply Voltage.

TABLE 28-5: MEMORY PROGRAMMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
		Program Memory Programming Specifications					
D110	V_{IHH}	Voltage on $\overline{MCLR}$/V_{PP} pin	8.0	—	9.0	V	**(Note 2)**
D111	I_{DDP}	Supply Current during Programming	—	—	10	mA	
D112	V_{BE}	V_{DD} for Bulk Erase	2.7	—	V_{DDMAX}	V	
D113	V_{PEW}	V_{DD} for Write or Row Erase	V_{DDMIN}	—	V_{DDMAX}	V	
D114	I_{PPPGM}	Current on $\overline{MCLR}$/V_{PP} during Erase/Write	—	1.0	—	mA	
D115	I_{DDPGM}	Current on V_{DD} during Erase/Write	—	5.0	—	mA	
		Program Flash Memory					
D121	E_P	Cell Endurance	10K	—	—	E/W	$-40°C \le T_A \le +85°C$ **(Note 1)**
D122	V_{PRW}	V_{DD} for Read/Write	V_{DDMIN}	—	V_{DDMAX}	V	
D123	T_{IW}	Self-timed Write Cycle Time	—	2	2.5	ms	
D124	T_{RETD}	Characteristic Retention	—	40	—	Year	Provided no other specifications are violated
D125	E_{HEFC}	High-Endurance Flash Cell	100K	—	—	E/W	$0°C \le T_A \le +60°C$, lower byte last 128 addresses

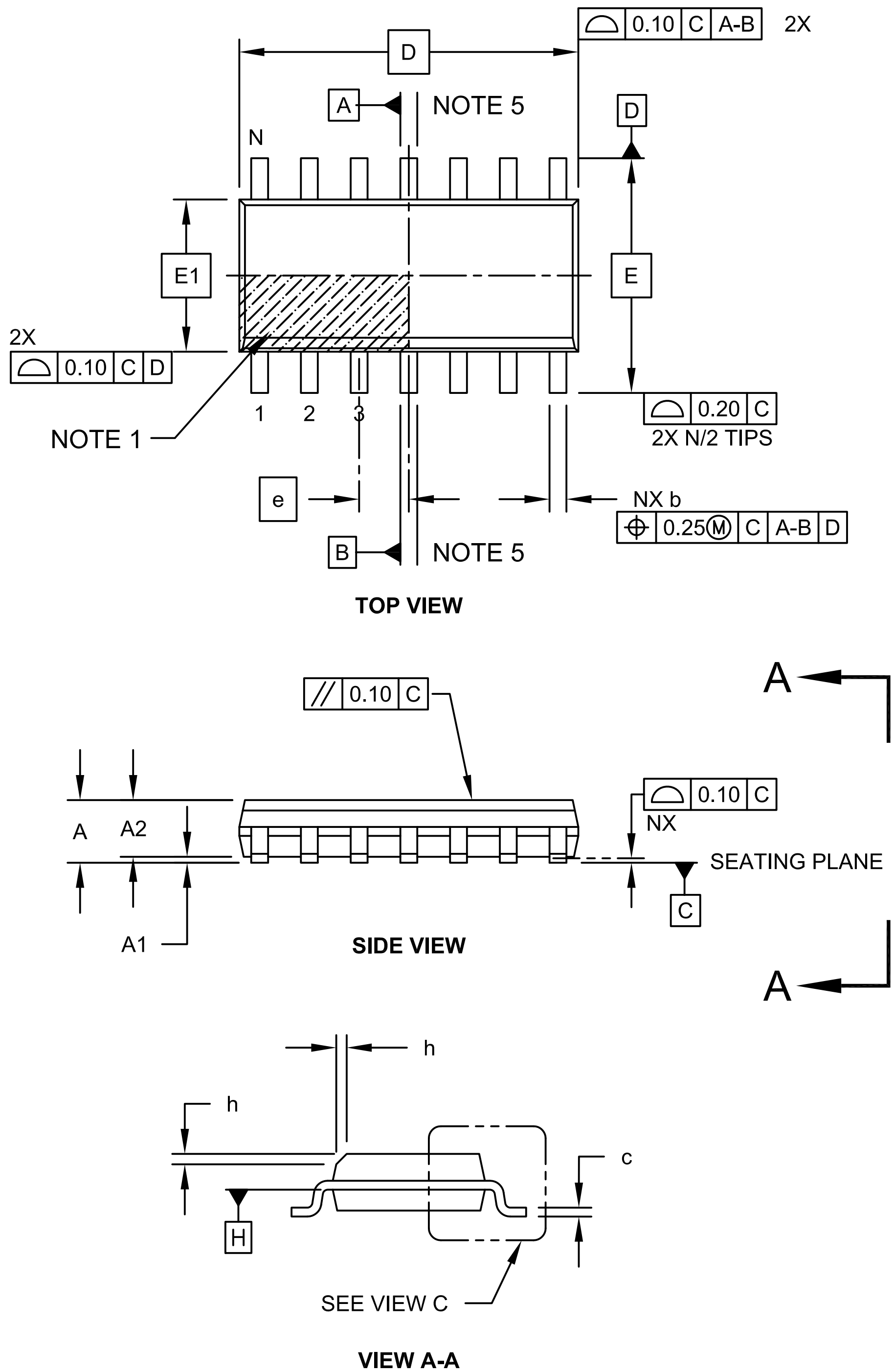
† Data in “Typ” column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Self-write and Block Erase.

2: Required only if single-supply programming is disabled.

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-065C Sheet 1 of 2