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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	6
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	8-VDFN Exposed Pad
Supplier Device Package	8-DFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1612-e-mf

PIC12(L)F1612/16(L)F1613

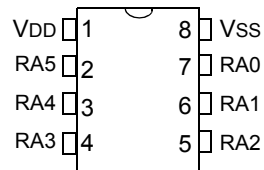
TABLE 2: PACKAGES

Packages	PDIP	SOIC	DFN	UDFN	TSSOP	QFN	UQFN	SSOP
PIC12(L)F1612	•	•	•	•				
PIC16(L)F1613	•	•			•	•	•	

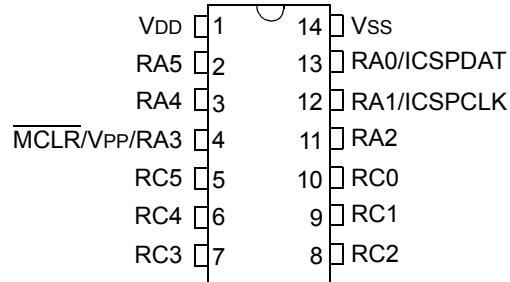
Note: Pin details are subject to change.

PIN DIAGRAMS

8-pin PDIP, SOIC, DFN, UDFN



14-pin PDIP, SOIC, TSSOP



16-pin QFN, UQFN

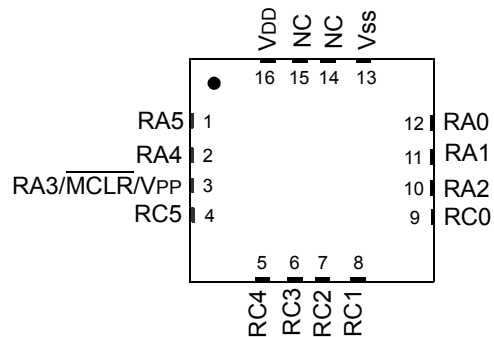


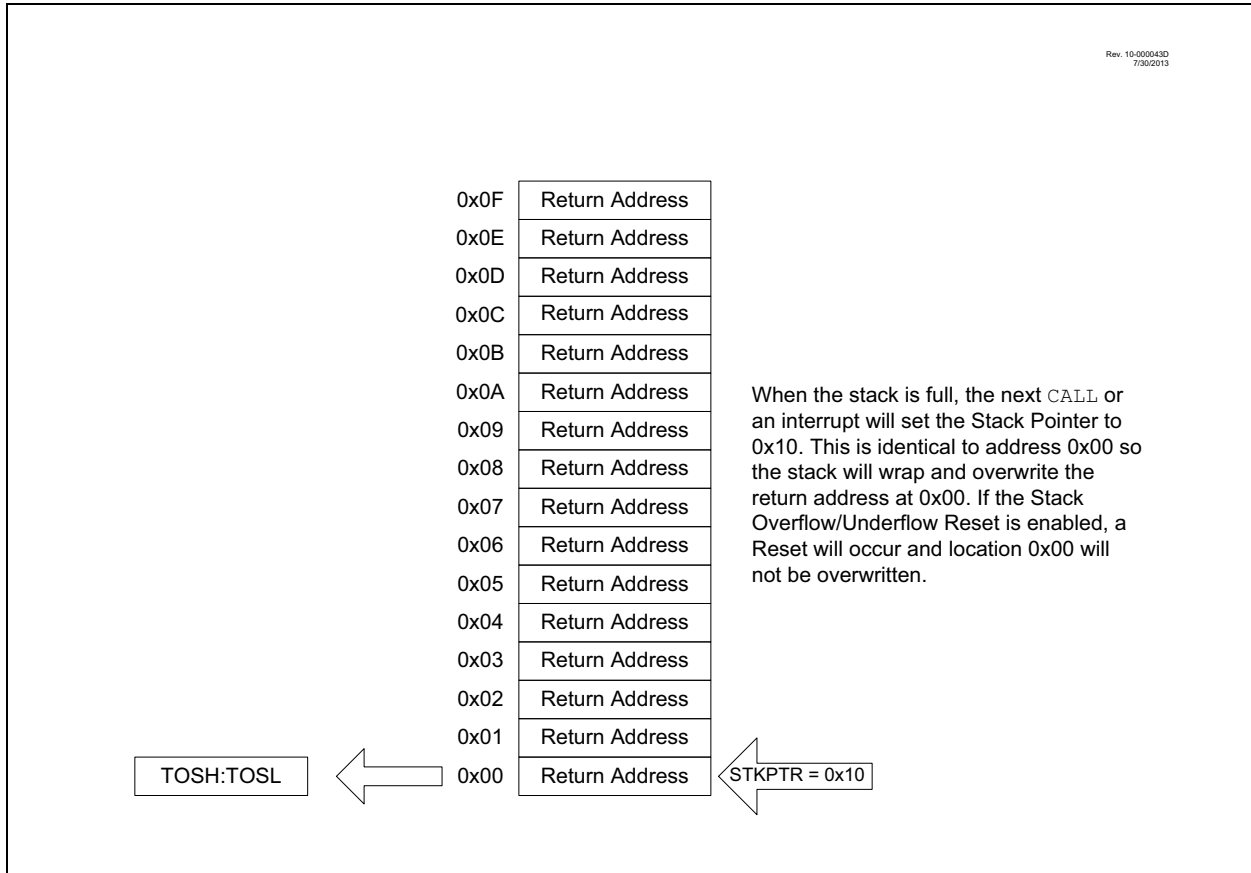
TABLE 3-9: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 5											
28Ch	ODCONA	—	—	ODA5	ODA4	—	ODA2	ODA1	ODA0	--00 -000	--00 -000
28Dh	—	Unimplemented								—	—
28Eh	ODCONC ⁽⁴⁾	—	—	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0	--00 0000	--00 0000
28Fh	—	Unimplemented								—	—
290h	—	Unimplemented								—	—
291h	CCP1RL	Capture/Compare/PWM 1 Register (LSB)								xxxx xxxx	uuuu uuuu
292h	CCP1RH	Capture/Compare/PWM 1 Register (MSB)								xxxx xxxx	uuuu uuuu
293h	CCP1CON	EN	OE	OUT	FMT	MODE<3:0>				0000 0000	0000 0000
294h	CCP1CAP	—	—	—	—	—	—	CTS<1:0>		---- --00	---- --00
295h — 297h	—	Unimplemented								—	—
298h	CCP2RL	Capture/Compare/PWM 2 Register (LSB)								xxxx xxxx	uuuu uuuu
299h	CCP2RH	Capture/Compare/PWM 2 Register (MSB)								xxxx xxxx	uuuu uuuu
29Ah	CCP2CON	EN	OE	OUT	FMT	MODE<3:0>				0000 0000	0000 0000
29Bh	CCP2CAP	—	—	—	—	—	—	CTS<1:0>		---- --00	---- --00
29Ch	—	Unimplemented								—	—
29Dh	—	Unimplemented								—	—
29Eh	CCPTMRS	—	—	—	—	C2TSEL<1:0>		C1TSEL<1:0>		---- 0000	---- 0000
29Fh	—	Unimplemented								—	—
Bank 6											
30Ch	SLRCONA	—	—	SLRA5	SLRA4	—	SLRA2	SLRA1	SLRA0	--00 -000	--00 -000
30Dh	—	Unimplemented								—	—
30Eh	SLRCONC ⁽⁴⁾	—	—	SLRC5	SLRC4	SLRC3	SLRC2	SLRC1	SLRC0	--00 0000	--00 0000
30Fh — 31Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, r = reserved. Shaded locations are unimplemented, read as '0'.

- Note**
- 1: PIC12F1612/16F1613 only.
 - 2: Unimplemented, read as '1'.
 - 3: PIC12(L)F1612 only.
 - 4: PIC16(L)F1613 only.

FIGURE 3-7: ACCESSING THE STACK EXAMPLE 4



3.5.2 OVERFLOW/UNDERFLOW RESET

If the `STVREN` bit in Configuration Words is programmed to '1', the device will be reset if the stack is `PUSHed` beyond the sixteenth level or `POPed` beyond the first level, setting the appropriate bits (`STKOVF` or `STKUNF`, respectively) in the `PCON` register.

3.6 Indirect Addressing

The `INDFn` registers are not physical registers. Any instruction that accesses an `INDFn` register actually accesses the register at the address specified by the File Select Registers (`FSR`). If the `FSRn` address specifies one of the two `INDFn` registers, the read will return '0' and the write will not occur (though Status bits may be affected). The `FSRn` register value is created by the pair `FSRnH` and `FSRnL`.

The `FSR` registers form a 16-bit address that allows an addressing space with 65536 locations. These locations are divided into three memory regions:

- Traditional Data Memory
- Linear Data Memory
- Program Flash Memory

PIC12(L)F1612/16(L)F1613

TABLE 6-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	71
PCON	STKOVF	STKUNF	WDTWV	RWD \overline{T}	RMCLR	R \overline{I}	POR	BOR	75
STATUS	—	—	—	T \overline{O}	P \overline{D}	Z	DC	C	21
WDTCON0	—	—	WDTPS<4:0>					SEN	99

Legend: — = unimplemented bit, reads as '0'. Shaded cells are not used by Resets.

Note 1: Other (non Power-up) Resets include MCLR Reset and Watchdog Timer Reset during normal operation.

TABLE 6-6: SUMMARY OF CONFIGURATION WORD WITH RESETS

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	—	—	CLKOUTEN	BOREN<1:0>		—	52
	7:0	CP	MCLRE	PWRT	—	—	—	FOSC<1:0>		
CONFIG2	13:8	—	—	LVP	DEBUG	LPBOR	BORV	STVREN	PLEN	53
	7:0	ZCD	—	—	—	—	—	WRT<1:0>		
CONFIG3	13:8	—	—	WDTCCS<2:0>			WDTCWS<2:0>			53
	7:0	—	WDTE<1:0>		WDTCPs<4:0>					

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

7.3 Interrupts During Sleep

Some interrupts can be used to wake from Sleep. To wake from Sleep, the peripheral must be able to operate without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the `SLEEP` instruction. The instruction directly after the `SLEEP` instruction will always be executed before branching to the ISR. Refer to **Section 8.0 “Power-Down Mode (Sleep)”** for more details.

7.4 INT Pin

The INT pin can be used to generate an asynchronous edge-triggered interrupt. This interrupt is enabled by setting the INTE bit of the INTCON register. The INTEDG bit of the OPTION_REG register determines on which edge the interrupt will occur. When the INTEDG bit is set, the rising edge will cause the interrupt. When the INTEDG bit is clear, the falling edge will cause the interrupt. The INTF bit of the INTCON register will be set when a valid edge appears on the INT pin. If the GIE and INTE bits are also set, the processor will redirect program execution to the interrupt vector.

7.5 Automatic Context Saving

Upon entering an interrupt, the return PC address is saved on the stack. Additionally, the following registers are automatically saved in the shadow registers:

- W register
- STATUS register (except for $\overline{\text{TO}}$ and $\overline{\text{PD}}$)
- BSR register
- FSR registers
- PCLATH register

Upon exiting the Interrupt Service Routine, these registers are automatically restored. Any modifications to these registers during the ISR will be lost. If modifications to any of these registers are desired, the corresponding shadow register should be modified and the value will be restored when exiting the ISR. The shadow registers are available in Bank 31 and are readable and writable. Depending on the user's application, other registers may also need to be saved.

PIC12(L)F1612/16(L)F1613

REGISTER 7-8: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

U-0	U-0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
—	—	CWGIF	ZCDIF	—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **CWGIF:** CWG Interrupt Flag bit

1 = Interrupt is pending

0 = Interrupt is not pending

bit 4 **ZCDIF:** ZCD Interrupt Flag bit

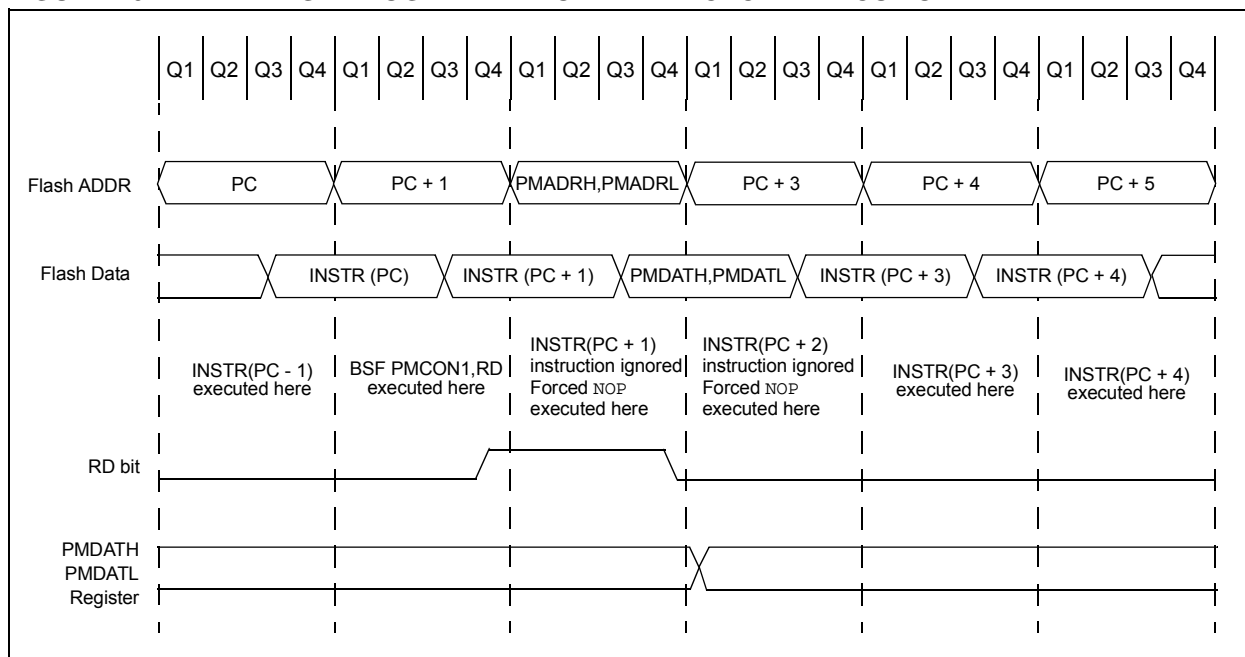
1 = Interrupt is pending

0 = Interrupt is not pending

bit 3-0 **Unimplemented:** Read as '0'

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

FIGURE 10-2: FLASH PROGRAM MEMORY READ CYCLE EXECUTION



EXAMPLE 10-1: FLASH PROGRAM MEMORY READ

```
* This code block will read 1 word of program
* memory at the memory address:
  PROG_ADDR_HI: PROG_ADDR_LO
* data will be returned in the variables;
*  PROG_DATA_HI, PROG_DATA_LO

  BANKSEL  PMADRL          ; Select Bank for PMCON registers
  MOVLW    PROG_ADDR_LO    ;
  MOVWF    PMADRL          ; Store LSB of address
  MOVLW    PROG_ADDR_HI    ;
  MOVWF    PMADRH          ; Store MSB of address

  BCF      PMCON1,CFGSS    ; Do not select Configuration Space
  BSF      PMCON1,RD       ; Initiate read
  NOP      ; Ignored (Figure 10-2)
  NOP      ; Ignored (Figure 10-2)

  MOVF     PMDATL,W        ; Get LSB of word
  MOVWF    PROG_DATA_LO    ; Store in user location
  MOVF     PMDATH,W        ; Get MSB of word
  MOVWF    PROG_DATA_HI    ; Store in user location
```


PIC12(L)F1612/16(L)F1613

REGISTER 12-14: WPUC: WEAK PULL-UP PORTC REGISTER^{(1),(2)}

U-0	U-0	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
—	—	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **WPUC<5:0>:** Weak Pull-up Register bits

1 = Pull-up enabled

0 = Pull-up disabled

Note 1: Global $\overline{\text{WPUEN}}$ bit of the OPTION_REG register must be cleared for individual pull-ups to be enabled.

Note 2: The weak pull-up device is automatically disabled if the pin is configured as an output.

REGISTER 12-15: ODCONC: PORTC OPEN-DRAIN CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **ODC<5:0>:** PORTC Open Drain Enable bits

For RC<5:0> pins, respectively

1 = Port pin operates as open-drain drive (sink current only)

0 = Port pin operates as standard push-pull drive (source and sink current)

13.0 INTERRUPT-ON-CHANGE

The PORTA and PORTC pins can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual port pin, or combination of port pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 13-1 is a block diagram of the IOC module.

13.1 Enabling the Module

To allow individual port pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

13.2 Individual Pin Configuration

For each port pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting both associated bits of the IOCxP and IOCxN registers, respectively.

13.3 Interrupt Flags

The IOCAFx and IOCCFx bits located in the IOCAF and IOCCF registers, respectively, are status flags that correspond to the interrupt-on-change pins of the associated port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCAFx and IOCCFx bits.

13.4 Clearing Interrupt Flags

The individual status flags, (IOCAFx and IOCCFx bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 13-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW    0xff
XORWF    IOCAF, W
ANDWF    IOCAF, F
```

13.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the IOCxF register will be updated prior to the first instruction executed out of Sleep.

PIC12(L)F1612/16(L)F1613

REGISTER 16-3: ADCON2: ADC CONTROL REGISTER 2

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0
TRIGSEL<3:0> ⁽¹⁾				—	—	—	—
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-4 **TRIGSEL<3:0>:** Auto-Conversion Trigger Selection bits⁽¹⁾

1111 = SMT2_PR
 1110 = SMT1_PR
 1101 = TMR6_postscaled
 1100 = TMR4_postscaled
 1011 = SMT2_CPR
 1010 = SMT2_CPW
 1001 = SMT1_CPR
 1000 = SMT1_CPW
 0111 = C2_OUT_sync⁽³⁾
 0110 = C1_OUT_sync
 0101 = TMR2_postscaled
 0100 = T1_overflow⁽²⁾
 0011 = T0_overflow⁽²⁾
 0010 = CCP2_out
 0001 = CCP1_out
 0000 = No auto-conversion trigger selected

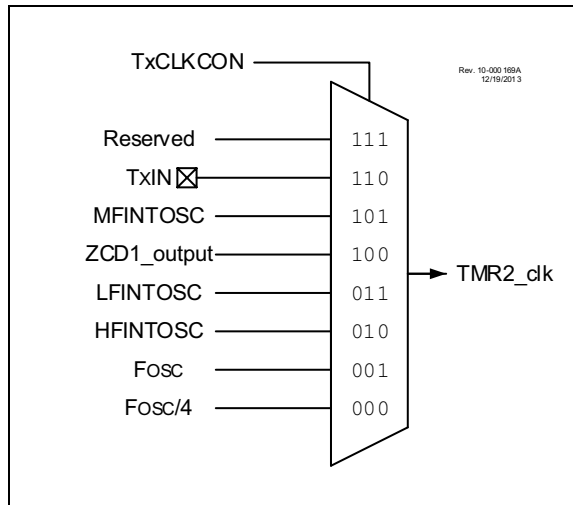
bit 3-0 **Unimplemented:** Read as '0'

Note 1: This is a rising edge sensitive input for all sources.

2: Signal also sets its corresponding interrupt flag.

3: PIC16(L)F1613 only. Reserved on PIC12(L)F1612.

FIGURE 22-2: TIMER2 CLOCK SOURCE BLOCK DIAGRAM



24.12 Configuring the CWG

The following steps illustrate how to properly configure the CWG.

1. Ensure that the TRIS control bits corresponding to the desired CWG pins for your application are set so that the pins are configured as inputs.
2. Clear the EN bit, if not already cleared.
3. Set desired mode of operation with the MODE bits.
4. Set desired dead-band times, if applicable to mode, with the CWGxDBR and CWGxDBF registers.
5. Setup the following controls in the CWGxAS0 and CWGxAS1 registers.
 - a. Select the desired shutdown source.
 - b. Select both output overrides to the desired levels (this is necessary even if not using auto-shutdown because start-up will be from a shutdown state).
 - c. Set which pins will be affected by auto-shutdown with the CWGxAS1 register.
 - d. Set the SHUTDOWN bit and clear the REN bit.
6. Select the desired input source using the CWGxISM register.
7. Configure the following controls.
 - a. Select desired clock source using the CWGxCLKCON register.
 - b. Select the desired output polarities using the CWGxCON1 register.
 - c. Set the output enables for the desired outputs.
8. Set the EN bit.
9. Clear TRIS control bits corresponding to the desired output pins to configure these pins as outputs.
10. If auto-restart is to be used, set the REN bit and the SHUTDOWN bit will be cleared automatically. Otherwise, clear the SHUTDOWN bit to start the CWG.

24.12.1 PIN OVERRIDE LEVELS

The levels driven to the output pins, while the shutdown input is true, are controlled by the LSB and LSAC bits of the CWGxAS0 register. LSB<1:0> controls the CWGxB and D override levels and LSAC<1:0> controls the CWGxA and C override levels. The control bit logic level corresponds to the output logic drive level while in the shutdown state. The polarity control does not affect the override level.

24.12.2 AUTO-SHUTDOWN RESTART

After an auto-shutdown event has occurred, there are two ways to resume operation:

- Software controlled
- Auto-restart

The restart method is selected with the REN bit of the CWGxAS0 register. Waveforms of software controlled and automatic restarts are shown in Figure 24-13 and Figure 24-14.

24.12.2.1 Software Controlled Restart

When the REN bit of the CWGxAS0 register is cleared, the CWG must be restarted after an auto-shutdown event by software. Clearing the shutdown state requires all selected shutdown inputs to be low, otherwise the SHUTDOWN bit will remain set. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

24.12.2.2 Auto-Restart

When the REN bit of the CWGxAS0 register is set, the CWG will restart from the auto-shutdown state automatically. The SHUTDOWN bit will clear automatically when all shutdown sources go low. The overrides will remain in effect until the first rising edge event after the SHUTDOWN bit is cleared. The CWG will then resume operation.

24.12.3 ALTERNATE OUTPUT PINS

This module incorporates outputs that can be moved to alternate pins with the use of the alternate pin function register APFCON. To determine which outputs can be moved and what their default pins are upon a Reset, see **Section 12.1 “Alternate Pin Function”** for more information.

25.6.5 WINDOWED MEASURE MODE

This mode measures the window duration of the SMTWINx input of the SMT. It begins incrementing the timer on a rising edge of the SMTWINx input and updates the SMTxCPR register with the value of the timer and resets the timer on a second rising edge. See Figure 25-10 and Figure 25-11.

25.6.10 GATED COUNTER MODE

This mode counts pulses on the SMTx_signal input, gated by the SMTxWIN input. It begins incrementing the timer upon seeing a rising edge of the SMTxWIN input and updates the SMTxCPW register upon a falling edge on the SMTxWIN input. See Figure 25-19 and Figure 25-20.

PIC12(L)F1612/16(L)F1613

TABLE 28-3: POWER-DOWN CURRENTS (IPD)^(1,2)

PIC12LF1612/16F1613		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC12F1612/16F1613		Low-Power Sleep Mode, VREGPM = 1						
Param. No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							VDD	Note
D022	Base IPD	—	0.020	1.0	8.0	μA	1.8	WDT, BOR, FVR disabled, all Peripherals inactive
		—	0.025	2.0	9.0	μA	3.0	
D022	Base IPD	—	0.25	3.0	10	μA	2.3	WDT, BOR, FVR disabled, all Peripherals inactive, Low-Power Sleep mode
		—	0.30	4.0	12	μA	3.0	
		—	0.40	6.0	15	μA	5.0	
D022A	Base IPD	—	9.8	16	18	μA	2.3	WDT, BOR, FVR disabled, all Peripherals inactive, Normal-Power Sleep mode, VREGPM = 0
		—	10.3	18	20	μA	3.0	
		—	11.5	21	26	μA	5.0	
D023		—	0.26	2.0	9.0	μA	1.8	WDT Current
		—	0.44	3.0	10	μA	3.0	
D023		—	0.43	6.0	15	μA	2.3	WDT Current
		—	0.53	7.0	20	μA	3.0	
		—	0.64	8.0	22	μA	5.0	
D023A		—	15	28	30	μA	1.8	FVR Current
		—	18	30	33	μA	3.0	
D023A		—	18	33	35	μA	2.3	FVR Current
		—	19	35	37	μA	3.0	
		—	20	37	39	μA	5.0	
D024		—	6.0	17	20	μA	3.0	BOR Current
D024		—	7.0	17	30	μA	3.0	BOR Current
		—	8.0	20	40	μA	5.0	
D24A		—	0.1	4.0	10	μA	3.0	LPBOR Current
D24A		—	0.35	5.0	14	μA	3.0	LPBOR Current
		—	0.45	8.0	17	μA	5.0	
D026		—	0.11	1.5	9.0	μA	1.8	ADC Current (Note 3), No conversion in progress
		—	0.12	2.7	10	μA	3.0	
D026		—	0.30	4.0	11	μA	2.3	ADC Current (Note 3), No conversion in progress
		—	0.35	5.0	13	μA	3.0	
		—	0.45	8.0	16	μA	5.0	
D026A*		—	250	—	—	μA	1.8	ADC Current (Note 3), Conversion in progress
		—	250	—	—	μA	3.0	
D026A*		—	280	—	—	μA	2.3	ADC Current (Note 3), Conversion in progress
		—	280	—	—	μA	3.0	
		—	280	—	—	μA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Legend: TBD = To Be Determined

Note 1: The peripheral Δ current can be determined by subtracting the base IPD current from this limit. Max. values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to Vss.

3: ADC clock source is FRC.

PIC12(L)F1612/16(L)F1613

TABLE 28-16: DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS⁽¹⁾

Operating Conditions (unless otherwise stated) V _{DD} = 3.0V, T _A = 25°C							
Param. No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
DAC01*	CLSB	Step Size	—	V _{DD} /256	—	V	
DAC02*	CACC	Absolute Accuracy	—	—	± 1.5	LSb	
DAC03*	CR	Unit Resistor Value (R)	—	—	—	Ω	
DAC04*	CST	Settling Time ⁽²⁾	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: See Section 29.0 “DC and AC Characteristics Graphs and Charts” for operating characterization.

2: Settling time measured while DACR<4:0> transitions from ‘0000’ to ‘1111’.

TABLE 28-17: ZERO CROSS PIN SPECIFICATIONS

Operating Conditions (unless otherwise stated) V _{DD} = 3.0V, T _A = 25°C							
Param. No.	Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
ZC01	ZCPINV	Voltage on Zero Cross Pin	—	0.75	—	V	
ZC02	ZCSRC	Source current	—	-300	-600	μA	
ZC03	ZCSNK	Sink current	—	300	600	μA	
ZC04	ZCISW	Response Time Rising Edge	—	1	—	μs	
		Response Time Falling Edge	—	1	—	μs	
ZC05	ZCOUT	Response Time Rising Edge	—	1	—	μs	
		Response Time Falling Edge	—	1	—	μs	

* These parameters are characterized but not tested.

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Note: Unless otherwise noted, $V_{IN} = 5V$, $F_{OSC} = 500\text{ kHz}$, $C_{IN} = 0.1\text{ }\mu F$, $T_A = 25^\circ C$.

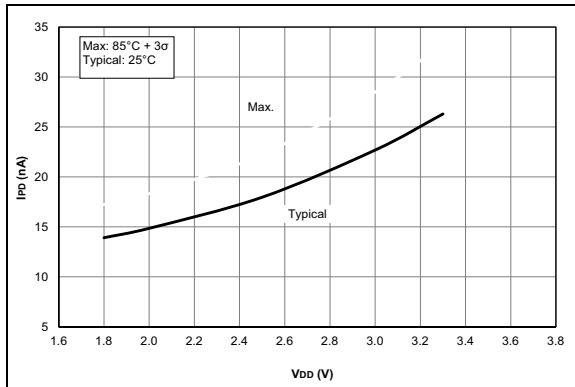


FIGURE 29-25: I_{PD} , Fixed Voltage Reference (FVR), PIC12LF1612/16F1613 Only.

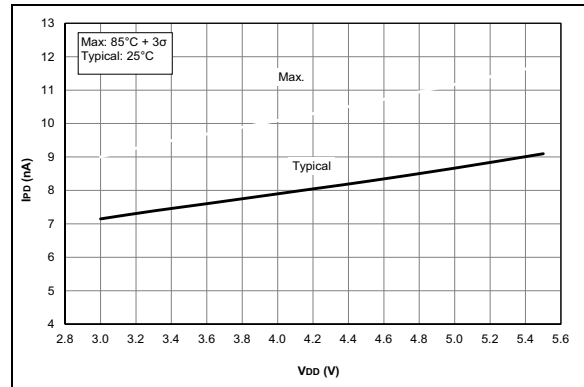


FIGURE 29-28: I_{PD} , Brown-Out Reset (BOR), BORV = 1, PIC12F1612/16F1613 Only.

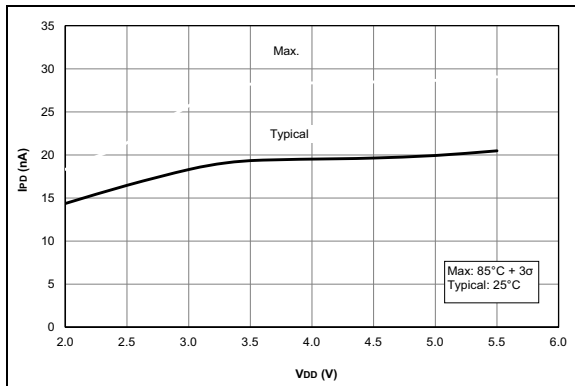


FIGURE 29-26: I_{PD} , Fixed Voltage Reference (FVR), PIC12F1612/16F1613 Only.

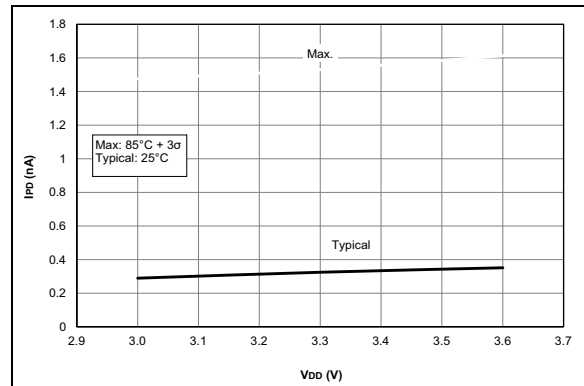


FIGURE 29-29: I_{PD} , LP Brown-Out Reset (LPBOR = 0), PIC12LF1612/16F1613 Only.

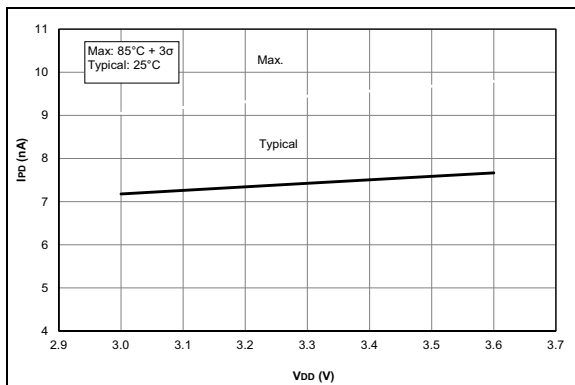


FIGURE 29-27: I_{PD} , Brown-Out Reset (BOR), BORV = 1, PIC12LF1612/16F1613 Only.

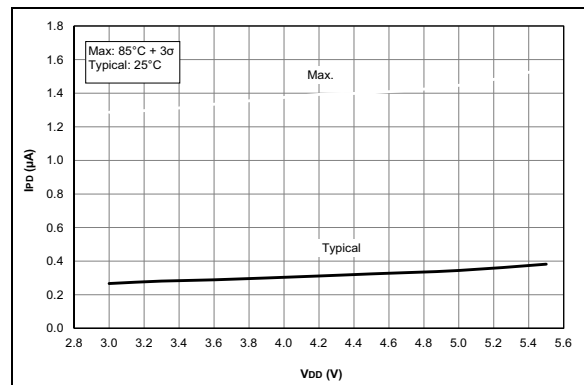


FIGURE 29-30: I_{PD} , LP Brown-Out Reset (LPBOR = 0), PIC12F1612/16F1613 Only.

30.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16, and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

30.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

30.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

30.5 MPLAB Assembler, Linker and Librarian for Various Device Families

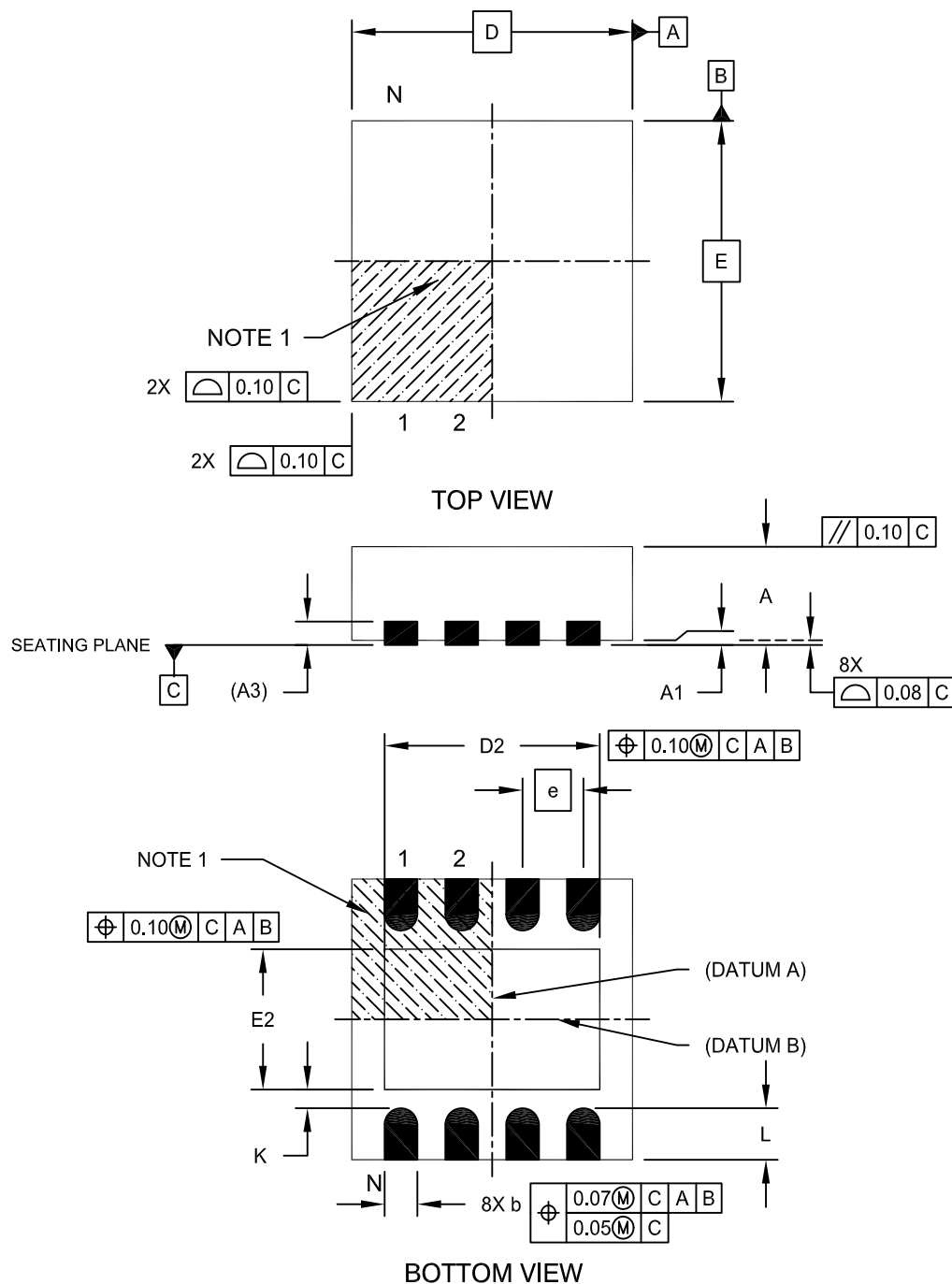
MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

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8-Lead Plastic Dual Flat, No Lead Package (MF) - 3x3x0.9mm Body [DFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>

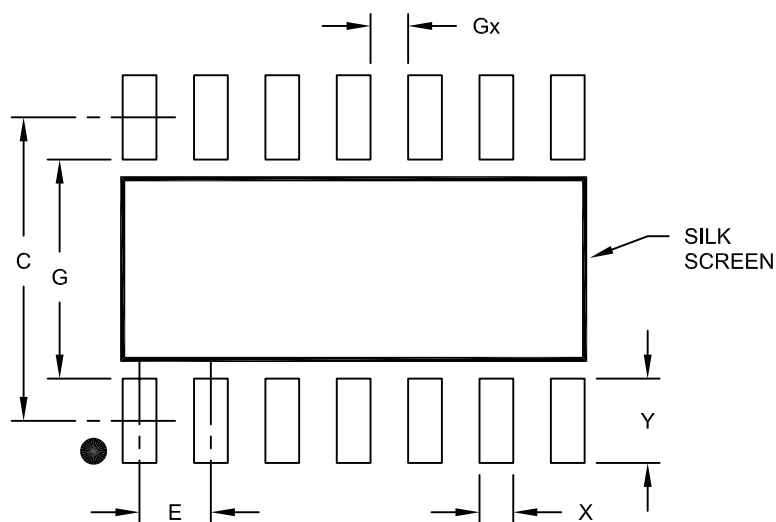


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PIC12(L)F1612/16(L)F1613

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A