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What is "[Embedded - Microcontrollers](#)"?

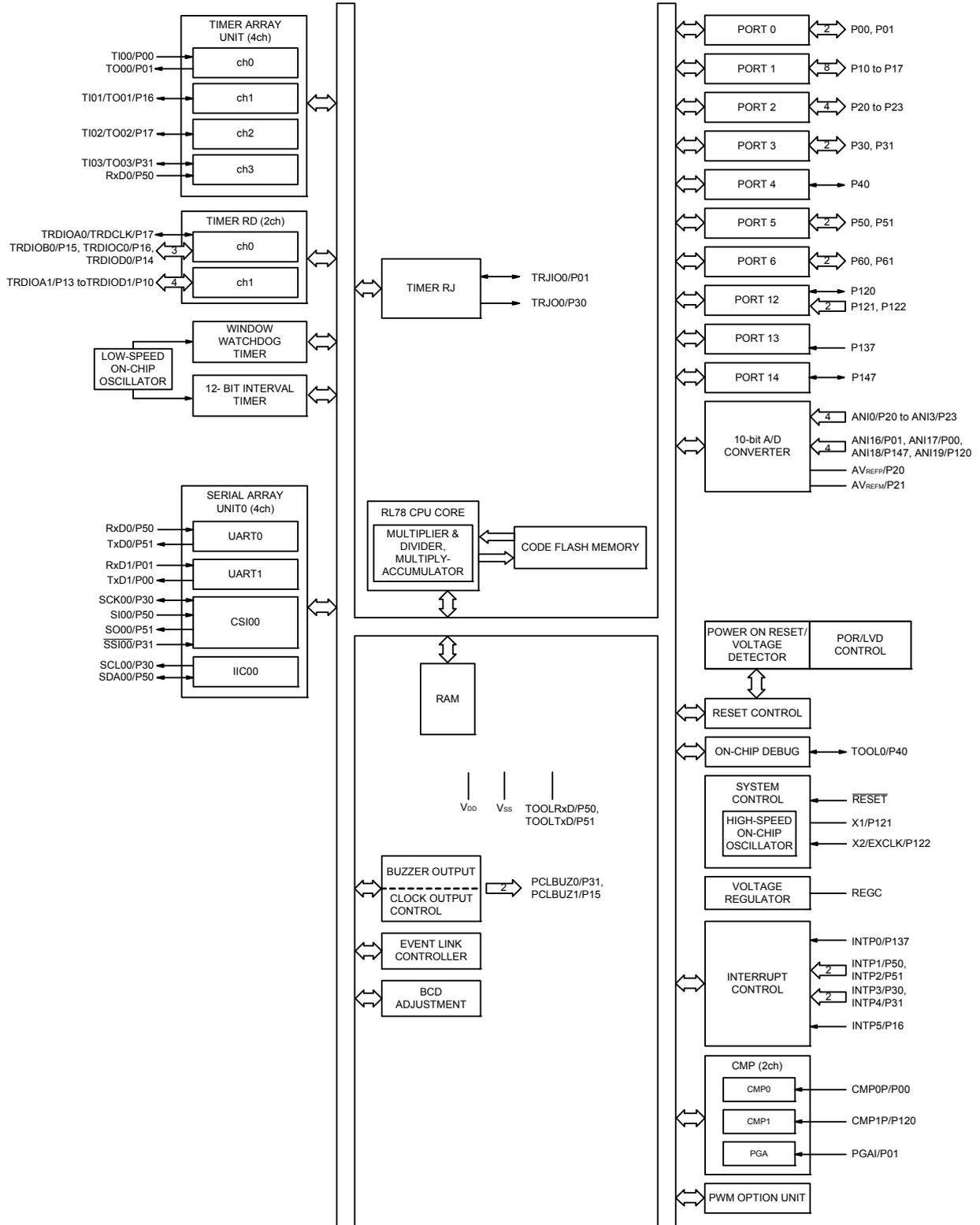
"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I ² C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	23
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	30-LSSOP (0.240", 6.10mm Width)
Supplier Device Package	30-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11eaaasp-50

1.5 Block Diagram

1.5.1 30-pin products



(2/2)

Item	30-pin	32-pin	44-pin
	R5F11EA8ASP, R5F11EAAAASP	R5F11EB8AFP, R5F11EBAAFP	R5F11EF8AFP, R5F11EFAAFP
Clock output/buzzer output	2 • 2.44 kHz, 4.88 kHz, 9.77 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f _{MAIN} = 20 MHz operation)		
8/10-bit resolution A/D converter	8 channels		12 channels
Comparator	2 channels		
PGA	1 channel		
Serial interface	• CSI: 1 channel/UART0: 1 channel/simplified I ² C: 1 channel • UART1: 1 channel		
Event link controller (ELC)	Event input: 18 Event trigger output: 6		Event input: 19 Event trigger output: 6
Vectored interrupt sources	Internal	20	
	External	6	7
Key interrupt	—		4
Reset	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 		
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V 		
Voltage detector	2.75 V to 4.06 V (6 stages)		
On-chip debug function	Provided		
Power supply voltage	V _{DD} = 2.7 to 5.5 V		
Operating ambient temperature	T _A = -40 to +85°C		

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

Caution 1. The RL78 microcontroller has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. The pins mounted are as follows according to product.

2.1 Pins Mounted According to Product

2.1.1 Port functions

Refer to 2.1.1 30-pin products, 2.1.2 32-pin products, and 2.1.3 44-pin products in the RL78/G1G User's Manual.

2.1.2 Non-port functions

Refer to 2.2.1 With functions for each product in the RL78/G1G User's Manual.

2.3 Oscillator Characteristics

2.3.1 X1 oscillator characteristics

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator, refer to 5.4 System Clock Oscillator in the RL78/G1G User's Manual.

2.3.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency ^{Notes 1, 2}	f _{IH}		1		24	MHz
	f _{HOCO}		1		48	
High-speed on-chip oscillator clock frequency accuracy			-2		+2	%
Low-speed on-chip oscillator clock frequency	f _{IL}			15		kHz
Low-speed on-chip oscillator clock frequency accuracy			-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	IOL1	Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147			20.0	mA ^{Note 2}
		Total of P00, P01, P40, P41, P120 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ VDD ≤ 5.5 V		70.0	mA
			2.7 V ≤ VDD < 4.0 V		15.0	mA
	Total of P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P73, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ VDD ≤ 5.5 V		80.0	mA	
		2.7 V ≤ VDD < 4.0 V		35.0	mA	
	Total of all pins (When duty ≤ 70% ^{Note 3})			150.0	mA	
	IOL2	Per pin for P20 to P27			0.4	mA ^{Note 2}
Total of all pins (When duty ≤ 70% ^{Note 3})	2.7 V ≤ VDD ≤ 5.5 V		5.0	mA		

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pin.

Note 2. However, do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output voltage, high	VOH1	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -10.0 mA	VDD - 1.5			V
			4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -3.0 mA	VDD - 0.7			V
			2.7 V ≤ VDD ≤ 5.5 V, IOH1 = -2.0 mA	VDD - 0.6			V
			2.7 V ≤ VDD ≤ 5.5 V, IOH1 = -1.0 mA	VDD - 0.5			V
	VOH2	P20 to P27	2.7 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA	VDD - 0.5			V
Output voltage, low	VOL1	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 20.0 mA			1.3	V
			4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 8.5 mA			0.7	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 3.0 mA			0.6	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA			0.4	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 0.3 mA			0.4	V
	VOL2	P20 to P27	2.7 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA			0.4	V

Caution P00, P10, P15, P17, P30, P50, and P51 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.4.2 Supply current characteristics

(1) Flash ROM: 16 KB of 30-pin to 44-pin products

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

(1/2)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Notes 3, 4	fHOCO = 48 MHz, fIH = 24 MHz	Basic operation	VDD = 5.0 V		1.8		mA	
				VDD = 3.0 V			1.8				
		HS (high-speed main) mode Notes 3, 4	fHOCO = 48 MHz, fIH = 24 MHz	Normal operation	VDD = 5.0 V		3.9	6.9	mA		
					VDD = 3.0 V		3.9	6.9			
					fHOCO = 24 MHz, fIH = 24 MHz	Normal operation	VDD = 5.0 V			3.7	6.3
							VDD = 3.0 V			3.7	6.3
		fHOCO = 16 MHz, fIH = 16 MHz	Normal operation	VDD = 5.0 V		2.8	4.6				
				VDD = 3.0 V		2.8	4.6				
		LS (low-speed main) mode Notes 3, 4	fIH = 8 MHz	Normal operation	VDD = 3.0 V		1.2	2.0	mA		
		HS (high-speed main) mode Notes 2, 4	fMX = 20 MHz, VDD = 5.0 V	Normal operation	Square wave input		3.1	5.3	mA		
					Resonator connection		3.3	5.5			
				Normal operation	Square wave input		3.1	5.3			
					Resonator connection		3.3	5.5			
				Normal operation	Square wave input		2.0	3.1			
Resonator connection					2.0	3.2					
Normal operation	Square wave input				2.0	3.1					
	Resonator connection				2.0	3.2					
LS (low-speed main) mode Notes 2, 4	fMX = 8 MHz, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA				
			Resonator connection		1.2	2.0					

Note 1. Total current flowing into VDD, including the input leakage current flowing when the level of the input pin is fixed to VDD or VSS. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, watchdog timer, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

Note 2. When high-speed on-chip oscillator is stopped.

Note 3. When high-speed system clock is stopped.

Note 4. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.

HS (high speed main) mode: VDD = 2.7 V to 5.5 V@1 MHz to 24 MHz

LS (low speed main) mode: VDD = 2.7 V to 5.5 V@1 MHz to 8 MHz

Remark 1. fMX: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. fHOCO: High-speed on-chip oscillator clock frequency (48 MHz max.)

Remark 3. fIH: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 4. Temperature condition of the TYP. value is TA = 25°C

(2) Peripheral Functions (Common to all products)**(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
12-bit interval timer operating current	I _{IT} Notes 1, 8				0.02		μA	
Watchdog timer operating current	I _{WDT} Notes 1, 2	f _{IL} = 15 kHz			0.22		μA	
A/D converter operating current	I _{ADC} Note 3	When conversion at maximum speed	Normal mode, AV _{REFP} = V _{DD} = 5.0 V		1.3	1.7	mA	
			Low voltage mode, AV _{REFP} = V _{DD} = 3.0 V		0.5	0.7		
A/D converter reference voltage current	I _{ADREF}				75		μA	
Temperature sensor operating current	I _{TMPS}				75		μA	
Comparator operating current	I _{COMP} Note 4	Per channel of comparator 1	When the comparator is operating		45.0	65.0	μA	
			When the comparator is stopped		0.0	0.1		
Programmable gain amplifier operating current	I _{PGA} Note 5	When the programmable gain amplifier is operating			240.0	340.0	μA	
		When the programmable gain amplifier is stopped			0.0	0.1		
LVD operating current	I _{LVI} Note 6				0.08		μA	
SNOOZE operating current	I _{SNOZ}	ADC operation	The mode is performed Note 7			0.50	0.60	mA
			The A/D conversion operations are performed	Low voltage mode AV _{REFP} = V _{DD} = 3.0 V		1.20	1.44	
		CSI/UART operation			0.70	0.84	mA	

Note 1. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 2. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontroller is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 3. Current flowing only to the A/D converter. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Note 4. Current flowing only to the comparator. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{COMP} when the comparator operates in operating mode or HALT mode.

Note 5. Current flowing only to the programmable gain amplifier. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{PGA} when the programmable gain amplifier operates in operating mode or HALT mode.

Note 6. Current flowing only to the LVD circuit. The current value of the RL78 microcontroller is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

Note 7. For details on the transition time to SNOOZE mode, refer to **18.3.3 SNOOZE mode in the RL78/G1G User's Manual**.

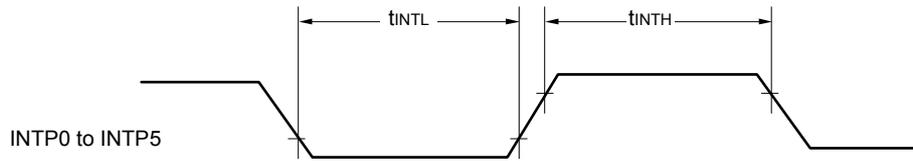
Note 8. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

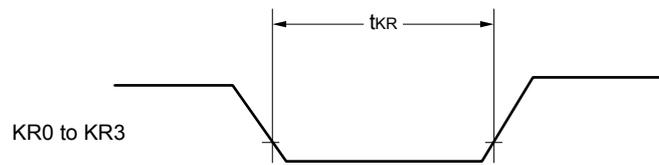
Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 3. Temperature condition of the TYP. value is TA = 25°C

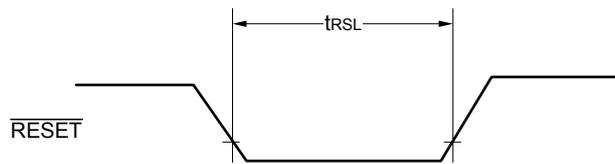
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Parameter	Symbol	Conditions		HS (high-speed main mode)		LS (low-speed main mode)		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time ^{Note 5}	tkCY2	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		ns
			$f_{MCK} \leq 20\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{MCK}$	$8/f_{MCK}$		—		ns
			$f_{MCK} \leq 16\text{ MHz}$	$6/f_{MCK}$		$6/f_{MCK}$		ns
SCKp high-/low-level width	tkH2, tkL2	$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$tkCY2/2 - 7$		$tkCY2/2 - 7$		ns
		$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$tkCY2/2 - 8$		$tkCY2/2 - 8$		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	tsIK2	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 20$		$1/f_{MCK} + 30$		ns
Slp hold time (from SCKp \uparrow) ^{Note 2}	tkSI2	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$1/f_{MCK} + 31$		$1/f_{MCK} + 31$		ns
Delay time from SCKp \downarrow to SOp output ^{Note 3}	tkSO2	$C = 30\text{ pF}$ ^{Note 4}	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		$2/f_{MCK} + 44$		$2/f_{MCK} + 110$	ns
$\overline{\text{SSI00}}$ setup time	tSSI K	DAPmn = 0	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	120		120		ns
		DAPmn = 1	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$1/f_{MCK} + 120$		$1/f_{MCK} + 120$		ns
$\overline{\text{SSI00}}$ hold time	tkSSI	DAPmn = 0	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	$1/f_{MCK} + 120$		$1/f_{MCK} + 120$		ns
		DAPmn = 1	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	120		120		ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Note 6. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[\text{F}]$: Communication line (TxDq) load capacitance, $V_b[\text{V}]$: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

Remark 3. f_{mck} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03))

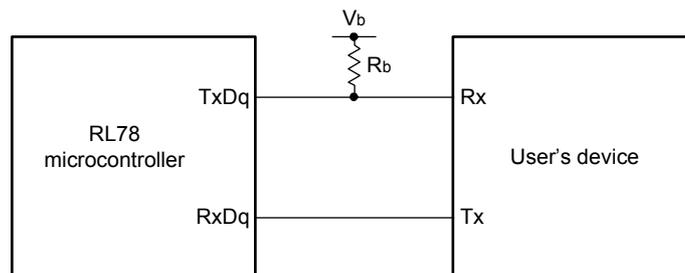
Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in UART mode.

$4.0\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$: $V_{IH} = 2.2\text{ V}$, $V_{IL} = 0.8\text{ V}$

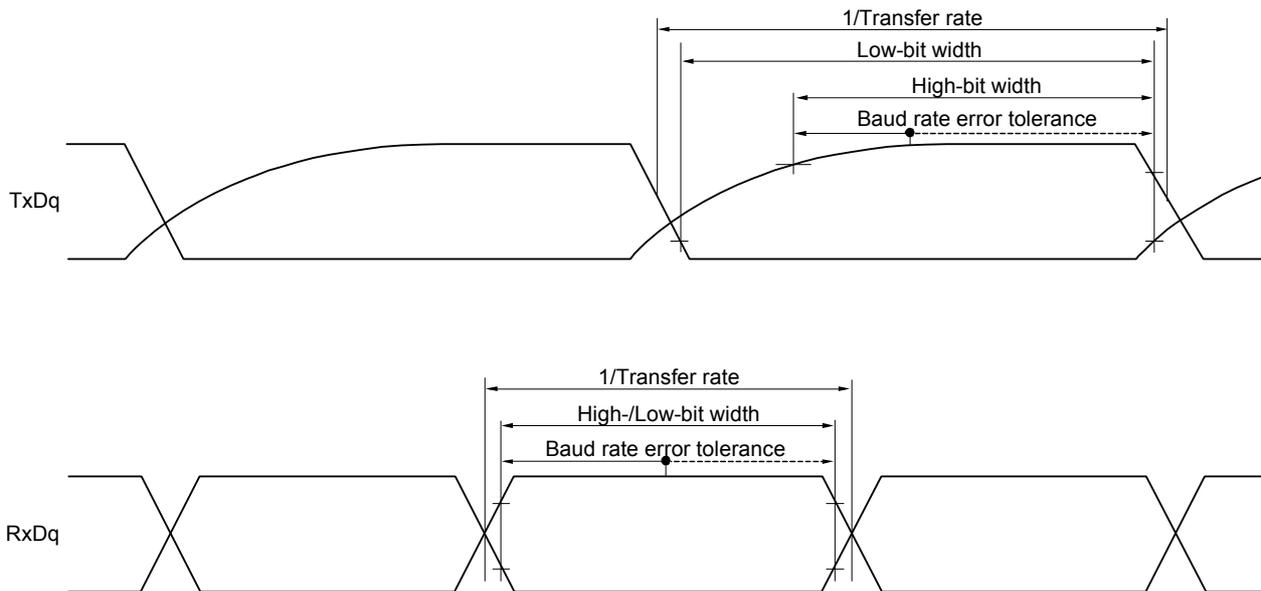
$2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$: $V_{IH} = 2.0\text{ V}$, $V_{IL} = 0.5\text{ V}$

$2.7\text{ V} \leq V_{DD} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$: $V_{IH} = 1.50\text{ V}$, $V_{IL} = 0.32\text{ V}$

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0, 1), g: PIM and POM number (g = 0, 5)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ 2/fCLK 4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	200		1150		ns
			300		1150		ns
SCKp high-level width	tkH1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 120		tkCY1/2 - 120		ns
SCKp low-level width	tkL1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 7		tkCY1/2 - 50		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 10		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) Note 1	tsIK1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	58		479		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	121		479		ns
Slp hold time (from SCKp↑) Note 1	tkSI1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		ns
Delay time from SCKp↓ to SOP output Note 1	tkSO1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		60		60	ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		130		130	ns
Slp setup time (to SCKp↓) Note 2	tsIK1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	23		110		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	33		110		ns
Slp hold time (from SCKp↓) Note 2	tkSI1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		ns
Delay time from SCKp↑ to SOP output Note 2	tkSO1	4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		10		10	ns
		2.7 V ≤ VDD < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		10		10	ns

(Notes, Caution and Remarks are listed on the next page.)

2.7 Analog Characteristics

2.7.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage	Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM	Reference voltage (+) = VDD Reference voltage (-) = VSS	Reference voltage (+) = VBGR Reference voltage (-) = AVREFM
ANI0 to ANI7		Refer to 2.7.1 (1).	Refer to 2.7.1 (3).	Refer to 2.7.1 (4).
ANI16 to ANI19		Refer to 2.7.1 (2).		
Internal reference voltage Temperature sensor output voltage		Refer to 2.7.1 (1).		—

(1) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI2 to ANI7

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP,
Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V		1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution AVREFP = VDD	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±0.25	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±0.25	% FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±1.5	LSB
Reference voltage (+)	AVREFP			2.7		VDD	V
Analog input voltage	VAIN			0		AVREFP	V
	VBGR	Select internal reference voltage output, 2.7 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

- (3) When $AV_{REF}(+) = V_{DD}$ ($ADREFP1 = 0$, $ADREFP0 = 0$), $AV_{REF}(-) = V_{SS}$ ($ADREFM = 0$),
target ANI pin: ANI0 to ANI7, ANI16 to ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{DD} , Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		1.2	± 7.0	LSB
Conversion time	tCONV	10-bit resolution	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
Integral linearity error Note 1	ILE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 4.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	VAIN	ANI0 to ANI7		0		V_{DD}	V
		ANI16 to ANI19		0		V_{DD}	V
	VBGR	Select internal reference voltage output, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

(4) When $AV_{REF} (+)$ = Internal reference voltage ($ADREFP1 = 1$, $ADREFP0 = 0$), $AV_{REF} (-)$ = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target ANI pin: ANI0 to ANI7, ANI16 to ANI19

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, Reference voltage (+) = V_{BGR} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	t _{CONV}	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 1.0	LSB
Reference voltage (+)	V_{BGR}			1.38	1.45	1.5	V
Analog input voltage	V_{AIN}			0		V_{BGR}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

2.7.6 LVD circuit characteristics

($T_A = -40$ to $+85^\circ\text{C}$, $V_{PDR} \leq V_{DD} \leq 5.5$ V, $V_{SS} = 0$ V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Detection voltage	Supply voltage level	VLVD0	Power supply rise time	3.98	4.06	4.14	V		
			Power supply fall time	3.90	3.98	4.06	V		
		VLVD1	Power supply rise time	3.68	3.75	3.82	V		
			Power supply fall time	3.60	3.67	3.74	V		
		VLVD2	Power supply rise time	3.07	3.13	3.19	V		
			Power supply fall time	3.00	3.06	3.12	V		
		VLVD3	Power supply rise time	2.96	3.02	3.08	V		
			Power supply fall time	2.90	2.96	3.02	V		
		VLVD4	Power supply rise time	2.86	2.92	2.97	V		
			Power supply fall time	2.80	2.86	2.91	V		
		VLVD5	Power supply rise time	2.76	2.81	2.87	V		
			Power supply fall time	2.70	2.75	2.81	V		
		Minimum pulse width		t _{LW}		300			μs
		Detection delay time		t _{LD}				300	μs

Remark VLVD (n - 1) > VLVDn: n = 1 to 5

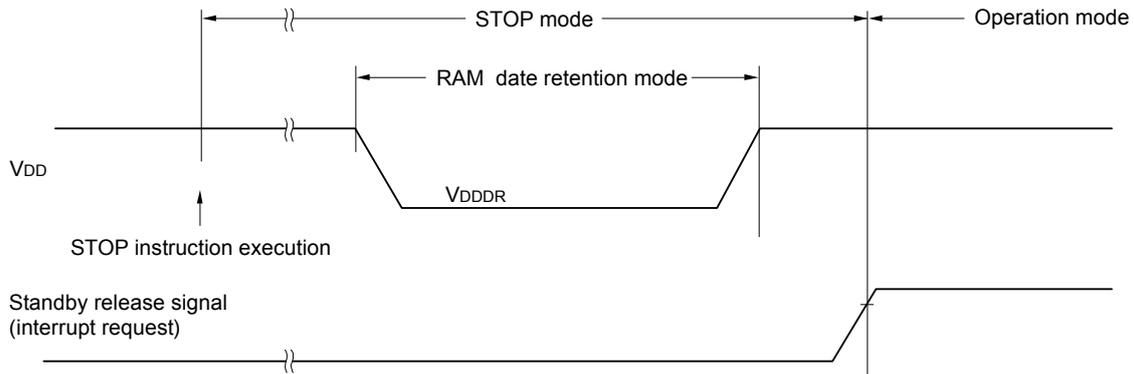
2.8 RAM Data Retention Characteristics

(TA = -40 to +85°C)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 Note		5.5	V

<R>

Note The value depends on the POR detection voltage. When the voltage drops, the data is retained before a POR reset is effected, but data is not retained when a POR reset is effected.



2.9 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU/peripheral hardware clock frequency	fCLK	2.7 V ≤ VDD ≤ 5.5 V	1		24	MHz
Number of code flash rewrites ^{Notes 1, 2, 3}	C _{erwr}	Retained for 20 years TA = 85°C ^{Note 3}	1,000			Times

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite.
The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self programming library.

Note 3. These specifications show the characteristics of the flash memory and the results obtained from Renesas Electronics reliability testing.

Remark When updating data multiple times, use the flash memory as one for updating data.

2.10 Dedicated Flash Memory Programmer Communication (UART)

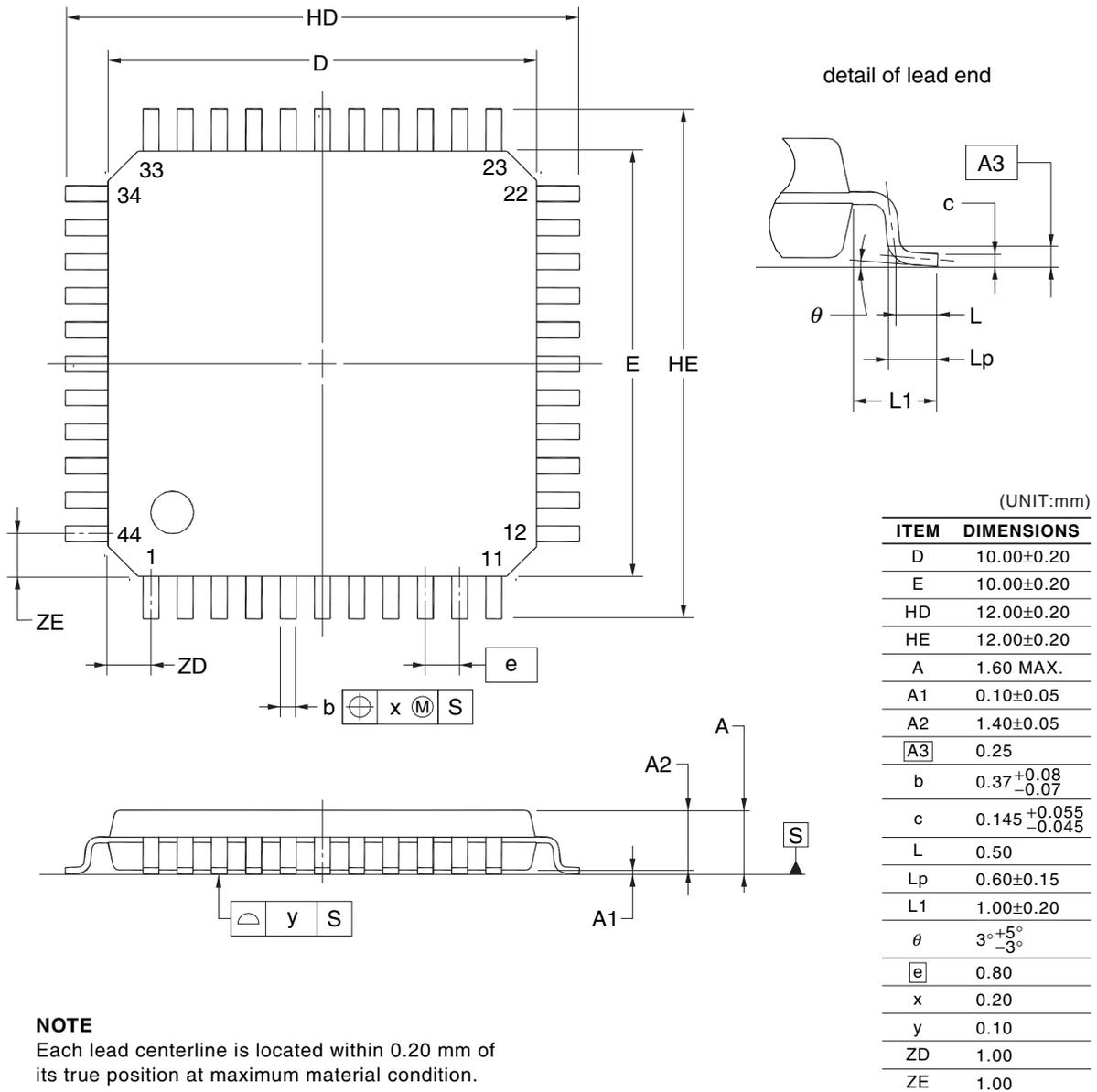
(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115.2 k		1 M	bps

3.3 44-pin Products

R5F11EF8AFP, R5F11EFAAFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



NOTE
Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.