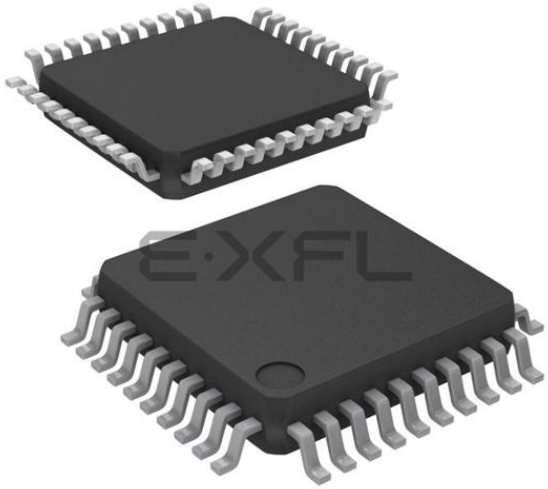
Renesas Electronics America Inc - R5F11EB8AFP#50 Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	RL78
Core Size	16-Bit
Speed	24MHz
Connectivity	CSI, I²C, UART/USART
Peripherals	LVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1.5K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	32-LQFP
Supplier Device Package	32-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f11eb8afp-50

○ ROM, RAM capacities

Flash ROM	RAM	30 pins	32 pins	44 pins
16 KB	1.5 KB Note	R5F11EAAASP	R5F11EBAAFP	R5F11EFAAFP
8 KB		R5F11EA8ASP	R5F11EB8AFP	R5F11EF8AFP

Note This is 630 bytes when the self-programming function is used.

1.2 List of Part Numbers

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G1G

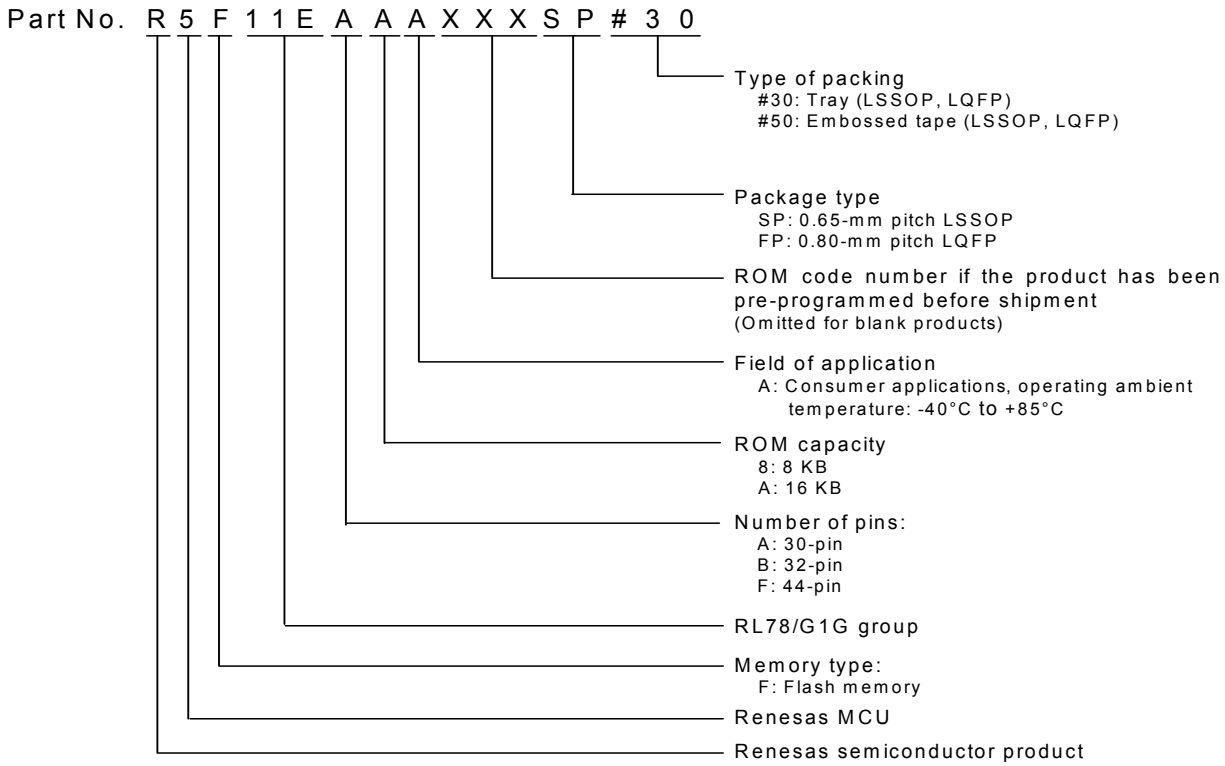


Table 1 - 1 Orderable Part Numbers

Pin Count	Package	Part Number
44 pins	44-pin plastic LQFP (10 × 10 mm)	R5F11EFAAFP#30, R5F11EFAAFP#50
		R5F11EF8AFP#30, R5F11EF8AFP#50
32 pins	32-pin plastic LQFP (7 × 7 mm)	R5F11EBAAFP#30, R5F11EBAAFP#50
		R5F11EB8AFP#30, R5F11EB8AFP#50
30 pins	30-pin plastic LSSOP (7.62 mm (300))	R5F11EAAASP#30, R5F11EAAASP#50
		R5F11EA8ASP#30, R5F11EA8ASP#50

1.4 Pin Identification

ANI0 to ANI7, ANI16 to ANI19:Analog input

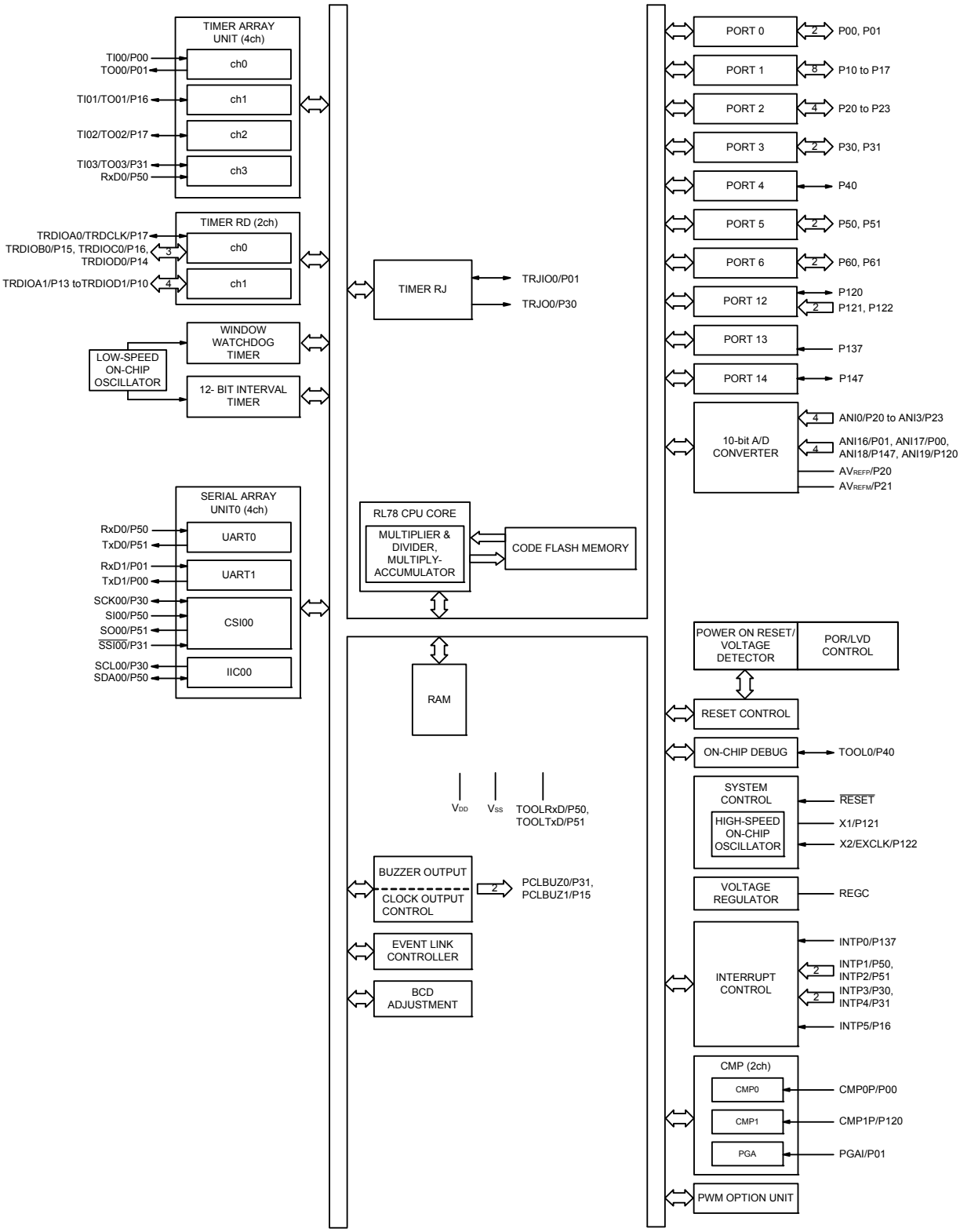
AV_{REFM}:	A/D converter reference potential (- side) input
AV_{REFP}:	A/D converter reference potential (+ side) input
EXCLK:	External clock input (main system clock)
INTP0 to INTP5:	External interrupt input
KR0 to KR3:	Key Return
P00, P01:	Port 0
P10 to P17:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40, P41:	Port 4
P50, P51:	Port 5
P60 to P63:	Port 6
P70 to P73:	Port 7
P120 to P124:	Port 12
P137:	Port 13
P146, P147:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
REGC:	Regulator capacitance
$\overline{\text{RESET}}$:	Reset
RxD0, RxD1:	Receive data
SCK00:	Serial clock input/output
SCL00:	Serial clock output
SDA00:	Serial data input/output
SI00:	Serial data input
SO00:	Serial data output
$\overline{\text{SSI00}}$:	Serial interface chip select input
TI00 to TI03:	Timer input
TO00 to TO03, TRJO0:	Timer output
TOOL0:	Data input/output for tool
TOOLRxD, TOOLTxD:	Data input/output for external device
TRDCLK:	Timer external input clock

TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0,:Timer input/output
TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1,
TRJIO0

TxD0, TxD1:	Transmit data
CMP0P, CMP1P:	Comparator input
PGAI:	PGA input
V_{DD}:	Power supply
V_{SS}:	Ground
X1, X2:	Crystal oscillator (main system clock)

1.5 Block Diagram

1.5.1 30-pin products



1.6 Outline of Functions

[30-pin, 32-pin, 44-pin products (code flash memory 8 KB to 16 KB)]

Caution The above outline of the functions applies when peripheral I/O redirection register 1 (PIOR1) is set to 00H.

(1/2)

Item		30-pin	32-pin	44-pin
		R5F11EA8ASP, R5F11EAAASP	R5F11EB8AFP, R5F11EBAAFP	R5F11EF8AFP, R5F11EFAAFP
Code flash memory (KB)		8 to 16		
RAM (KB)		1.5		
Address space		1 MB		
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 20 MHz (V_{DD} = 2.7 to 5.5 V)		
	High-speed on-chip oscillator clock (f_{IH})	LS (low-speed main) mode: 1 to 8 MHz (V_{DD} = 2.7 to 5.5 V) HS (high-speed main) mode: 1 to 24 MHz (V_{DD} = 2.7 to 5.5 V)		
Low-speed on-chip oscillator clock		15 kHz (TYP.): V_{DD} = 2.7 to 5.5 V		
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)		
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator clock: f_{IH} = 24 MHz operation)		
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)		
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.		
I/O port	Total	26	28	40
	CMOS I/O	23	25	35
	CMOS input	3	3	5
	CMOS output	—		
	N-ch open-drain I/O (6 V tolerance)	—		
Timer	16-bit timer	7 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels)		
	Watchdog timer	1 channel		
	12-bit interval timer	1 channel		
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels		

Caution Since a library is used when rewriting the flash memory using the user program, flash ROM and RAM areas are used. Refer to the RL78 Family Flash Self-Programming Library Type01 User's Manual before using these products.

(2/2)

Item		30-pin	32-pin	44-pin
		R5F11EA8ASP, R5F11EAAASP	R5F11EB8AFP, R5F11EBAAFP	R5F11EF8AFP, R5F11EFAAFP
Clock output/buzzer output		2		
		• 2.44 kHz, 4.88 kHz, 9.77 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation)		
8/10-bit resolution A/D converter		8 channels		12 channels
Comparator		2 channels		
PGA		1 channel		
Serial interface		• CSI: 1 channel/UART0: 1 channel/simplified I^2C: 1 channel • UART1: 1 channel		
Event link controller (ELC)		Event input: 18 Event trigger output: 6		Event input: 19 Event trigger output: 6
Vectored interrupt sources	Internal	20		
	External	6		7
Key interrupt		—		4
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution Note • Internal reset by RAM parity error • Internal reset by illegal-memory access		
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V		
Voltage detector		2.75 V to 4.06 V (6 stages)		
On-chip debug function		Provided		
Power supply voltage		V_{DD} = 2.7 to 5.5 V		
Operating ambient temperature		T_A = -40 to +85°C		

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -10.0 mA	V_{DD} - 1.5			V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -3.0 mA	V_{DD} - 0.7			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -2.0 mA	V_{DD} - 0.6			V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH1} = -1.0 mA	V_{DD} - 0.5			V
	V_{OH2}	P20 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OH2} = -100 μA	V_{DD} - 0.5			V
Output voltage, low	V_{OL1}	P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P73, P120, P146, P147	4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 20.0 mA			1.3	V
			4.0 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 8.5 mA			0.7	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 3.0 mA			0.6	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 1.5 mA			0.4	V
			2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL1} = 0.3 mA			0.4	V
	V_{OL2}	P20 to P27	2.7 V ≤ V_{DD} ≤ 5.5 V, I_{OL2} = 400 μA			0.4	V

Caution P00, P10, P15, P17, P30, P50, and P51 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(1) Flash ROM: 16 KB of 30-pin to 44-pin products

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD2} Note 2	HALT mode	HS (high-speed main) mode Notes 4, 6	f_{HOCO} = 48 MHz, f_{IH} = 24 MHz	V_{DD} = 5.0 V		0.60	2.40	mA
					V_{DD} = 3.0 V		0.60	2.40	
				f_{HOCO} = 24 MHz, f_{IH} = 24 MHz	V_{DD} = 5.0 V		0.40	1.83	
					V_{DD} = 3.0 V		0.40	1.83	
				f_{HOCO} = 16 MHz, f_{IH} = 16 MHz	V_{DD} = 5.0 V		0.38	1.38	
					V_{DD} = 3.0 V		0.38	1.38	
			LS (low-speed main) mode Notes 4, 6	f_{IH} = 8 MHz	V_{DD} = 3.0 V		260	710	μA
			HS (high-speed main) mode Notes 3, 6	f_{MX} = 20 MHz, V_{DD} = 5.0 V	Square wave input		0.28	1.55	mA
					Resonator connection		0.42	1.74	
				f_{MX} = 20 MHz, V_{DD} = 3.0 V	Square wave input		0.28	1.55	
					Resonator connection		0.42	1.74	
				f_{MX} = 10 MHz, V_{DD} = 5.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.27	0.93	
				f_{MX} = 10 MHz, V_{DD} = 3.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.27	0.93	
			LS (low-speed main) mode Notes 3, 6	f_{MX} = 8 MHz, V_{DD} = 3.0 V	Square wave input		95	550	μA
					Resonator connection		145	590	
	I_{DD3}	STOP mode Note 5	T_A = -40°C				0.18	0.51	μA
			T_A = +25°C				0.24	0.51	
			T_A = +50°C				0.29	1.10	
			T_A = +70°C				0.41	1.90	
			T_A = +85°C				0.90	3.30	

Note 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, comparator, programmable gain amplifier, watchdog timer, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors.

Note 2. During HALT instruction execution by flash memory.

Note 3. When high-speed on-chip oscillator is stopped.

Note 4. When high-speed system clock is stopped.

Note 5. When high-speed on-chip oscillator and high-speed system clock are stopped. When watchdog timer is stopped. The values below the MAX. column include the leakage current.

Note 6. Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high speed main) mode: V_{DD} = 2.7 V to 5.5 V@1 MHz to 24 MHz
LS (low speed main) mode: V_{DD} = 2.7 V to 5.5 V@1 MHz to 8 MHz

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (48 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (24 MHz max.)

Remark 4. Temperature condition of the TYP. value is T_A = 25°C

(2) Peripheral Functions (Common to all products)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
12-bit interval timer operating current	I_{IT} Notes 1, 8					0.02		μA
Watchdog timer operating current	I_{WDT} Notes 1, 2	f_{IL} = 15 kHz				0.22		μA
A/D converter operating current	I_{ADC} Note 3	When conversion at maximum speed	Normal mode, AV_{REFP} = V_{DD} = 5.0 V			1.3	1.7	mA
			Low voltage mode, AV_{REFP} = V_{DD} = 3.0 V			0.5	0.7	mA
A/D converter reference voltage current	I_{ADREF}					75		μA
Temperature sensor operating current	I_{TMPS}					75		μA
Comparator operating current	I_{CMP} Note 4	Per channel of comparator 1	When the comparator is operating			45.0	65.0	μA
			When the comparator is stopped			0.0	0.1	
Programmable gain amplifier operating current	I_{PGA} Note 5	When the programmable gain amplifier is operating				240.0	340.0	μA
		When the programmable gain amplifier is stopped				0.0	0.1	
LVD operating current	I_{LVI} Note 6					0.08		μA
SNOOZE operating current	I_{SNOZ}	ADC operation	The mode is performed Note 7			0.50	0.60	mA
			The A/D conversion operations are performed	Low voltage mode AV_{REFP} = V_{DD} = 3.0 V		1.20	1.44	mA
		CSI/UART operation				0.70	0.84	mA

Note 1. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 2. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontroller is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates in STOP mode.

Note 3. Current flowing only to the A/D converter. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Note 4. Current flowing only to the comparator. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{CMP} when the comparator operates in operating mode or HALT mode.

Note 5. Current flowing only to the programmable gain amplifier. The current value of the RL78 microcontroller is the sum of I_{DD1} or I_{DD2} and I_{PGA} when the programmable gain amplifier operates in operating mode or HALT mode.

Note 6. Current flowing only to the LVD circuit. The current value of the RL78 microcontroller is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{LVI} when the LVD circuit operates in the Operating, HALT or STOP mode.

Note 7. For details on the transition time to SNOOZE mode, refer to **18.3.3 SNOOZE mode in the RL78/G1G User's Manual.**

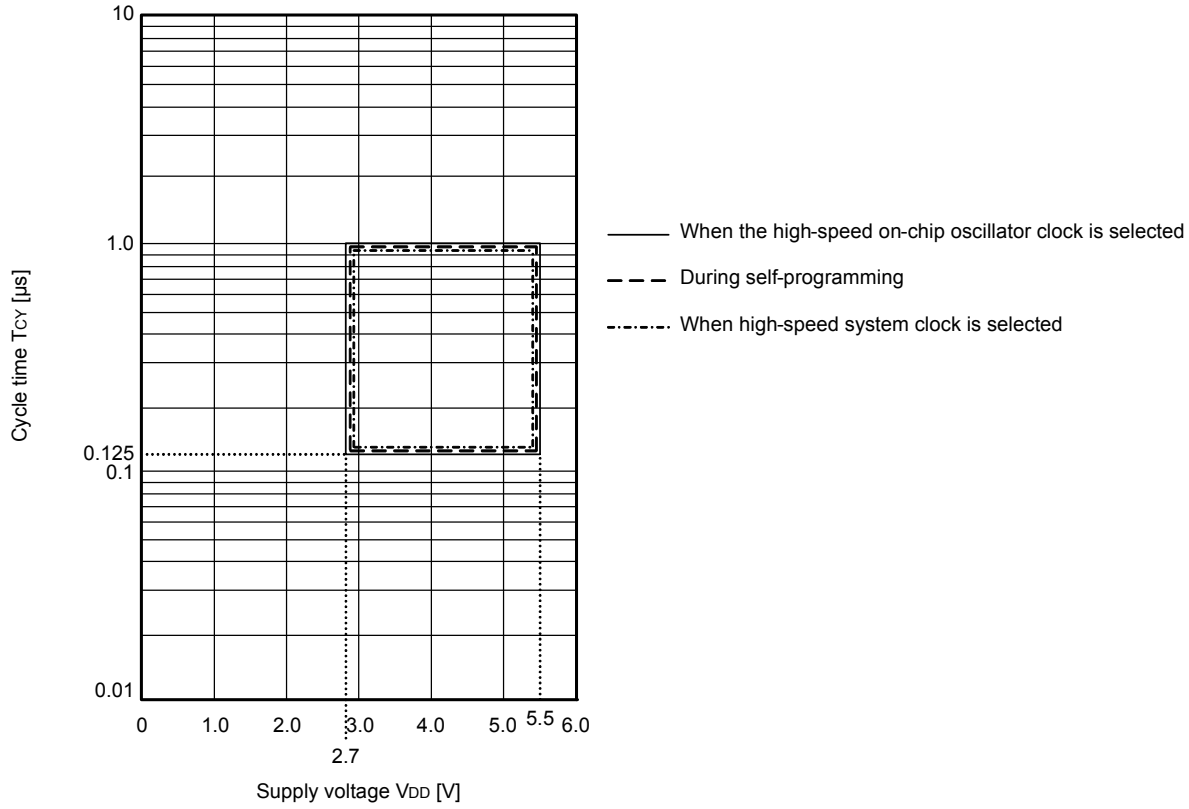
Note 8. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontroller is the sum of the values of either I_{DD1} or I_{DD2}, and I_{IT}, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, I_{FIL} should be added.

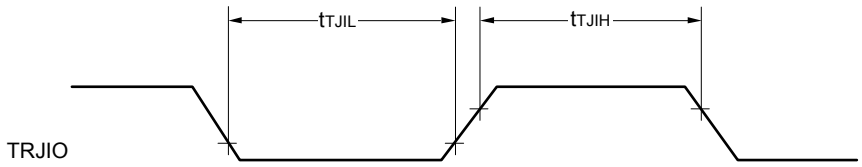
Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

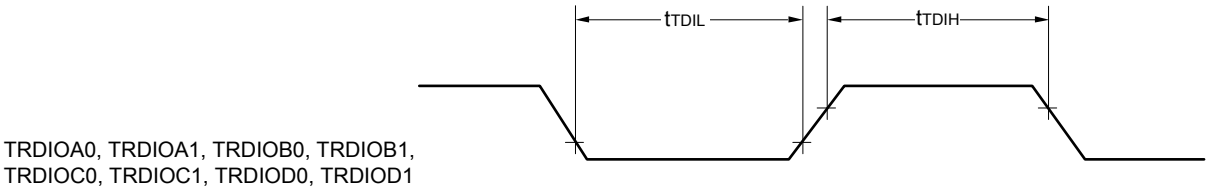
Remark 2. f_{CLK}: CPU/peripheral hardware clock frequency

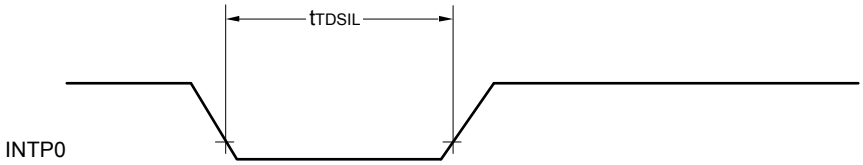
Remark 3. Temperature condition of the TYP. value is T_A = 25°C

TCY vs VDD (LS (low-speed main) mode)

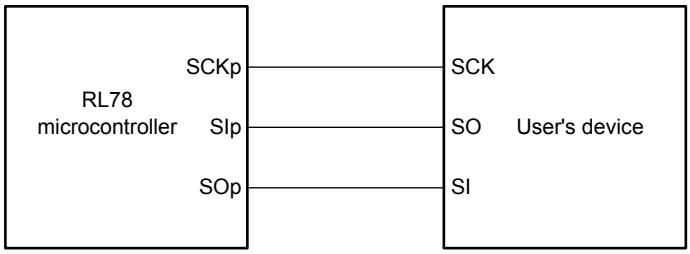



tTJIL
tTJIH
TRJIO

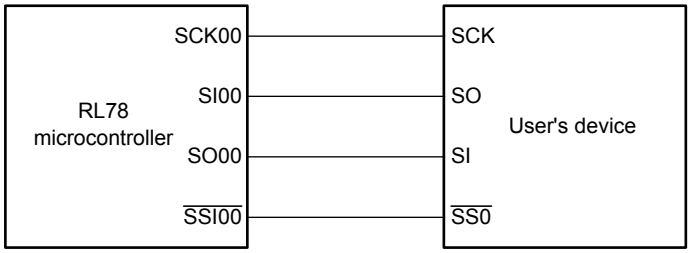

tTDIL
tTDIH
TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1,
TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1


tTDSIL
INTP0

CSI mode connection diagram (during communication at same potential)



CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))



Remark 1. p: CSI number (p = 00)
Remark 2. m: Unit number, n: Channel number (mn = 00)

(5) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ		1000 Note 1		400 Note 1	kHz
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1		400 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		ns
Hold time when SCLr = "H"	t_{HIGH}	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	475		1150		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		1150		ns
Data setup time (reception)	$t_{SU:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 85 Note 2		1/f_{MCK} + 145 Note 2		ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		1/f_{MCK} + 145 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		2.7 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	0	355	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

(Remaks are listed on the next page.)

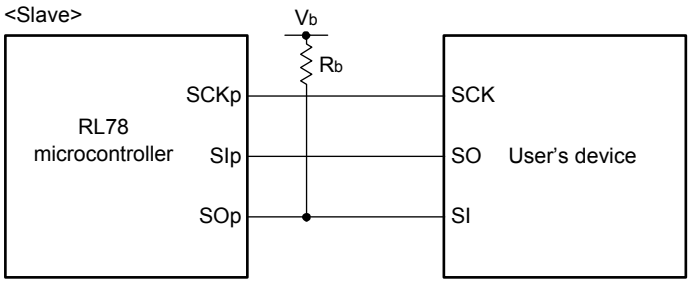
(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 2/f_{CLK}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ	200		1150		ns
			2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ	300		1150		ns
SCKp high-level width	t_{KH1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 50		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 120		t_{KCY1}/2 - 120		ns
SCKp low-level width	t_{KL1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		t_{KCY1}/2 - 7		t_{KCY1}/2 - 50		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		t_{KCY1}/2 - 10		t_{KCY1}/2 - 50		ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		58		479		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		121		479		ns
SIp hold time (from SCKp↑) Note 1	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		ns
Delay time from SCKp↓ to SOp output Note 1	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			60		60	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			130		130	ns
SIp setup time (to SCKp↓) Note 2	t_{SIK1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		23		110		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		33		110		ns
SIp hold time (from SCKp↓) Note 2	t_{KSI1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ		10		10		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	t_{KSO1}	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 20 pF, R_b = 1.4 kΩ			10		10	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V, C_b = 20 pF, R_b = 2.7 kΩ			10		10	ns

(**Notes**, **Caution** and **Remarks** are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



Note 1. Transfer rate in the SNOOZE mode: MAX. 1 Mbps

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. R_b[Ω]: Communication line (SOp) pull-up resistance, C_b[F]: Communication line (SOp) load capacitance, V_b[V]: Communication line voltage

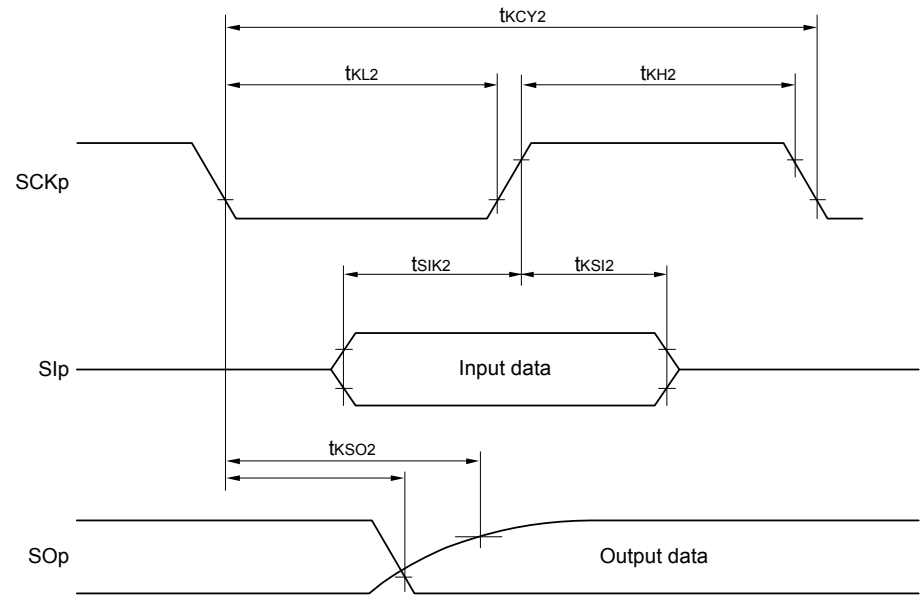
Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

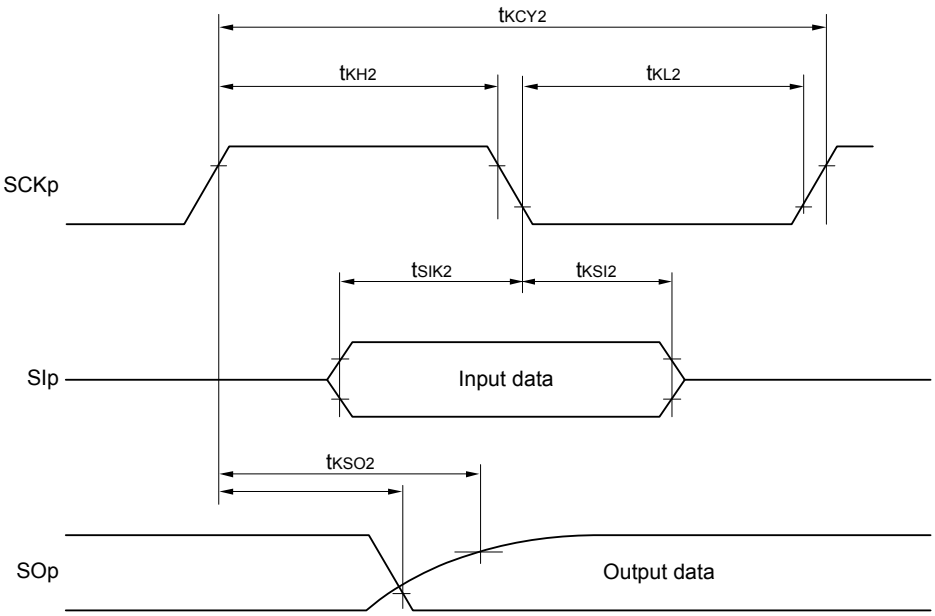
Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in CSI mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

Remark 5. Communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 2. Communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(10) Communication at different potential (2.5 V, 3 V) (simplified I^2C mode)

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V) **(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	$t_{SU:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	1/f_{MCK} + 135 Note 3		1/f_{MCK} + 190 Note 3		ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
		2.7 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b < 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	1/f_{MCK} + 190 Note 3		1/f_{MCK} + 190 Note 3		ns
Data hold time (transmission)	$t_{HD:DAT}$	4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 50 pF, R_b = 2.7 kΩ	0	305	0	305	ns
		4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V, C_b = 100 pF, R_b = 2.8 kΩ	0	355	0	355	ns
		2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b < 2.7 V, C_b = 100 pF, R_b = 2.7 kΩ	0	355	0	355	ns
		2.7 V ≤ V_{DD} < 3.3 V, 1.6 V ≤ V_b < 2.0 V Note 2, C_b = 100 pF, R_b = 5.5 kΩ	0	405	0	405	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

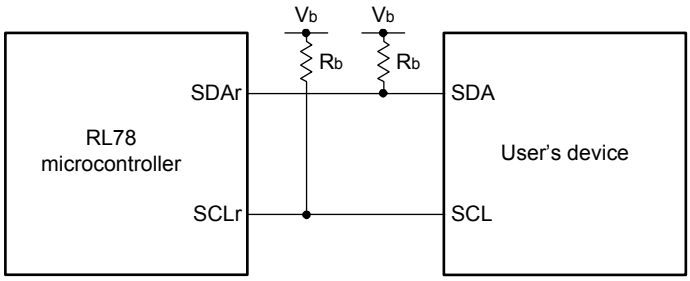
Note 2. Use it with V_{DD} ≥ V_b.

Note 3. Set the f_{MCK} value to keep the hold time of SCLr = “L” and SCLr = “H”.

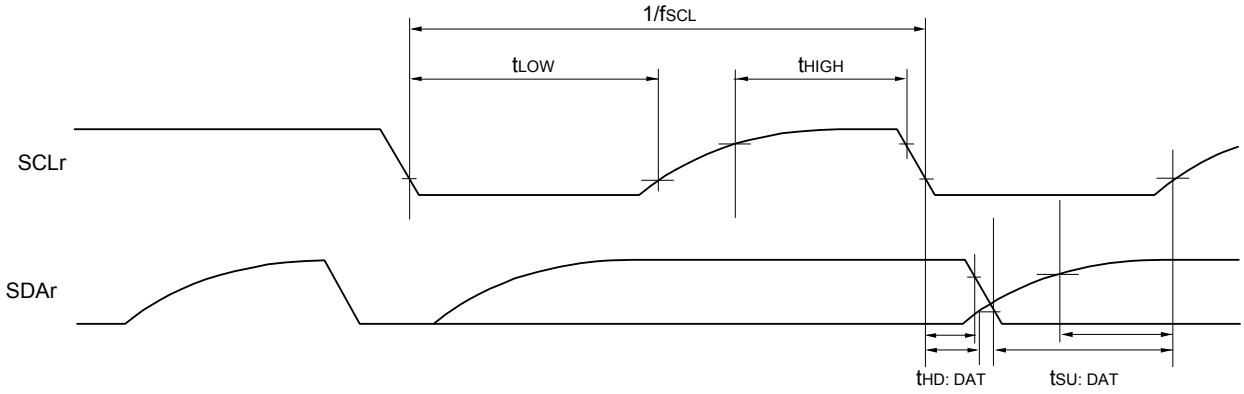
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(**Remarks** are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00), g: PIM, POM number (g = 3, 5)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0), n: Channel number (n = 0), mn = 00)

Remark 4. V_{IH} and V_{IL} below are observation points for the AC characteristics of the serial array unit when communicating at different potentials in simplified I²C mode.
4.0 V ≤ V_{DD} ≤ 5.5 V, 2.7 V ≤ V_b ≤ 4.0 V: V_{IH} = 2.2 V, V_{IL} = 0.8 V
2.7 V ≤ V_{DD} < 4.0 V, 2.3 V ≤ V_b ≤ 2.7 V: V_{IH} = 2.0 V, V_{IL} = 0.5 V

(2) When AVREF (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI16 to ANI19

(T_A = -40 to +85°C, 2.7 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AVREFP, Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V		1.2	±5.0	LSB
Conversion time	tCONV	10-bit resolution AVREFP = VDD	3.6 V ≤ VDD ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875		39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±0.35	% FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±0.35	% FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD	2.7 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Reference voltage (+)	AVREFP			2.7		VDD	V
Analog input voltage	VAIN			0		AVREFP	V
	VBGR	Select internal reference voltage output, 2.7 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode		1.38	1.45	1.5	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

(4) When AVREF (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), AVREF (-) = AVREFM/ANI1 (ADREFM = 1), target ANI pin: ANI0 to ANI7, ANI16 to ANI19

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = VBGR, Reference voltage (-) = AVREFM = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES				8		bit
Conversion time	tCONV	8-bit resolution	2.7 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error Notes 1, 2	EZS	8-bit resolution	2.7 V ≤ VDD ≤ 5.5 V			±0.60	% FSR
Integral linearity error Note 1	ILE	8-bit resolution	2.7 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error Note 1	DLE	8-bit resolution	2.7 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Reference voltage (+)	VBGR			1.38	1.45	1.5	V
Analog input voltage	VAIN			0		VBGR	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.