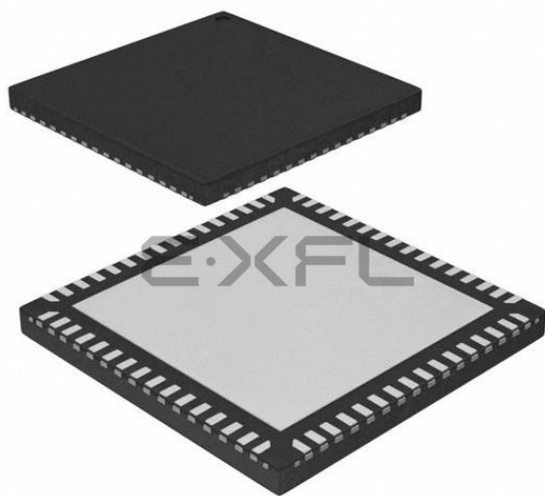




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg230f128-qfn64t

3.2.9 EFM32LG380

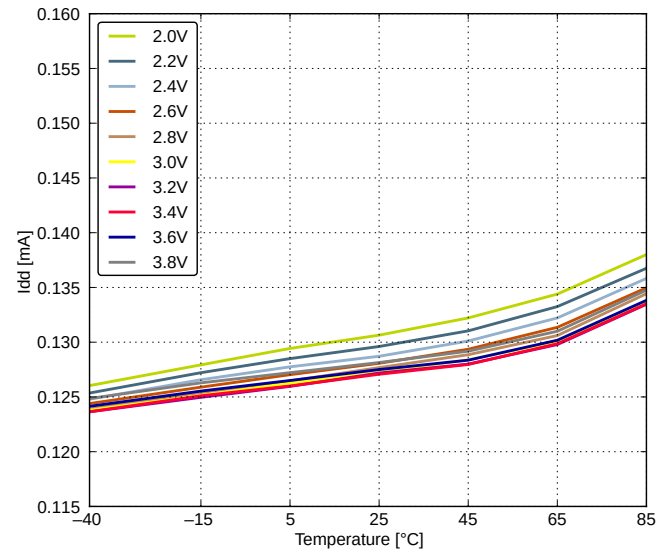
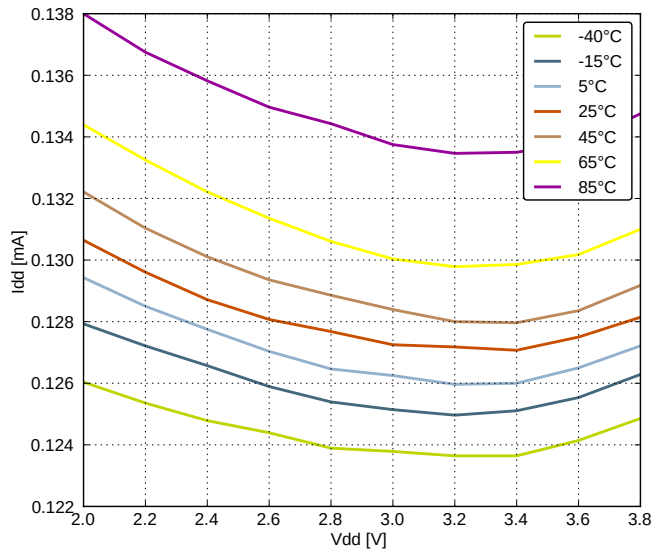
The features of the EFM32LG380 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.9. EFM32LG380 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNCR, EBI_NANDREN, EBI_NANDWEN, EBI_REN, EBI_VSNCR, EBI_WEN
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O

Module	Configuration	Pin Connections
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	50 pins	Available pins are shown in 5.19.3 GPIO Pinout Overview
LCD	Full configuration	LCD_SEG[15:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM1 current (Production test condition = 14 MHz)	I _{EM1}	48 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C	—	63	75	μA/MHz
		48 MHz HFXO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C	—	65	76	μA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C	—	64	75	μA/MHz
		28 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C	—	65	77	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C	—	65	76	μA/MHz
		21 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C	—	66	78	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C	—	67	79	μA/MHz
		14 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C	—	68	82	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C	—	68	81	μA/MHz
		11 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C	—	70	83	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C	—	74	87	μA/MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C	—	76	89	μA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =25°C	—	106	120	μA/MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V _{DD} = 3.0 V, T _{AMB} =85°C	—	112	129	μA/MHz
EM2 current	I _{EM2}	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =25°C	—	0.95 ¹	1.7 ¹	μA
		EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V _{DD} = 3.0 V, T _{AMB} =85°C	—	3.0 ¹	4.0 ¹	μA
EM3 current	I _{EM3}	V _{DD} = 3.0 V, T _{AMB} =25°C	—	0.65	1.3	μA
		V _{DD} = 3.0 V, T _{AMB} =85°C	—	2.65	4.0	μA
EM4 current	I _{EM4}	V _{DD} = 3.0 V, T _{AMB} =25°C	—	0.020	0.055	μA
		V _{DD} = 3.0 V, T _{AMB} =85°C	—	0.44	0.90	μA
Note: 1. Using backup RTC.						



4.4.2 EM2 Current Consumption

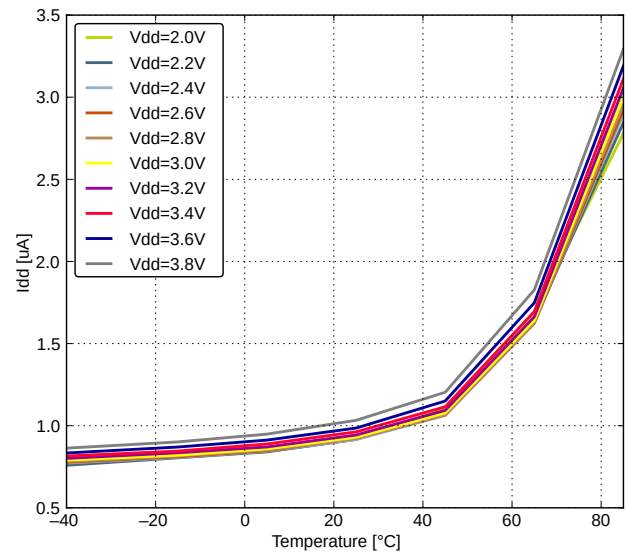
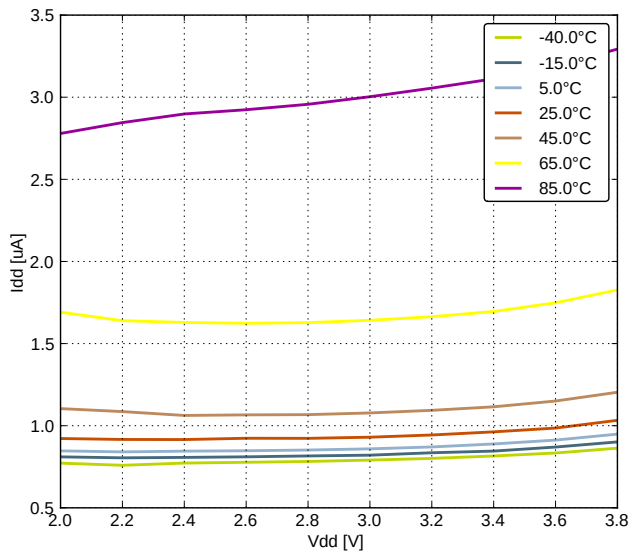


Figure 4.7. EM2 Current Consumption, RTC prescaled to 1 kHz, 32.768 kHz LFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Signal-to-Noise And Distortion-ratio (SINAD)	SINAD _{ADC}	1 MSamples/s, 12 bit, single ended, internal 1.25V reference	—	58	—	dB
		1 MSamples/s, 12 bit, single ended, internal 2.5 V reference	—	62	—	dB
		1 MSamples/s, 12 bit, single ended, VDD reference	—	64	—	dB
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference	—	60	—	dB
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference	—	64	—	dB
		1 MSamples/s, 12 bit, differential, 5 V reference	—	54	—	dB
		1 MSamples/s, 12 bit, differential, VDD reference	—	66	—	dB
		1 MSamples/s, 12 bit, differential, 2xVDD reference	—	68	—	dB
		200 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	61	—	dB
		200 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	65	—	dB
		200 kSamples/s, 12 bit, single ended, VDD reference	—	66	—	dB
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	63	—	dB
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	66	—	dB
		200 kSamples/s, 12 bit, differential, 5V reference	—	66	—	dB
Signal-to-Noise And Distortion-ratio (SINAD)	SINAD _{ADC}	200 kSamples/s, 12 bit, differential, VDD reference	62	66	—	dB
		200 kSamples/s, 12 bit, differential, 2xVDD reference	—	69	—	dB

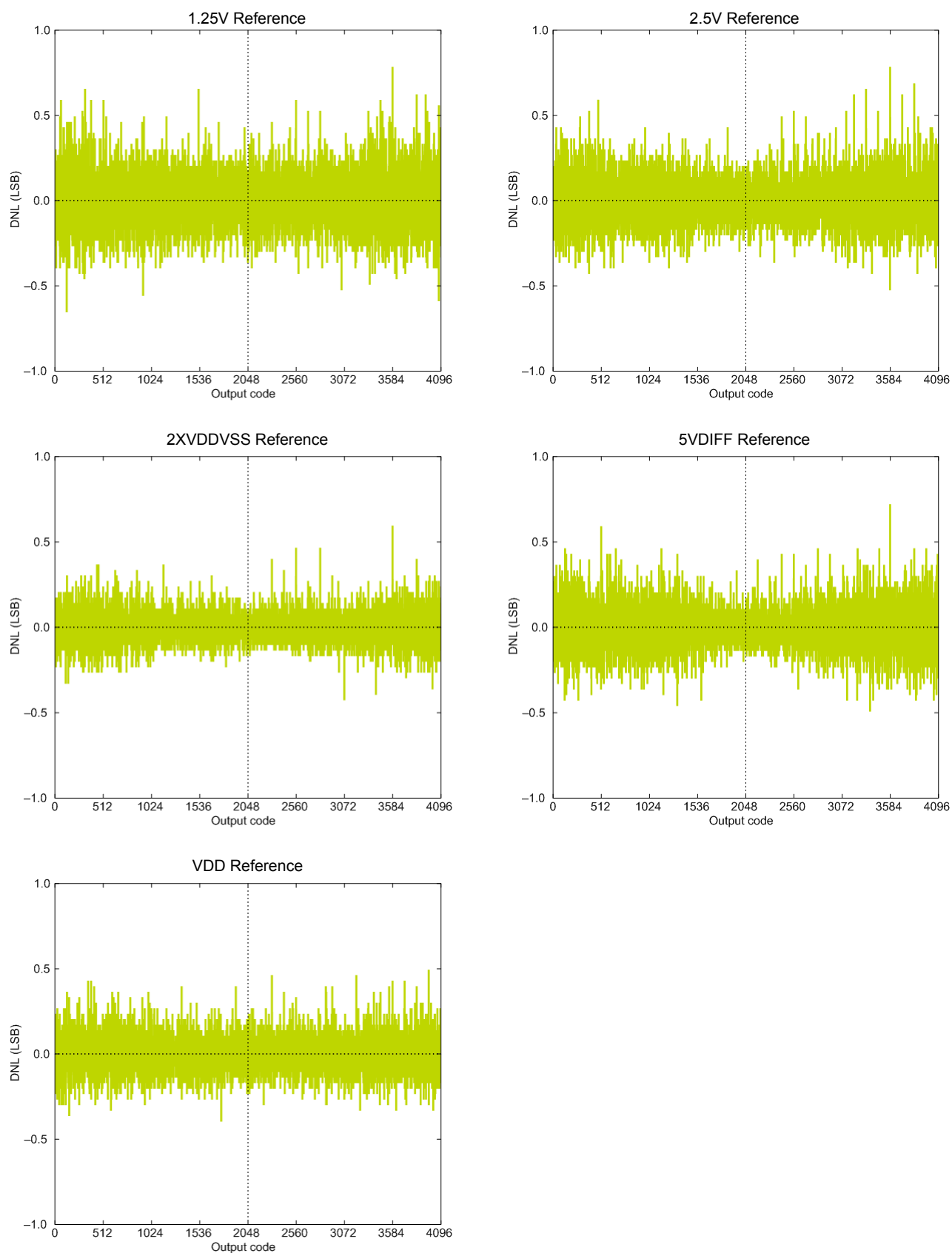


Figure 4.27. ADC Differential Linearity Error vs Code, VDD = 3 V, Temp = 25 °C

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative response time	$t_{\text{RESPONSE_N}}$	BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=0	—	353	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=1	—	547	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=2	—	578	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=3	—	627	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=4	—	670	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=5	—	741	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=6	—	811	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=7	—	926	—	ns

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Capacitive Sense Internal Resistance	R _{CSRES}	CSRESSEL=0b00 in ACMPn_INPUTSEL	—	39	—	kΩ
		CSRESSEL=0b01 in ACMPn_INPUTSEL	—	71	—	kΩ
		CSRESSEL=0b10 in ACMPn_INPUTSEL	—	104	—	kΩ
		CSRESSEL=0b11 in ACMPn_INPUTSEL	—	136	—	kΩ
Startup time	t _{ACMPSTART}		—	—	10	μs
VDD_SCALED input accuracy	V _{VDDSCALED}	VDD_SCALED=9,BIA-SPROG=0b1111, FULLBIAS=0, HALFBIAS=1, HYSTSEL=0, LPREF=0	—	-10.8	—	mV
		VDD_SCALED=9,BIA-SPROG=0b0000, FULLBIAS=0, HALFBIAS=1, HYSTSEL=0, LPREF=1	—	1.3	—	mV
Note: 1. Reference current not included.						

The total ACMP current is the sum of the contributions from the ACMP and its internal voltage reference as given in the following equation. $I_{ACMPREF}$ is zero if an external voltage reference is used.

$$I_{ACMPTOTAL} = I_{ACMP} + I_{ACMPREF}$$

Parameter	Symbol	Min	Typ	Max	Unit
SCLK to MISO	$t_{\text{SCLK_MI}}^{1\ 2}$	$-264 + t_{\text{HFFPERCLK}}$	—	$-234 + 2 \times t_{\text{HFFPERCLK}}$	ns
Note: 1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0) 2. Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})					

4.19 Digital Peripherals

Table 4.32. Digital Peripherals

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
USART current	I_{USART}	USART idle current, clock enabled	—	4.0	—	$\mu\text{A}/\text{MHz}$
UART current	I_{UART}	UART idle current, clock enabled	—	3.8	—	$\mu\text{A}/\text{MHz}$
LEUART current	I_{LEUART}	LEUART idle current, clock enabled	—	194.0	—	nA
I2C current	I_{I2C}	I2C idle current, clock enabled	—	7.6	—	$\mu\text{A}/\text{MHz}$
TIMER current	I_{TIMER}	TIMER_0 idle current, clock enabled	—	6.5	—	$\mu\text{A}/\text{MHz}$
LETIMER current	I_{LETIMER}	LETIMER idle current, clock enabled	—	85.8	—	nA
PCNT current	I_{PCNT}	PCNT idle current, clock enabled	—	91.4	—	nA
RTC current	I_{RTC}	RTC idle current, clock enabled	—	54.6	—	nA
LCD current	I_{LCD}	LCD idle current, clock enabled	—	72.7	—	nA
AES current	I_{AES}	AES idle current, clock enabled	—	1.8	—	$\mu\text{A}/\text{MHz}$
GPIO current	I_{GPIO}	GPIO idle current, clock enabled	—	3.4	—	$\mu\text{A}/\text{MHz}$
EBI current	I_{EBI}	EBI idle current, clock enabled	—	6.5	—	$\mu\text{A}/\text{MHz}$
PRS current	I_{PRS}	PRS idle current	—	3.9	—	$\mu\text{A}/\text{MHz}$
DMA current	I_{DMA}	Clock enable	—	10.9	—	$\mu\text{A}/\text{MHz}$
LE Peripheral Interface Clock current	I_{LFCLK}	Using LFXO, LFA clock tree	—	12.2	—	$\mu\text{A}/\text{MHz}$
		Using LFXO, LFB clock tree	—	4.3	—	$\mu\text{A}/\text{MHz}$

5.7.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.20. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_VIN	PD8							Battery input for Backup Power Domain

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12						I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_SEG1	PF3							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15							LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6							LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
4	PA3	-2065.0	1439.7	LCD_SEG16	EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
5	PA4	-2065.0	1307.2	LCD_SEG17	EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
6	PA5	-2065.0	1174.7	LCD_SEG18	EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	PA6	-2065.0	1042.3	LCD_SEG19	EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU 1
8	IOVDD_0	-2065.0	909.8	Digital IO power supply 0.				
9	IOVSS_0	-2065.0	630.9	Digital IO ground 0.				
10	PD14	-2065.0	550.5				I2C0_SDA #3	
11	PD15	-2065.0	451.0				I2C0_SCL #3	
12	PB0	-2065.0	352.7	LCD_SEG32	EBI_A16 #0/1/2	TIM1_CC0 #2		
13	PB1	-2065.0	249.0	LCD_SEG33	EBI_A17 #0/1/2	TIM1_CC1 #2		
14	PB2	-2065.0	107.0	LCD_SEG34	EBI_A18 #0/1/2	TIM1_CC2 #2		
15	NC	-2065.0	-40.8	Do not connect.				
16	PB3	-2065.0	-215.2	LCD_SEG20/ LCD_COM4	EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
17	PB4	-2065.0	-347.7	LCD_SEG21/ LCD_COM5	EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
18	PB5	-2065.0	-504.7	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
19	PB6	-2065.0	-612.6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
20	IOVSS_1	-2065.0	-745.0	Digital IO ground 1.				
21	IOVDD_1	-2065.0	-860.7	Digital IO power supply 1.				
22	PC0	-2065.0	-994.8	ACMP0_CH0 DAC0_OUT0ALT T #0/ OPAMP_OUT0 ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
23	PC1	-2065.0	-1098.4	ACMP0_CH1 DAC0_OUT0ALT T #1/ OPAMP_OUT0 ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
24	PC2	-2065.0	-1220.4	ACMP0_CH2 DAC0_OUT0ALT T #2/ OPAMP_OUT0 ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0

5.18.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG940 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.54. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	—	—	—	—	—	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	—	—	—	—	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	PF12	PF11	PF10	—	—	—	—	PF5	—	—	PF2	PF1	PF0

5.18.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG940 is shown in the following figure.

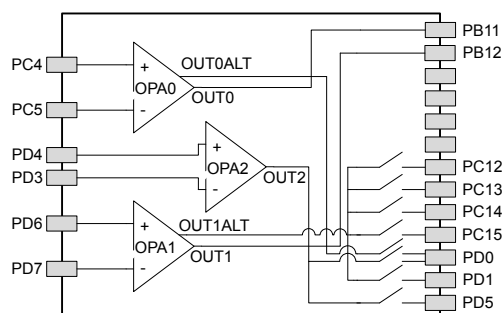


Figure 5.36. Opamp Pinout

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PA2	LCD_SEG15	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
4	PA3	LCD_SEG16	TIM0_CDTI0 #0		LES_ALTEX2 #0 ETM_TD1 #3
5	PA4	LCD_SEG17	TIM0_CDTI1 #0		LES_ALTEX3 #0 ETM_TD2 #3
6	PA5	LCD_SEG18	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	IOVDD_0	Digital IO power supply 0.			
8	VSS	Ground.			
9	PB3	LCD_SEG20/ LCD_COM4	PCNT1_S0IN #1	US2_TX #1	
10	PB4	LCD_SEG21/ LCD_COM5	PCNT1_S1IN #1	US2_RX #1	
11	PB5	LCD_SEG22/ LCD_COM6		US2_CLK #1	
12	PB6	LCD_SEG23/ LCD_COM7		US2_CS #1	
13	PC4	ACMP0_CH4 OPAMP_P0	TIM0_CDTI2 #4 LE- TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
14	PC5	ACMP0_CH5 OPAMP_N0	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
15	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
16	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
17	PA12	LCD_BCAP_P	TIM2_CC0 #1		
18	PA13	LCD_BCAP_N	TIM2_CC1 #1		
19	PA14	LCD_BEXT	TIM2_CC2 #1		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
22	VSS	Ground.			
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
25	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

6.3 BGA112 Package Marking

In the illustration below package fields and position are shown.

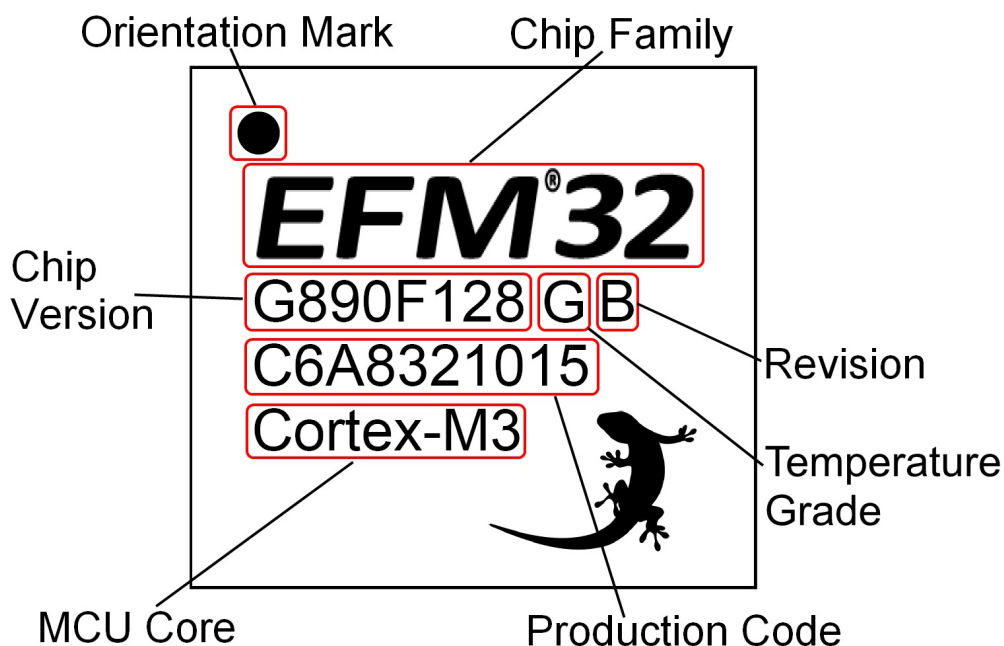


Figure 6.5. Example Chip Marking (Top View)

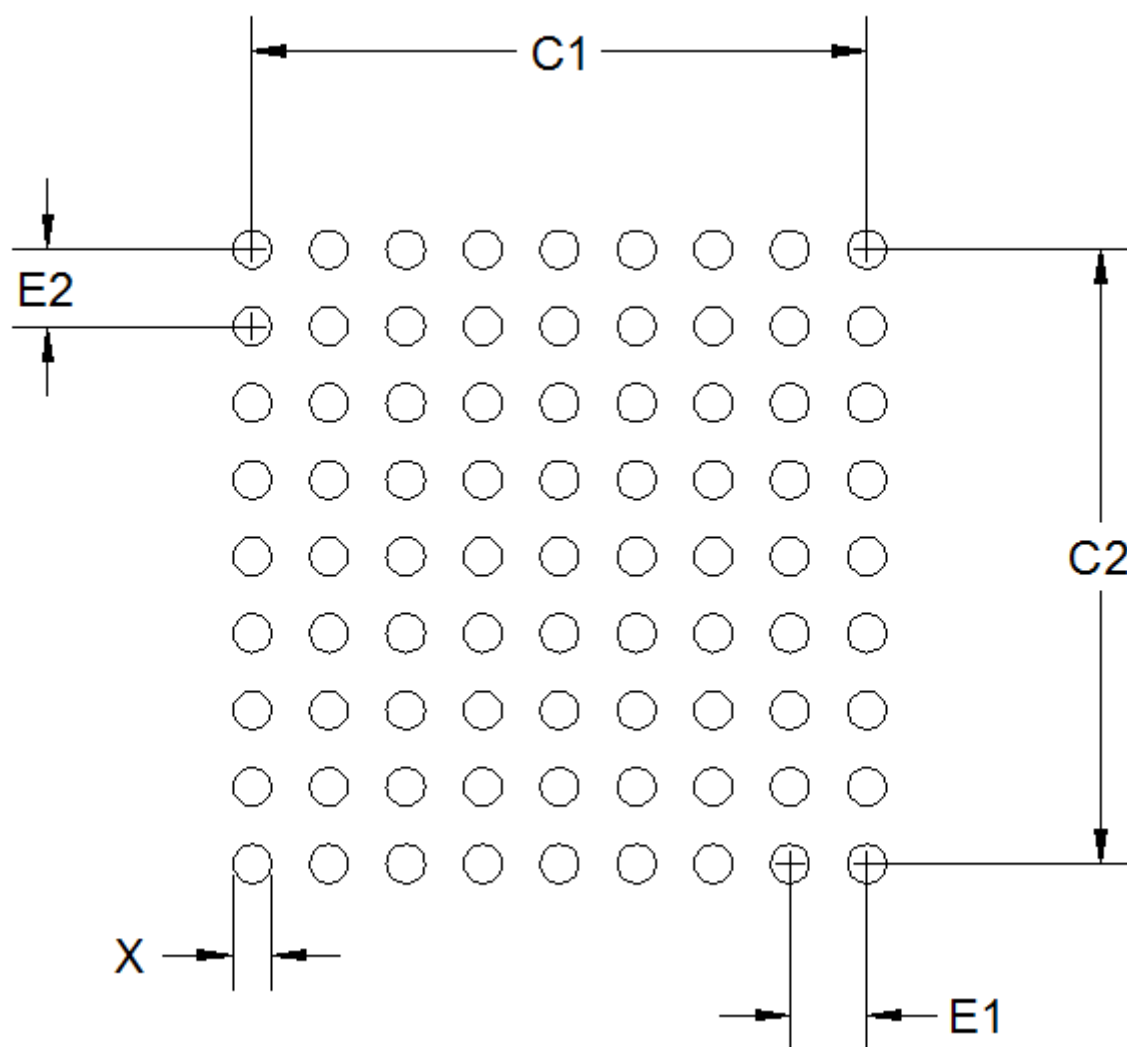


Figure 8.3. CSP81 PCB Solder Mask

Table 8.3. CSP81 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
X	0.26
C1	3.20
C2	3.20
E1	0.40
E2	0.40

11.3 QFN64 Package Marking

In the illustration below package fields and position are shown.

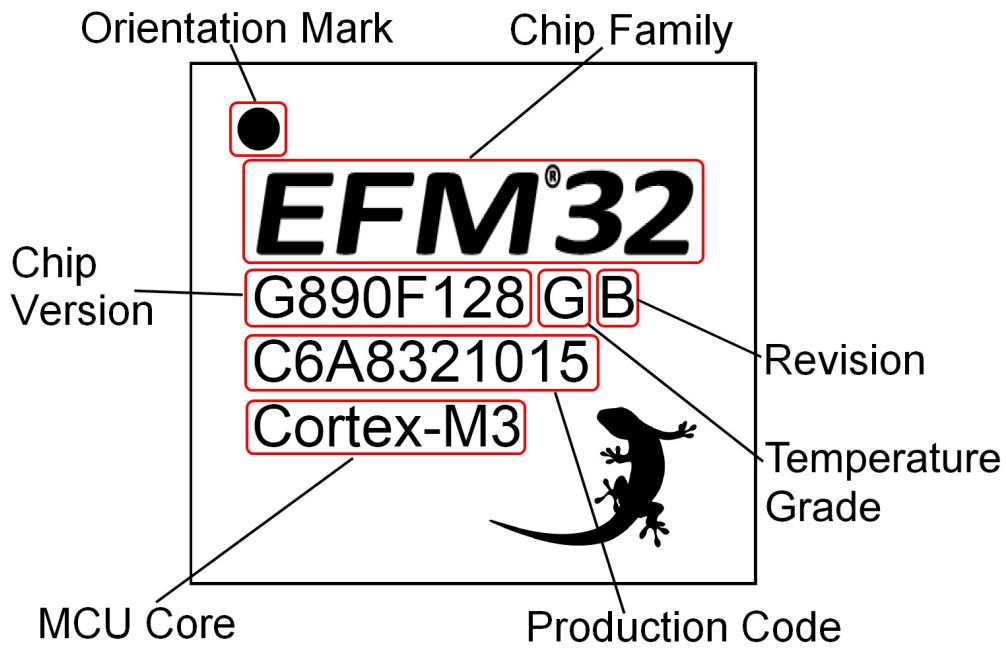


Figure 11.5. Example Chip Marking (Top View)