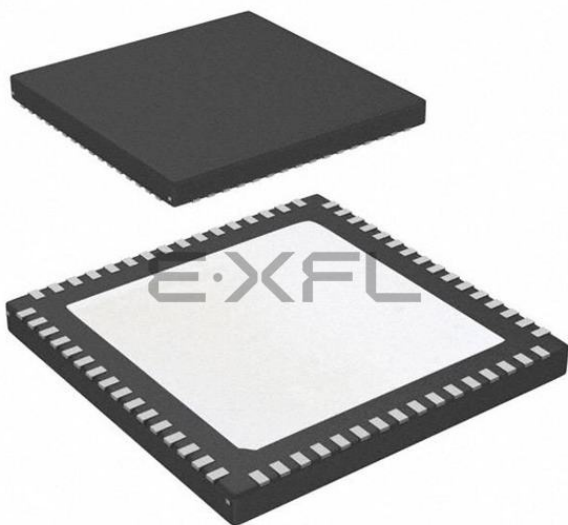




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg230f256g-e-qfn64

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3. System Summary

3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32LG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32LG devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32LG Reference Manual.

A block diagram of the EFM32LG is shown in the following figure.

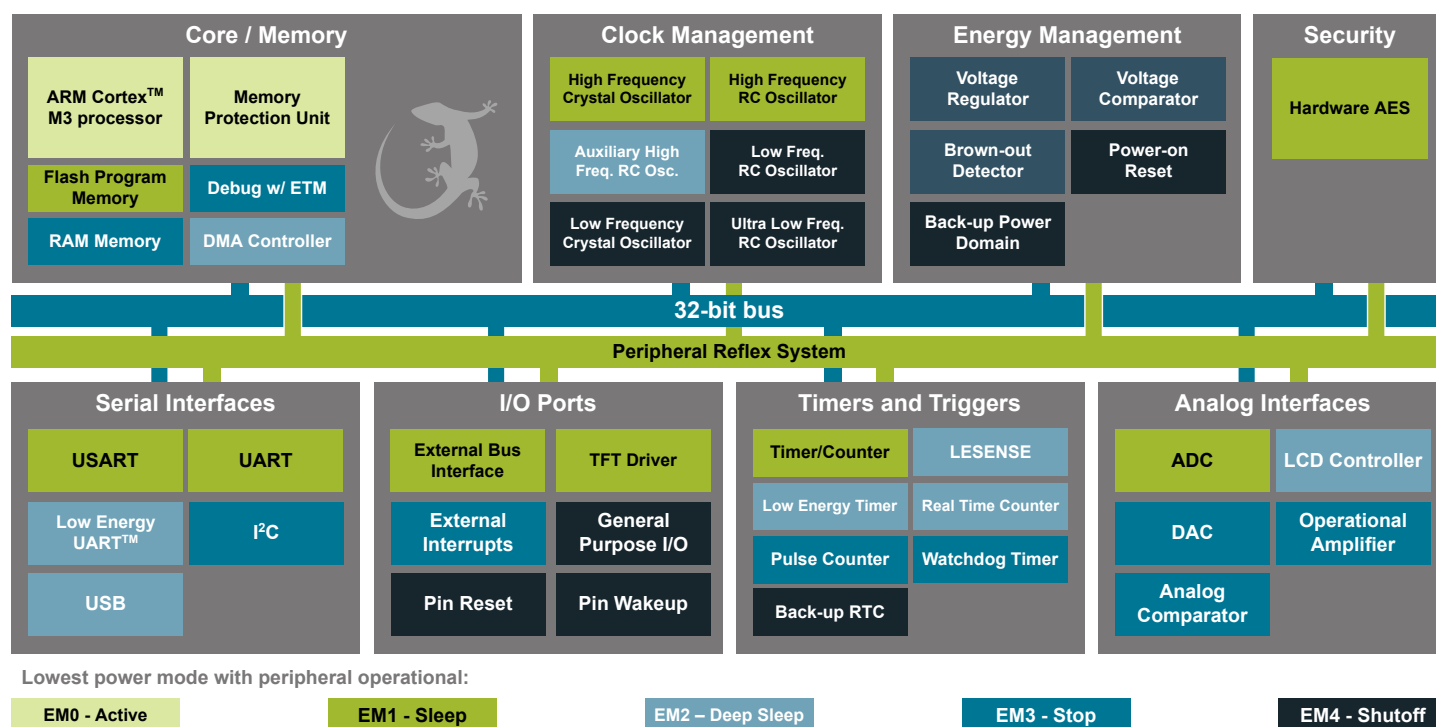


Figure 3.1. Block Diagram

3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32LG Reference Manual.

3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32LG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

Module	Configuration	Pin Connections
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	85 pins	Available pins are shown in 5.3.3 GPIO Pinout Overview

3.3 Memory Map

The EFM32LG memory map is shown in the following figure, with RAM and Flash sizes for the largest memory configuration.

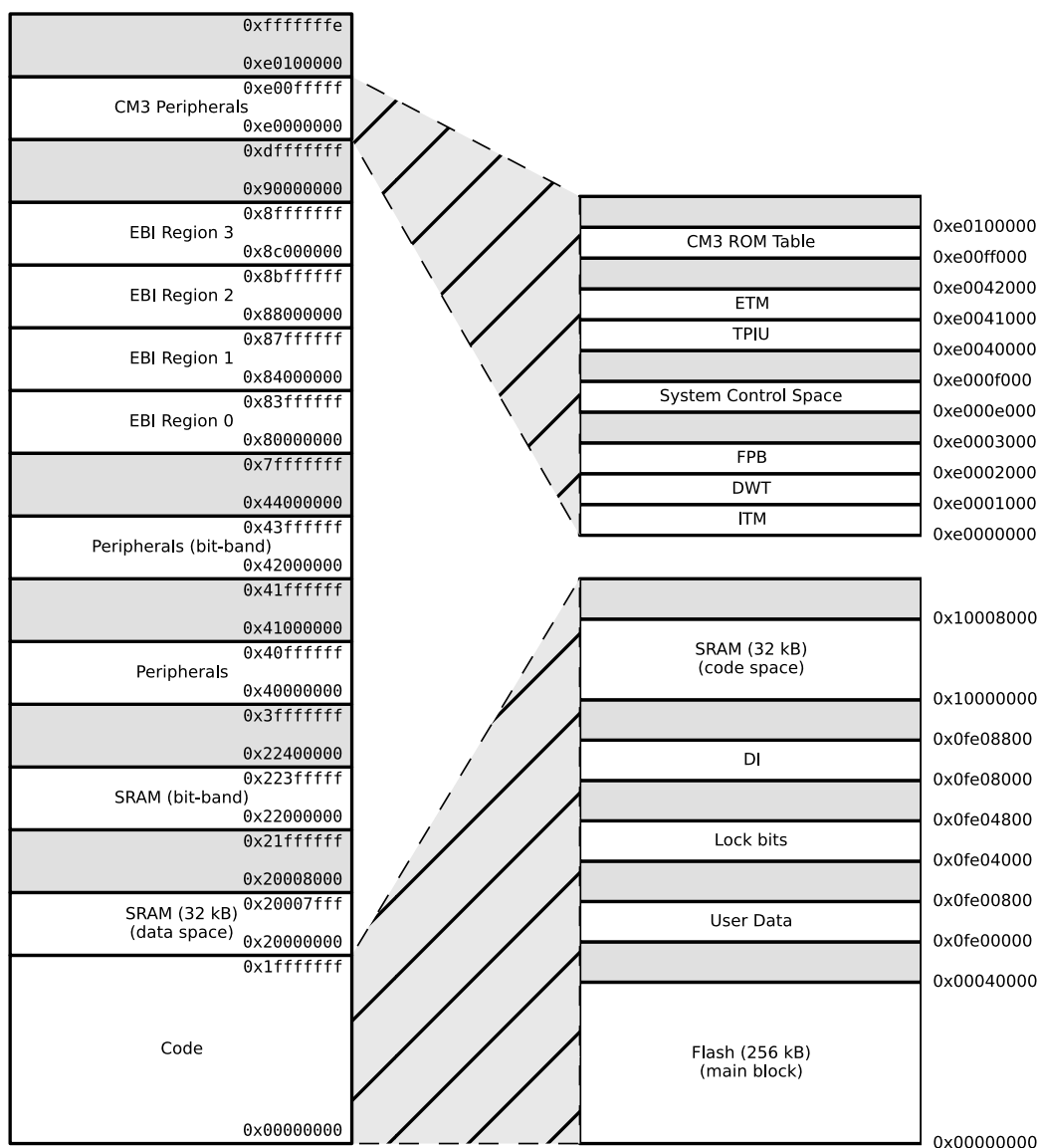


Figure 3.2. System Address Space with Core and Code Space Listing

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ADCIN}	Single ended	0	—	V_{REF}	V
		Differential	$-V_{\text{REF}}/2$	—	$V_{\text{REF}}/2$	V
Input range of external reference voltage, single ended and differential	V_{ADCREFIN}		1.25	—	V_{DD}	V
Input range of external negative reference voltage on channel 7	$V_{\text{ADCREFIN_CH7}}$	See V_{ADCREFIN}	0	—	$V_{\text{DD}} - 1.1$	V
Input range of external positive reference voltage on channel 6	$V_{\text{ADCREFIN_CH6}}$	See V_{ADCREFIN}	0.625	—	V_{DD}	V
Common mode input range	V_{ADCCMIN}		0	—	V_{DD}	V
Input current	I_{ADCIN}	2 pF sampling capacitors	—	<100	—	nA
Analog input common mode rejection ratio	CMRR_{ADC}		—	65	—	dB
Average active current	I_{ADC}	1 MSamples/s, 12 bit, external reference	—	351	—	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00	—	67	—	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01	—	63	—	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10	—	64	—	μA
Input capacitance	C_{ADCIN}		—	2	—	pF
Input ON resistance	R_{ADCIN}		1	—	—	M Ω
Input RC filter resistance	R_{ADCFILT}		—	10	—	k Ω
Input RC filter/decoupling capacitance	C_{ADCFILT}		—	250	—	fF
Input bias current	$I_{\text{ADCBIASIN}}$	$V_{\text{SS}} < V_{\text{IN}} < V_{\text{DD}}$	-40	—	40	nA
Input offset current	$I_{\text{ADCOFFSETIN}}$	$V_{\text{SS}} < V_{\text{IN}} < V_{\text{DD}}$	-40	—	40	nA
ADC Clock Frequency	f_{ADCCLK}		—	—	13	MHz
Conversion time	t_{ADCCONV}	6 bit	7	—	—	ADCCLK Cycles
		8 bit	11	—	—	ADCCLK Cycles
		12 bit	13	—	—	ADCCLK Cycles

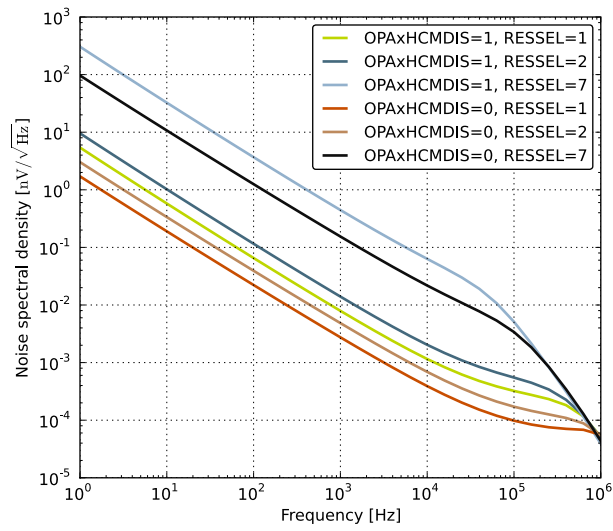


Figure 4.35. OPAMP Voltage Noise Spectral Density(Non-Unity Gain)

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
26	PA7		EBI_CSTFT #0/1/2			
27	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
28	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		
29	PA10		EBI_VSNC #0/1/2	TIM2_CC2 #0		
30	PA11		EBI_HSNC #0/1/2			
31	IOVDD_2	Digital IO power supply 2.				
32	VSS	Ground.				
33	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
34	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
35	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
36	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
37	PB9		EBI_A03 #0/1/2		U1_TX #2	
38	PB10		EBI_A04 #0/1/2		U1_RX #2	
39	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
40	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
41	AVDD_1	Analog power supply 1.				
42	PB13	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
43	PB14	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
44	IOVDD_3	Digital IO power supply 3.				
45	AVDD_0	Analog power supply 0.				
46	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
47	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
48	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
49	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
50	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
51	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
L1	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
L2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
L3	PA7		EBI_CSTFT #0/1/2			
L4	IOVDD_5	Digital IO power supply 5.				
L5	VSS	Ground.				
L6	VSS	Ground.				
L7	IOVDD_6	Digital IO power supply 6.				
L8	PB9		EBI_A03 #0/1/2		U1_TX #2	
L9	PB10		EBI_A04 #0/1/2		U1_RX #2	
L10	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
L11	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
L12	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
L13	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
M1	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
M2	PC4	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LE- TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
M3	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
M4	PA10		EBI_VSNC #0/1/2	TIM2_CC2 #0		
M5	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
M6	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
M7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
M8	AVSS_1	Analog ground 1.				
M9	AVDD_2	Analog power supply 2.				
M10	AVDD_1	Analog power supply 1.				

5.5.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.14. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12						I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.

CSP81 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
J6	AVDD_1	Analog power supply 1.			
J7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
J8	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
J9	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	

5.11 EFM32LG395 (BGA120)

5.11.1 Pinout

The EFM32LG395 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

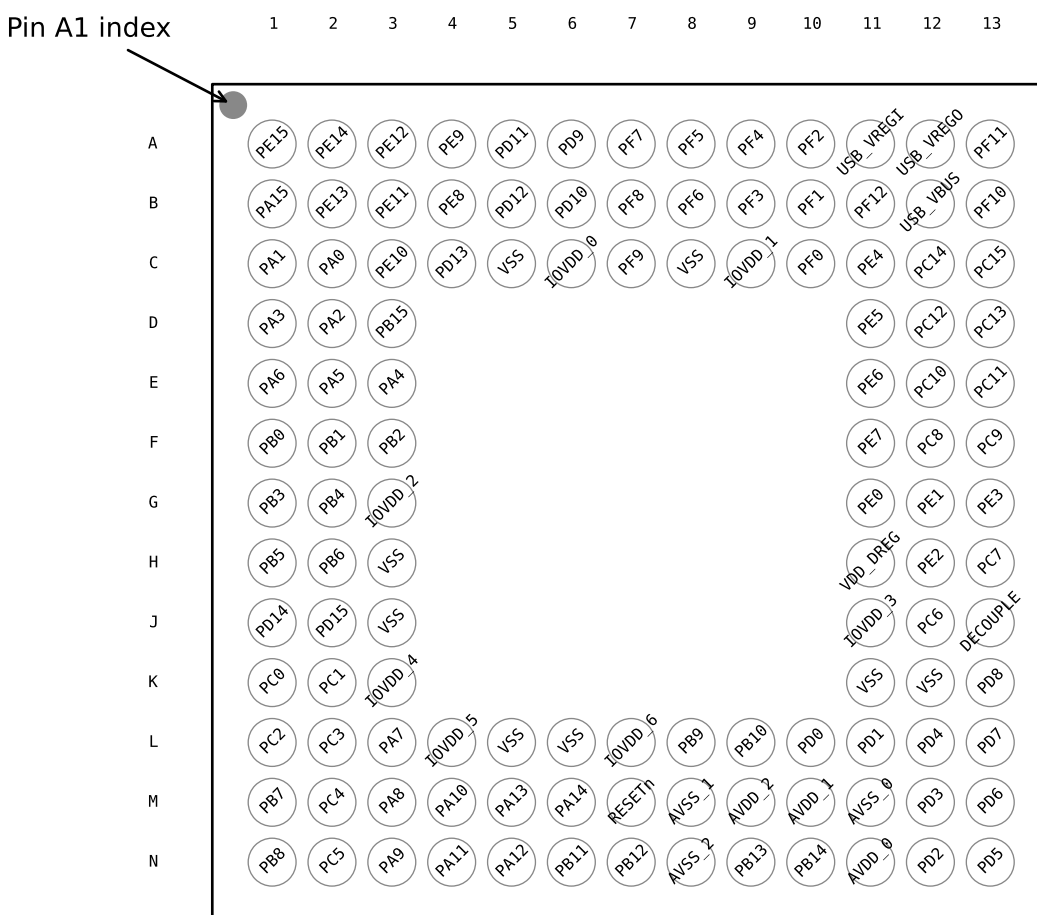


Figure 5.21. EFM32LG395 Pinout (top view, not to scale)

Table 5.31. Device Pinout

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15		EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
A2	PE14		EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7							LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13			PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14			PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3		PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2		PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3		PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13		PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14		PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12						Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13						Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14						Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
US0_CLK	PE12	PE5		PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4		PC14	PB14	PB14		USART0 chip select input / output.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE		PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNCR	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREN	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEN	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REN	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNCR	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEN		PF8						External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4					UART0 Receive input.
U0_TX	PF6	PE0	PA3					UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX		PF11	PB10	PE3				UART1 Receive input.
U1_TX		PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.21.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG990 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.63. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	—	—	—	—	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	—	—	PF2	PF1	PF0

5.21.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG990 is shown in the following figure.

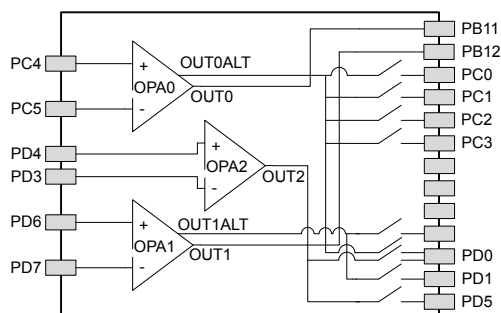


Figure 5.42. Opamp Pinout

Symbol	Dim. (mm)
c	0.50
d	15.40
e	15.40

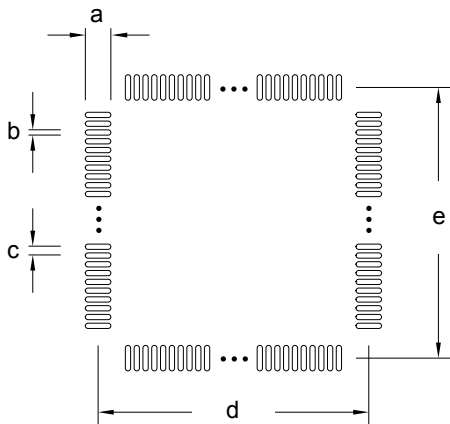


Figure 9.4. LQFP100 PCB Stencil Design

Table 9.4. LQFP100 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	1.35
b	0.20
c	0.50
d	15.40
e	15.40

- Note:**
- 1. The drawings are not to scale.
 - 2. All dimensions are in millimeters.
 - 3. All drawings are subject to change without notice.
 - 4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
 - 5. Stencil thickness 0.125 mm.
 - 6. For detailed pin-positioning, see Pin Definitions.

14.7 Revision 1.10

June 28th, 2013

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Updated power requirements in the Power Management section.

For BGA packages, updated PCB Land Pattern, PCB Solder Mask and PCB Stencil Design figures.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

This revision applies the following devices:

- EFM32LG900

December 12th, 2014

Added recommendation to use gold bond wire.