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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg232f128g-e-qfp64r

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Module	Configuration	Pin Connections
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	83 pins	Available pins are shown in 5.9.3 GPIO Pinout Overview

3.2.15 EFM32LG890

The features of the EFM32LG890 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.15. EFM32LG890 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNCR, EBI_NANDREN, EBI_NANDWEN, EBI_REn, EBI_VSNCR, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	48 MHz HFXO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	211	225	$\mu\text{A}/\text{MHz}$
		48 MHz HFXO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	211	230	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	212	220	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	213	223	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	214	224	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	215	226	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	216	231	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	217	237	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	218	239	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	219	239	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	224	245	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	224	258	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	257	285	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	261	293	$\mu\text{A}/\text{MHz}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range (SFDR)	SFDR _{ADC}	1 MSamples/s, 12 bit, single ended, internal 1.25 V reference	—	64	—	dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5 V reference	—	76	—	dBc
		1 MSamples/s, 12 bit, single ended, VDD reference	—	73	—	dBc
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference	—	66	—	dBc
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference	—	77	—	dBc
		1 MSamples/s, 12 bit, differential, VDD reference	—	76	—	dBc
		1 MSamples/s, 12 bit, differential, 2xVDD reference	—	75	—	dBc
		1 MSamples/s, 12 bit, differential, 5 V reference	—	69	—	dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	75	—	dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	75	—	dBc
		200 kSamples/s, 12 bit, single ended, VDD reference	—	76	—	dBc
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, 5 V reference	—	78	—	dBc
Spurious-Free Dynamic Range (SFDR)	SFDR _{ADC}	200 kSamples/s, 12 bit, differential, VDD reference	68	79	—	dBc
		200 kSamples/s, 12 bit, differential, 2xVDD reference	—	79	—	dBc
Offset voltage	V _{ADCOFFSET}	After calibration, single ended	-3.5	0.3	3	mV
		After calibration, differential	—	0.3	—	mV
Thermometer output gradient	TGRAD _{ADCTH}		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes/°C
Differential non-linearity (DNL)	DNL _{ADC}		-1	±0.7	4	LSB
Integral non-linearity (INL), End point method	INL _{ADC}		—	±1.2	±3	LSB
Missing codes	MC _{ADC}		11.999 ¹	12	—	bits
Gain error drift	GAIN _{ED}	1.25 V reference	—	0.01 ²	0.033 ³	%/°C
		2.5 V reference	—	0.01 ²	0.03 ³	%/°C

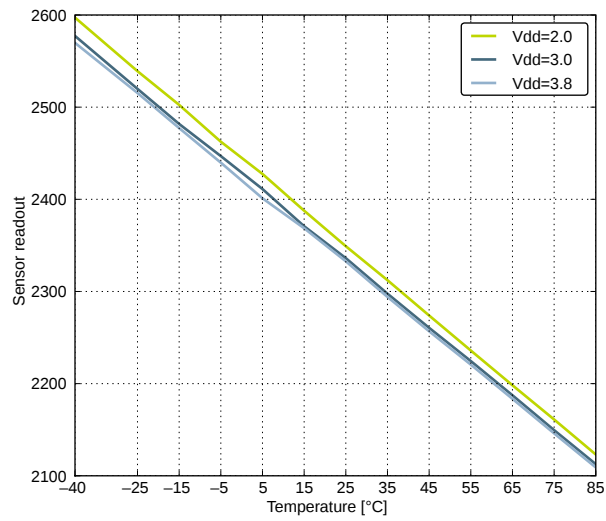


Figure 4.30. ADC Temperature Sensor Readout

4.13 Analog Comparator (ACMP)

Table 4.17. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}		0	—	V_{DD}	V
Input bias current	$I_{ACMPBIASIN}$	$V_{SS} < V_{IN} < V_{DD}$	-40	—	40	nA
Input offset current	$I_{ACMPOFFSETIN}$	$V_{SS} < V_{IN} < V_{DD}$	-40	—	40	nA
ACMP Common Mode voltage range	V_{ACMPCM}		0	—	V_{DD}	V
Active current	I_{ACMP}	BIASPROG=0b0000, FULL-BIAS=0 and HALFBIAS=1 in ACMPn_CTRL register	—	0.1 ¹	0.4 ¹	μA
		BIASPROG=0b1111, FULL-BIAS= 0 and HALFBIAS=0 in ACMPn_CTRL register	—	2.87 ¹	15 ¹	μA
		BIASPROG=0b1111, FULL-BIAS= 1 and HALFBIAS=0 in ACMPn_CTRL register	—	195 ¹	520 ¹	μA
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1 in ACMPn_CTRL register	—	0.8 ¹	2.2 ¹	μA
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1 in-ACMPn_CTRL register	—	2.7 ¹	8.1 ¹	μA
Current consumption of internal voltage reference	$I_{ACMPREF}$	Internal voltage reference off. Using external voltage reference	—	0	—	μA
		Internal voltage reference	—	5	—	μA

4.14 Voltage Comparator (VCMP)

Table 4.18. VCMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V _{VCMPIN}		—	V _{DD}	—	V
VCMP Common Mode voltage range	V _{VCMPCM}		—	V _{DD}	—	V
Active current	I _{VCMP}	BIASPROG=0b0000 and HALF-BIAS=1 in VCMPn_CTRL register	—	0.3 ¹	0.6 ¹	μA
		BIASPROG=0b1111 and HALF-BIAS=0 in VCMPn_CTRL register. LPREF=0.	—	22 ¹	35 ¹	μA
Startup time reference generator	t _{VCMPREF}	NORMAL	—	10	—	μs
Offset voltage	V _{VCMPOFFSET}	Single ended	—	10	—	mV
		Differential	—	10	—	mV
Negative hysteresis	V _{VCMPHYST_N}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1	-46.6	-15.6	11.4	mV
Positive hysteresis	V _{VCMPHYST_P}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1	-7.5	23.4	46.6	mV
Hysteresis delta	V _{VCMPHYST_DELTA}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1	4.2	35.2	70.0	mV
Startup time	t _{VCMPSTART}		—	—	10	μs
Negative response time	t _{RESPONSE_N}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1, HYS-TSEL=0	—	372.3	—	μs
Positive response time	t _{RESPONSE_P}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1, HYS-TSEL=0	—	865.7	—	μs
Note: 1. Includes required contribution from the voltage reference.						

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL}$$

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.4.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG290 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.12. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

5.4.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG290 is shown in the following figure.

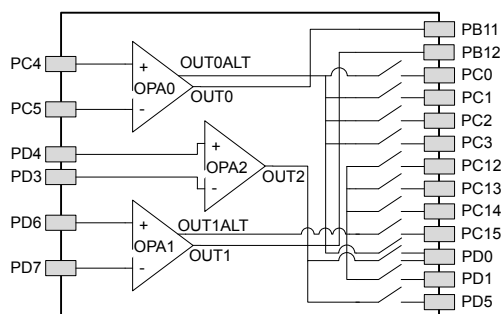


Figure 5.8. Opamp Pinout

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A3	PE12		EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
A4	PE9		EBI_AD01 #0/1/2	PCNT2_S1IN #1		
A5	PD11		EBI_CS2 #0/1/2			
A6	PD9		EBI_CS0 #0/1/2			
A7	PF7		EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
A8	PF5		EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
A9	PF4		EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
A10	PF2		EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
A11	USB_VREGI					
A12	USB_VREGO					
A13	PF11				U1_RX #1	
B1	PA15		EBI_AD08 #0/1/2	TIM3_CC2 #0		
B2	PE13		EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B3	PE11		EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
B4	PE8		EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
B5	PD12		EBI_CS3 #0/1/2			
B6	PD10		EBI_CS1 #0/1/2			
B7	PF8		EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
B8	PF6		EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
B9	PF3		EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
B10	PF1			TIM0_CC1 #5 LE- TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
B11	PF12					
B12	USB_VBUS	USB 5.0 V VBUS input.				
B13	PF10				U1_TX #1	
C1	PA1		EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C2	PA0		EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
C3	PE10		EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					ETM_TD1 #1

CSP81 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D1	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
D2	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0
D3	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT		U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
D4	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
D5	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
D6	PA4		TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
D7	PA5		TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
D8	PA6			LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
D9	IOVDD_0	Digital IO power supply 0.			
E1	PE4			US0_CS #1	
E2	PE5			US0_CLK #1	
E3	PE3	BU_STAT		U1_RX #3	ACMP1_O #1
E4	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
E5	PE15		TIM3_CC1 #0	LEU0_RX #2	
E6	PB5			US2_CLK #1	
E7	PB3		PCNT1_S0IN #1	US2_TX #1	
E8	PB4		PCNT1_S1IN #1	US2_RX #1	
E9	VSS	Ground.			
F1	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C^{DECOUPLE}$ is required at this pin.			
F2	PE2	BU_VOUT	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
F3	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
F4	PD7	ADC0_CH7 OPAMP_N1	TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
F5	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
F6	PA8		TIM2_CC0 #0		
F7	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.8.3 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG360 is shown in the following figure.

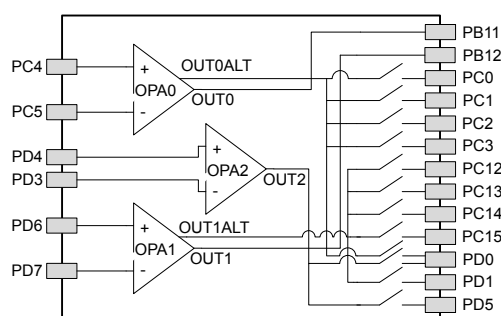


Figure 5.16. Opamp Pinout

5.8.4 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG360 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.24. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	-	-	-	-	PA10	PA9	PA8	-	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	PB12	PB11	-	-	PB8	PB7	PB6	PB5	PB4	PB3	-	-	-
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	-	-	PE5	PE4	PE3	PE2	-	-
Port F	-	-	-	PF12	PF11	PF10	-	-	-	-	PF5	-	-	PF2	PF1	PF0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
U0_RX	PF7	PE1	PA4					UART0 Receive input.
U0_TX	PF6	PE0	PA3					UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX		PF11	PB10	PE3				UART1 Receive input.
U1_TX		PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
74	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
75	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
76	PF0			TIM0_CC0 #5 LE- TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
77	PF1			TIM0_CC1 #5 LE- TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
78	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
79	PF3	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
80	PF4	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
81	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
82	IOVDD_5	Digital IO power supply 5.				
83	VSS	Ground.				
84	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
85	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
86	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
87	PF9	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
88	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
89	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
90	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
91	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
92	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
93	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
94	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
95	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
96	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
97	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
98	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
114	PD11	-313.8	2065.0	LCD_SEG30	EBI_CS2 #0/1/2			
115	PD12	-426.2	2065.0	LCD_SEG31	EBI_CS3 #0/1/2			
116	PD13	-534.7	2065.0					ETM_TD1 #1
117	PD15	-644.6	2065.0					ETM_TD2 #1
118	PE8	-745.8	2065.0	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
119	PE9	-867.9	2065.0	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
120	PE10	-976.1	2065.0	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
121	PE11	-1085.3	2065.0	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
122	IOVDD_6	-1196.1	2065.0	Digital IO power supply 6.				
123	IOVSS_6	-1289.0	2065.0	Digital IO ground 6.				
124	PE12	-1385.4	2065.0	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
125	PE13	-1518.2	2065.0	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU 5
126	PE14	-1626.4	2065.0	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
127	PE15	-1729.6	2065.0	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
128	PA15	-1844.0	2065.0	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
F11	PE7	LCD_COM3	EBI_A14 #0/1/2		US0_TX #1	
F12	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
F13	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
G1	PB3	LCD_SEG20/ LCD_COM4	EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
G2	PB4	LCD_SEG21/ LCD_COM5	EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
G3	IOVDD_2	Digital IO power supply 2.				
G11	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
G12	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
G13	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
H1	PB5	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
H2	PB6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
H3	VSS	Ground.				
H11	VDD_DREG	Power supply for on-chip voltage regulator.				
H12	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
H13	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
J1	PD14				I2C0_SDA #3	
J2	PD15				I2C0_SCL #3	
J3	VSS	Ground.				
J11	IOVDD_3	Digital IO power supply 3.				
J12	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
J13	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
K1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
K2	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
K3	IOVDD_4	Digital IO power supply 4.				
K11	VSS	Ground.				
K12	VSS	Ground.				

6.2 BGA112 PCB Layout

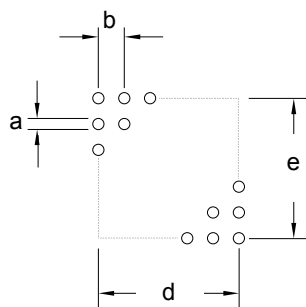


Figure 6.2. BGA112 PCB Land Pattern

Table 6.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.35
b	0.80
d	8.00
e	8.00

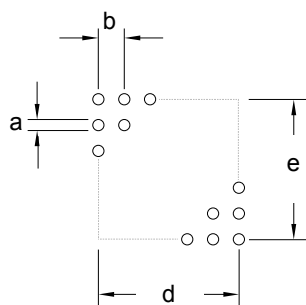


Figure 6.3. BGA112 PCB Solder Mask

Table 6.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.48
b	0.80
d	8.00
e	8.00

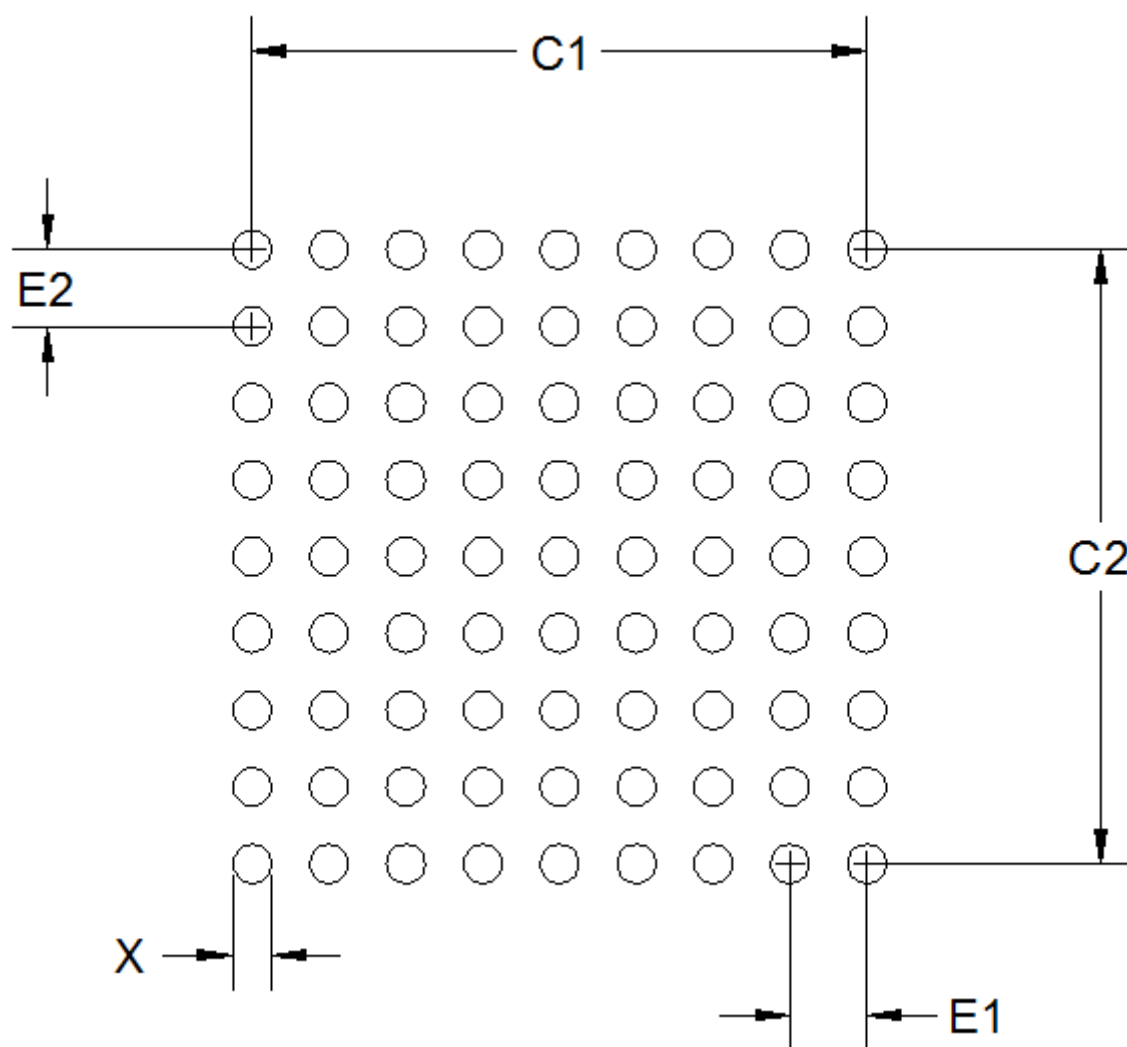


Figure 8.3. CSP81 PCB Solder Mask

Table 8.3. CSP81 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
X	0.26
C1	3.20
C2	3.20
E1	0.40
E2	0.40