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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	86
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg280f64-qfp100

Module	Configuration	Pin Connections
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	65 pins	Available pins are shown in 5.8.4 GPIO Pinout Overview

4.7 Flash

Table 4.6. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC_{FLASH}		20000	—	—	cycles
Flash data retention	RET_{FLASH}	T_{AMB}<150 °C	10000	—	—	h
		T_{AMB}<85 °C	10	—	—	years
		T_{AMB}<70 °C	20	—	—	years
Word (32-bit) programming time	t_{W_PROG}		20	—	—	µs
Page erase time	t_{PERASE}		20	20.4	20.8	ms
Device erase time	t_{DERASE}		40	40.8	41.6	ms
Erase current	I_{ERASE}		—	—	7[1]	mA
Write current	I_{WRITE}		—	—	7[1]	mA
Supply voltage during flash erase and write	V_{FLASH}		1.98	—	3.8	V

Note:
1. Measured at 25 °C.

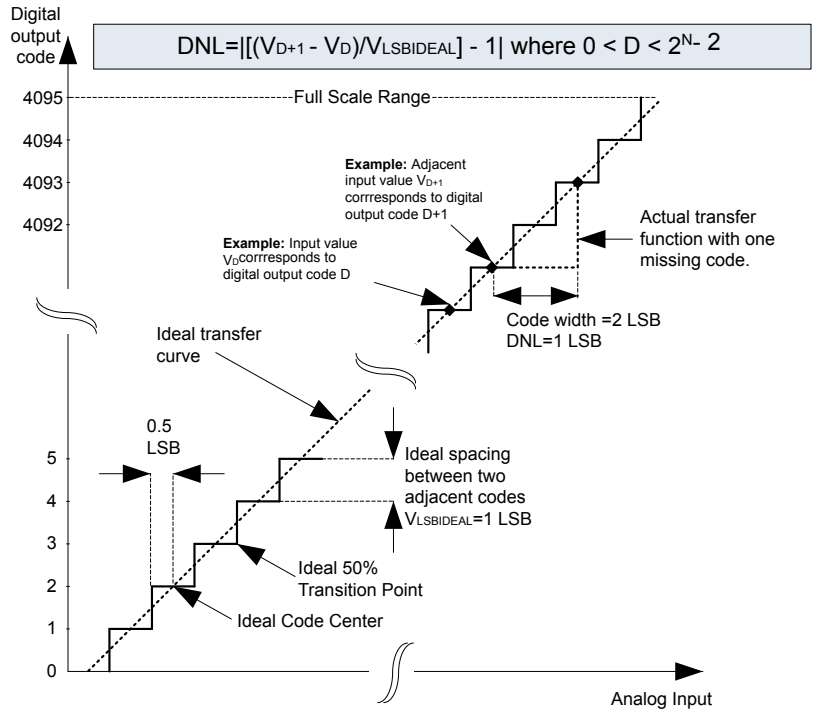

Figure 4.24. Differential Non-Linearity (DNL)

4.13 Analog Comparator (ACMP)

Table 4.17. ACMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ACMPIN}		0	—	V_{DD}	V
Input bias current	$I_{ACMPBIASIN}$	VSS < VIN < VDD	-40	—	40	nA
Input offset current	$I_{ACMPOFFSETIN}$	VSS < VIN < VDD	-40	—	40	nA
ACMP Common Mode voltage range	V_{ACMPCM}		0	—	V_{DD}	V
Active current	I_{ACMP}	BIASPROG=0b0000, FULLBIAS=0 and HALFBIAS=1 in ACMPn_CTRL register	—	0.1[1]	0.4[1]	µA
		BIASPROG=0b1111, FULLBIAS= 0 and HALFBIAS=0 in ACMPn_CTRL register	—	2.87[1]	15[1]	µA
		BIASPROG=0b1111, FULLBIAS= 1 and HALFBIAS=0 in ACMPn_CTRL register	—	195[1]	520[1]	µA
		BIASPROG=0b0100, FULLBIAS=0, HALFBIAS=1 in ACMPn_CTRL register	—	0.8[1]	2.2[1]	µA
		BIASPROG=0b1111, FULLBIAS=0, HALFBIAS=1 in-ACMPn_CTRL register	—	2.7[1]	8.1[1]	µA
Current consumption of internal voltage reference	$I_{ACMPREF}$	Internal voltage reference off. Using external voltage reference	—	0	—	µA
		Internal voltage reference	—	5	—	µA

4.17 I2C

Table 4.25. I2C Standard-mode (Sm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0	—	100[1]	kHz
SCL clock low time	t_{LOW}	4.7	—	—	µs
SCL clock high time	t_{HIGH}	4.0	—	—	µs
SDA set-up time	$t_{SU,DAT}$	250	—	—	ns
SDA hold time	$t_{HD,DAT}$	8	—	3450[2,3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	4.7	—	—	µs
(Repeated) START condition hold time	$t_{HD,STA}$	4.0	—	—	µs
STOP condition set-up time	$t_{SU,STO}$	4.0	—	—	µs
Bus free time between a STOP and a START condition	t_{BUF}	4.7	—	—	µs

Note:
1. For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32LG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

Table 4.26. I2C Fast-mode (Fm)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0		400[1]	kHz
SCL clock low time	t_{LOW}	1.3			µs
SCL clock high time	t_{HIGH}	0.6			µs
SDA set-up time	$t_{SU,DAT}$	100			ns
SDA hold time	$t_{HD,DAT}$	8		900[2,3]	ns
Repeated START condition set-up time	$t_{SU,STA}$	0.6			µs
(Repeated) START condition hold time	$t_{HD,STA}$	0.6			µs
STOP condition set-up time	$t_{SU,STO}$	0.6			µs
Bus free time between a STOP and a START condition	t_{BUF}	1.3			µs

Note:
1. For the minimum HFPERCLK frequency required in Fast-mode, see the I2C chapter in the EFM32LG Reference Manual.
2. The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}).
3. When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((900*10^{-9} [s] * $f_{HFPERCLK}$ [Hz]) - 4).

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
46	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		LES_CH13 #0
47	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3	LES_CH14 #0
48	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3	LES_CH15 #0 DBG_SWO #1
49	PF0		TIM0_CC0 #5 LE-TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
50	PF1		TIM0_CC1 #5 LE-TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
51	PF2		TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
52	PF3		TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
53	PF4		TIM0_CDTI1 #2/5		PRS_CH1 #1
54	PF5		TIM0_CDTI2 #2/5		PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	PE8		PCNT2_S0IN #1		PRS_CH3 #1
57	PE9		PCNT2_S1IN #1		
58	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11		TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
60	PE12		TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
61	PE13			US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
62	PE14		TIM3_CC0 #0	LEU0_TX #2	
63	PE15		TIM3_CC1 #0	LEU0_RX #2	
64	PA15		TIM3_CC2 #0		

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
3	PA2		TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
4	PA3		TIM0_CDTI0 #0		LES_ALTEX2 #0 ETM_TD1 #3
5	PA4		TIM0_CDTI1 #0		LES_ALTEX3 #0 ETM_TD2 #3
6	PA5		TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	IOVDD_0	Digital IO power supply 0.			
8	VSS	Ground.			
9	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
10	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
11	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
12	PC3	ACMP0_CH3DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
13	PC4	ACMP0_CH4 OPAMP_P0	TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
14	PC5	ACMP0_CH5 OPAMP_N0	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
15	PB7	LFXTAL_P	TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
16	PB8	LFXTAL_N	TIM1_CC1 #3	US0_RX #4 US1_CS #0	
17	PA8		TIM2_CC0 #0		
18	PA9		TIM2_CC1 #0		
19	PA10		TIM2_CC2 #0		
20	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.			
21	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LE-TIM0_OUT0 #1	I2C1_SDA #1	
22	VSS	Ground.			
23	AVDD_1	Analog power supply 1.			
24	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	
25	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15				UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14				UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX	PC13		PB10	PE3				UART1 Receive input.
U1_TX	PC12		PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit.Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
50	PF1		TIM0_CC1 #5 LE-TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
51	PF2		TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
52	USB_VBUS	USB 5.0 V VBUS input.			
53	PF12			USB_ID	
54	PF5		TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	PE8		PCNT2_S0IN #1		PRS_CH3 #1
57	PE9		PCNT2_S1IN #1		
58	PE10		TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11		TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
60	PE12		TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
61	PE13			US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
62	PE14		TIM3_CC0 #0	LEU0_TX #2	
63	PE15		TIM3_CC1 #0	LEU0_RX #2	
64	PA15		TIM3_CC2 #0		

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT					PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
ETM_TCLK	PD7		PC6					Embedded Trace Module ETM clock .
ETM_TD0	PD6		PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7			PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6			PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5							I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.

5.14 EFM32LG880 (LQFP100)

5.14.1 Pinout

The EFM32LG880 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

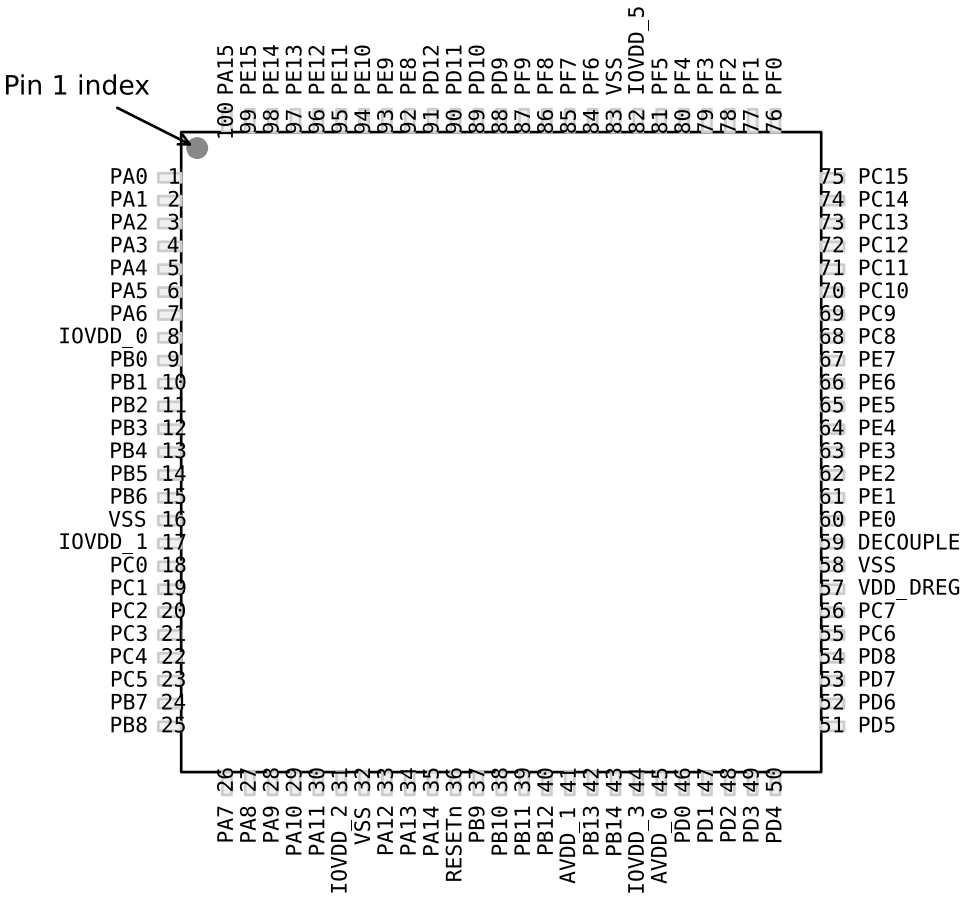

Figure 5.27. EFM32LG880 Pinout (top view, not to scale)

Table 5.40. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
99	PE15	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
100	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (µm)	Y (µm)	Analog	EBI	Timers	Communica-tion	Other
25	PC3	-2065.0	-1322.6	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0 ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
26	PC4	-2065.0	-1484.3	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
27	PC5	-2065.0	-1586.5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
28	PB7	-2065.0	-1708.6	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
29	PB8	-2065.0	-1830.6	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
30	PA7	-1832.5	-2065.0	LCD_SEG35	EBI_CSTFT #0/1/2			
31	PA8	-1695.5	-2065.0	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
32	PA9	-1558.5	-2065.0	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
33	PA10	-1421.5	-2065.0	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
34	PA11	-1284.5	-2065.0	LCD_SEG39	EBI_HSNC #0/1/2			
35	IOVDD_2	-1147.5	-2065.0	Digital IO power supply 2.				
36	IOVSS_2	-1027.4	-2065.0	Digital IO ground 2.				
37	PA12	-907.2	-2065.0	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
38	PA13	-780.6	-2065.0	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
39	PA14	-654.0	-2065.0	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
40	RESETn	-527.4	-2065.0	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
41	PB9	-401.0	-2065.0		EBI_A03 #0/1/2		U1_TX #2	
42	PB10	-274.5	-2065.0		EBI_A04 #0/1/2		U1_RX #2	
43	PB11	260.7	-2065.0	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
44	PB12	366.0	-2065.0	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
45	AVSS_2	464.8	-2065.0	Analog ground 2.				
46	AVDD_2	560.5	-2065.0	Analog power supply 2.				

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
52	USB_VBUS	USB 5.0 V VBUS input.			
53	PF12			USB_ID	
54	PF5	LCD_SEG3	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	PE8	LCD_SEG4	PCNT2_S0IN #1		PRS_CH3 #1
57	PE9	LCD_SEG5	PCNT2_S1IN #1		
58	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
60	PE12	LCD_SEG8	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
61	PE13	LCD_SEG9		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
62	PE14	LCD_SEG10	TIM3_CC0 #0	LEU0_TX #2	
63	PE15	LCD_SEG11	TIM3_CC1 #0	LEU0_RX #2	
64	PA15	LCD_SEG12	TIM3_CC2 #0		

5.21.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.62. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit.Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.22.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG995 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.66. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

Symbol	Min	Nom	Max
e		0.50 BSC	
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa		0.10	
bbb		0.10	
ccc		0.10	
ddd		0.05	
eee		0.08	

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.

11.2 QFN64 PCB Layout

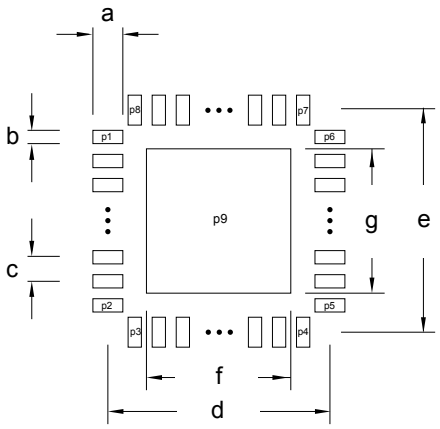

Figure 11.2. QFN64 PCB Land Pattern

Table 11.2. QFN64 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Pin Number	Symbol	Pin Number
a	0.85	P1	1	P8	64
b	0.30	P2	16	P9	65
c	0.50	P3	17		
d	8.90	P4	32		
e	8.90	P5	33		
f	7.20	P6	48		
g	7.20	P7	49		

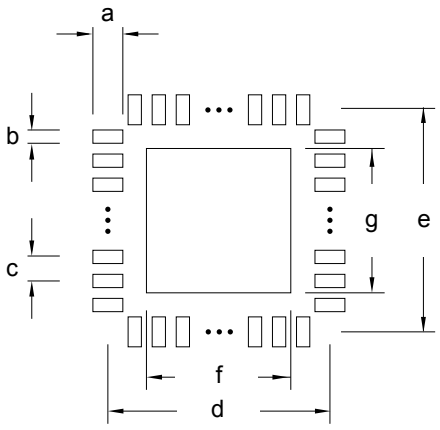

Figure 11.3. QFN64 PCB Solder Mask

- VREF voltage drift (V_{REF_VDRIFT}) – added min, typ, max.
- VREF temperature drift (V_{REF_TDRIFT}) – added min, typ, max.
- VREF current consumption (I_{VREF}) – added typ, max, replacing I_{ADCREF}.
- ADC and DAC VREF matching (V_{REF_MATCH}) – added typical.

4.11 Digital Analog Converter (DAC) – Updated the footnote for active average current (I_{DAC}), and added the following new VREF specs at each voltage reference:

- VREF output voltage (V_{REF}) – added min, typ, max.
- VREF voltage drift (V_{REF_VDRIFT}) – added min, typ, max.
- VREF temperature drift (V_{REF_TDRIFT}) – added min, typ, max.
- VREF current consumption (I_{VREF}) – added typ, max.
- ADC and DAC VREF matching (V_{REF_MATCH}) – added typical.

4.12 Operational Amplifier (OPAMP) – Removed note specifying that OPAMP specs stem from simulations, and added new specifications for the following:

- Active Current (I_{OPAMP}) – new specifications at various (new) bias program settings.
- Gain Bandwidth Product (GBW_{OPAMP}) – new (typ) specifications at new bias program settings and DC bias settings.
- Input Offset Voltage (V_{OFFSET}) – specified min, typ, max for Op Amps (OPA0-1).
- Input Bias Current ($I_{OPAMPBIASIN}$) – new min and max specifications.
- Input Offset Current ($I_{OPAMPOFF\text{-}SETIN}$) – new min and max specifications.
- Slew Rate (SR_{OPAMP}) – new specifications at new bias program settings.
- Updated footnote.

4.13 Analog Comparator (ACMP) – Added new specifications for the following:

- Input Bias Current ($I_{ACMPBIASIN}$) – added min and max.
- Input Offset Current ($I_{ACMPOFFSETIN}$) – added min and max.
- Active Current (I_{ACMP}) – added two new condition settings, and footnote.
- Negative Response Time ($t_{RESPONSE\_N}$) – added new specifications.
- Positive Response Times ($t_{RESPONSE\_P}$) – added new specifications.
- Offset Voltage ($V_{ACMPOFFSET}$) – added specifications at new bias program settings.
- ACMP Hysteresis ($V_{ACMPHYST}$) – added specifications for negative and positive hysteresis at various bias program settings.
- VDD SCALED Input Accuracy ($V_{VDDSCALED}$) – added new specifications (typical).

4.14 Voltage Comparator (VCMP) – Added the following new specifications:

- Negative hysteresis ($V_{VCMPHYST\_N}$), replacing VCMP hysteresis.
- Positive hysteresis ($V_{VCMPHYST\_P}$), replacing VCMP hysteresis.
- Hysteresis Delta ($V_{VCMPHYST\_DELTA}$).
- Negative Response Time ($t_{RESPONSE\_N}$).
- Positive Response Time ($t_{RESPONSE\_P}$).
- Footnote for active current, I_{VCMP}.

4.18 USART SPI – Corrected parameter descriptions for $t_{CS\_DIS\_MI}$.

4.19 Digital Peripherals – Added (typical) LE Peripheral Interface Clock Current (I_{LFCLK}) specifications with both the LFXO-LFA and LFXO-LFB clock trees.

Removed MSL information (Moisture Sensitivity Level). Instead, MSL information can be found in the Qual report that is available on the Silicon Labs website.

New formatting throughout.

14.5 Revision 1.20

September 30th, 2013

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Added I2C characterization data.

Added SPI characterization data.

Corrected the DAC and OPAMP2 pin sharing information in the Alternate Functionality Pinout section.

Corrected GPIO operating voltage from 1.8 V to 1.85 V.

For devices with USB, added the USB bootloader information.

Corrected the ADC resolution from 12, 10 and 6 bit to 12, 8 and 6 bit.

For QFN64 packages, removed UART mentioned incorrectly in the QFN64 parts.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

This revision applies the following devices:

- EFM32LG900

March 16th, 2015

Corrected pad numbers and the order of the pads in the padout table so that it matches the drawing.