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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg330f64-qfn64

3.1.23 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.24 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

3.1.25 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

3.1.26 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

3.1.27 Operational Amplifier (OPAMP)

The EFM32LG features up to 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

3.1.28 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSE™), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

3.1.29 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32LG to keep track of time and retain data, even if the main power source should drain out.

3.1.30 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data and key registers. All write accesses to the AES module must be 32-bit operations, i.e. 8- or 16-bit operations are not supported.

3.1.31 General Purpose Input/Output (GPIO)

In the EFM32LG, there are up to 93 General Purpose Input/Output (GPIO) pins, which are divided into ports with up to 16 pins each. These pins can individually be configured as either an output or input. More advanced configurations like open-drain, filtering and drive strength can also be configured individually for the pins. The GPIO pins can also be overridden by peripheral pin connections, like Timer PWM outputs or USART communication, which can be routed to several locations on the device. The GPIO supports up to 16 asynchronous external pin interrupts, which enables interrupts from any pin on the device. Also, the input value of a pin can be routed through the Peripheral Reflex System to other peripherals.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15				UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14				UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX	PC13		PB10	PE3				UART1 Receive input.
U1_TX	PC12		PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).

5.7.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG332 is shown in the following figure.

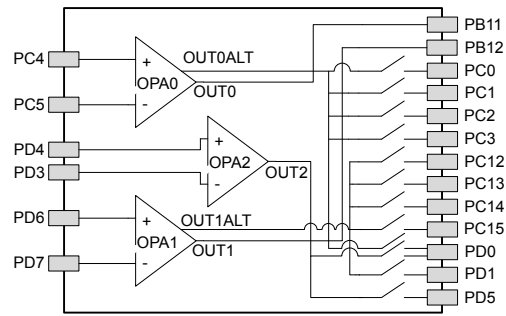


Figure 5.14. Opamp Pinout

5.10.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.29. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.

5.12.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.35. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_VIN	PD8							Battery input for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LCD_SEG24	PF6							LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG25	PF7							LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG26	PF8							LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG27	PF9							LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG28	PD9							LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10							LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG30	PD11							LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12							LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0							LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1							LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2							LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7							LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8							LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9							LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10							LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG39	PA11							LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
25	PC3	-2065.0	-1322.6	ACMP0_CH3 DAC0_OUT0ALT T #3/ OPAMP_OUT0 ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
26	PC4	-2065.0	-1484.3	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
27	PC5	-2065.0	-1586.5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
28	PB7	-2065.0	-1708.6	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
29	PB8	-2065.0	-1830.6	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
30	PA7	-1832.5	-2065.0	LCD_SEG35	EBI_CSTFT #0/1/2			
31	PA8	-1695.5	-2065.0	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
32	PA9	-1558.5	-2065.0	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
33	PA10	-1421.5	-2065.0	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
34	PA11	-1284.5	-2065.0	LCD_SEG39	EBI_HSNC #0/1/2			
35	IOVDD_2	-1147.5	-2065.0	Digital IO power supply 2.				
36	IOVSS_2	-1027.4	-2065.0	Digital IO ground 2.				
37	PA12	-907.2	-2065.0	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
38	PA13	-780.6	-2065.0	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
39	PA14	-654.0	-2065.0	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
40	RESETn	-527.4	-2065.0	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
41	PB9	-401.0	-2065.0		EBI_A03 #0/1/2		U1_TX #2	
42	PB10	-274.5	-2065.0		EBI_A04 #0/1/2		U1_RX #2	
43	PB11	260.7	-2065.0	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
44	PB12	366.0	-2065.0	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
45	AVSS_2	464.8	-2065.0	Analog ground 2.				
46	AVDD_2	560.5	-2065.0	Analog power supply 2.				

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.17.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG900 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.51. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
C11	PC11	ACMP1_CH3	EBI_ALE #1/2		US0_TX #2	LES_CH11 #0
D1	PA3	LCD_SEG16	EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
D2	PA2	LCD_SEG15	EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
D3	PB15					ETM_TD2 #1
D4	VSS	Ground.				
D5	IOVDD_6	Digital IO power supply 6.				
D6	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
D7	IOVDD_5	Digital IO power supply 5.				
D8	PF1			TIM0_CC1 #5 LE- TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
D9	PE7	LCD_COM3	EBI_A14 #0/1/2		US0_TX #1	
D10	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
D11	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
E1	PA6	LCD_SEG19	EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
E2	PA5	LCD_SEG18	EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
E3	PA4	LCD_SEG17	EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
E4	PB0	LCD_SEG32	EBI_A16 #0/1/2	TIM1_CC0 #2		
E8	PF0			TIM0_CC0 #5 LE- TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
E9	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
E10	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
E11	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
F1	PB1	LCD_SEG33	EBI_A17 #0/1/2	TIM1_CC1 #2		
F2	PB2	LCD_SEG34	EBI_A18 #0/1/2	TIM1_CC2 #2		
F3	PB3	LCD_SEG20/ LCD_COM4	EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
F4	PB4	LCD_SEG21/ LCD_COM5	EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
F8	VDD_DREG	Power supply for on-chip voltage regulator.				
F9	VSS_DREG	Ground for on-chip voltage regulator.				
F10	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_SEG28	PD9							LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10							LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG30	PD11							LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12							LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0							LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1							LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2							LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7							LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8							LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9							LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10							LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG39	PA11							LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN		PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN		PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1							Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3				PC2			Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4				PC3			Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12	PB2	PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.

6.2 BGA112 PCB Layout

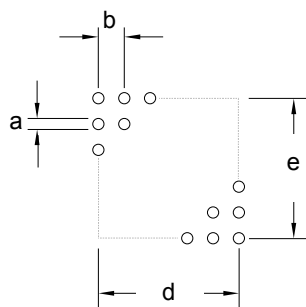


Figure 6.2. BGA112 PCB Land Pattern

Table 6.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.35
b	0.80
d	8.00
e	8.00

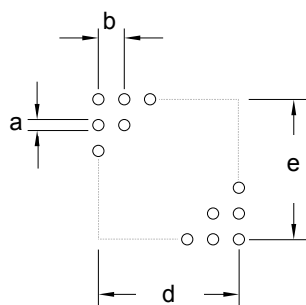


Figure 6.3. BGA112 PCB Solder Mask

Table 6.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.48
b	0.80
d	8.00
e	8.00

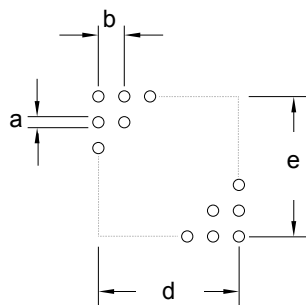


Figure 7.4. BGA120 PCB Stencil Design

Table 7.3. BGA120 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.25
b	0.50
d	6.00
e	6.00

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

9. LQFP100 Package Specifications

9.1 LQFP100 Package Dimensions

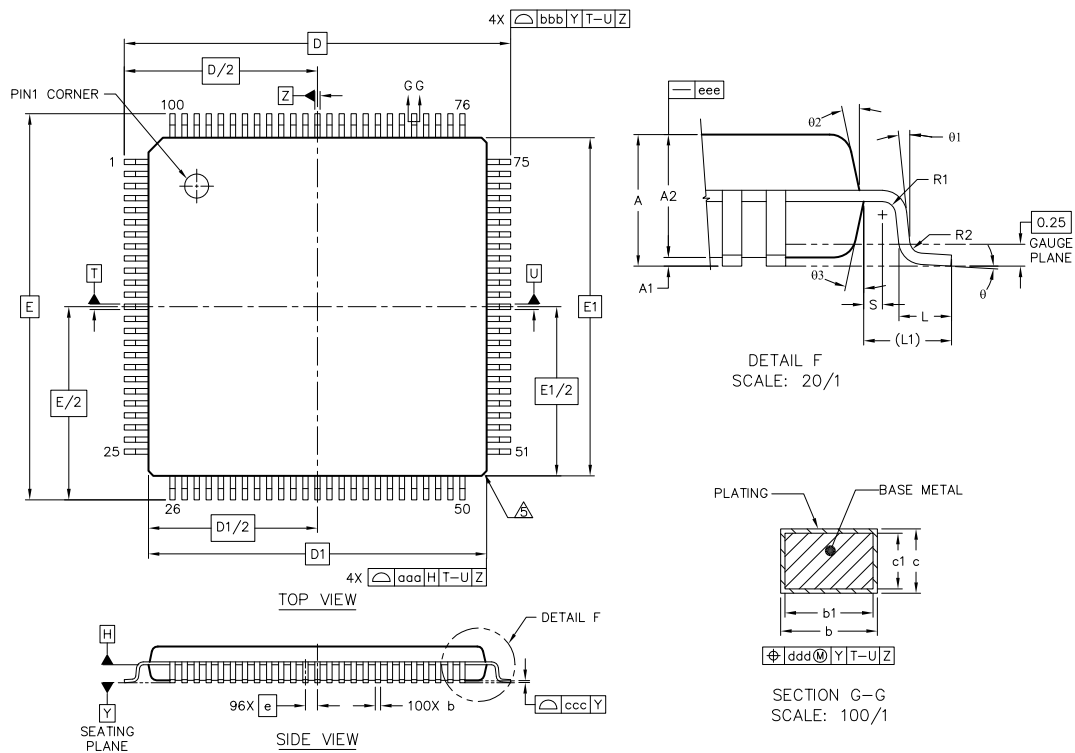


Figure 9.1. LQFP100

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'.
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

Table 9.1. LQFP100 (Dimensions in mm)

	SYMBOL	MIN	NOM	MAX
total thickness	A	—	—	1.6
stand off	A1	0.05	—	0.15
mold thickness	A2	1.35	1.4	1.45
lead width (plating)	b	0.17	0.2	0.27
lead width	b1	0.17	—	0.23
L/F thickness (plating)	c	0.09	—	0.2

14.2 Revision 1.31

December 16th, 2015

Removed Environmental section from General Operating Conditions.

Added max current consumption numbers for energy modes.

For devices with an ADC, added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

For devices with an EBI, updated EBI ready/wait figure.

Updated memory map.

Removed DC_{HFRCO} and $DC_{AUXHFRCO}$ parameters.

For CSP81 package, updated typical and added min/max values for f_{HFRCO} and $f_{AUXHFRCO}$.

For devices in CSP81 package with a DAC, updated OPAMP table.

Fixed typos

Added OPAMP, ADC, and ACMP Input Bias Current and Input Offset Current specifications.

Added lower limit for GPIO Input Leakage Current and updated the upper limit for this specification.

Removed the "by simulation and/or technology characterization" phrase from the Electrical Characteristics Test Conditions section.

14.3 Revision 1.30

June 13th, 2014

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Removed "Preliminary" markings.

Updated electrical characteristics and updated/added plots.

Updated orderable part numbers.

Added AUXHFRCO to block diagram and electrical characteristics.

For devices with EBI, added EBI timing chapter.

14.4 Revision 1.21

November 21st, 2013

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

For devices with a DAC, re-added missing DAC-data.