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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	50
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg332f64-qfp64t

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32LG395F256G-E-BGA120	256	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG840F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG840F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG840F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG842F64G-E-QFP64	64	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG842F128G-E-QFP64	128	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG842F256G-E-QFP64	256	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG880F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG880F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG880F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG890F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG890F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG890F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG895F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG895F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG895F256G-E-BGA120	256	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG900F256G-E-D1I	256	32	48	1.98 - 3.8	-40 - 85	Wafer
EFM32LG940F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG940F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG940F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG942F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG942F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG942F256G-E-BGA120	256	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG980F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG980F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG980F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG990F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG990F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG990F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG995F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG995F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG995F256G-E-BGA120	256	32	48	1.98 - 3.8	-40 - 85	BGA120

Module	Configuration	Pin Connections
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	93 pins	Available pins are shown in 5.11.3 GPIO Pinout Overview

Module	Configuration	Pin Connections
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	93 pins	Available pins are shown in Table 4.3 (p. 70)
LCD	Full configuration	LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

3.2.18 EFM32LG940

The features of the EFM32LG940 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.18. EFM32LG940 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT

4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	211	225	$\mu\text{A}/\text{MHz}$
		48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	211	230	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	212	220	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	213	223	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	214	224	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	215	226	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	216	231	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	217	237	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	218	239	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	219	239	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	224	245	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	224	258	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	257	285	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	261	293	$\mu\text{A}/\text{MHz}$

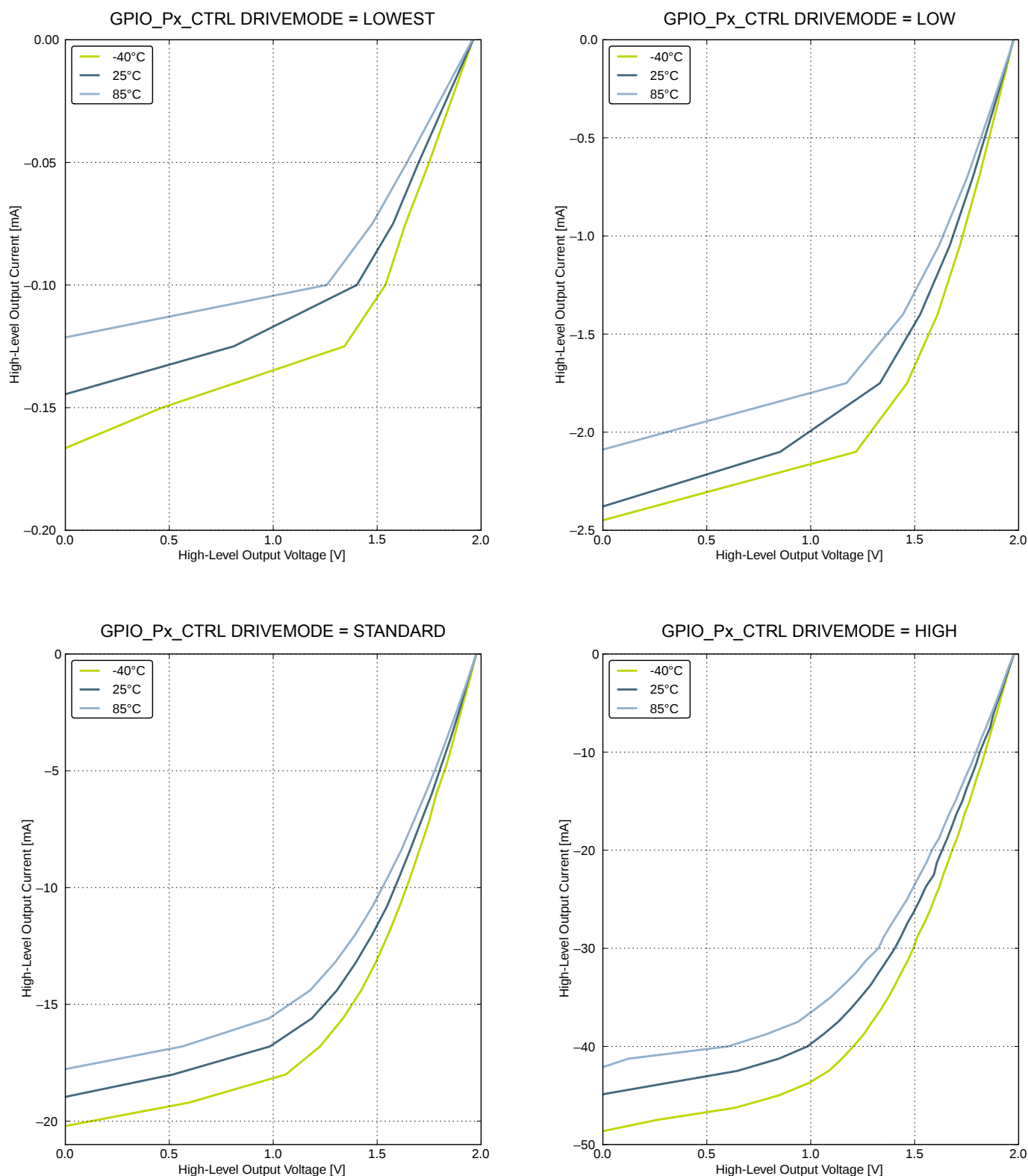


Figure 4.11. Typical High-Level Output Current, 2 V Supply Voltage

4.9.5 AUXHFRCO

Table 4.12. AUXHFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency, all packages except CSP, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	f_{AUXHFRCO}	28 MHz frequency band	27.5	28.0	28.5	MHz
		21 MHz frequency band	20.6	21.0	21.4	MHz
		14 MHz frequency band	13.7	14.0	14.3	MHz
		11 MHz frequency band	10.8	11.0	11.2	MHz
		7 MHz frequency band	6.48 ¹	6.60 ¹	6.72 ¹	MHz
		1 MHz frequency band	1.15 ²	1.20 ²	1.25 ²	MHz
Oscillation frequency, CSP devices, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	f_{AUXHFRCO}	28 MHz frequency band	—	28.0	—	MHz
		21 MHz frequency band	—	21.0	—	MHz
		14 MHz frequency band	—	14.0	—	MHz
		11 MHz frequency band	—	11.0	—	MHz
		7 MHz frequency band	—	6.60 ¹	—	MHz
		1 MHz frequency band	—	1.20 ²	—	MHz
Settling time after start-up	$t_{\text{AUXHFRCO_settling}}$	$f_{\text{AUXHFRCO}} = 14\text{ MHz}$	—	0.6	—	Cycles
Frequency step for LSB change in TUNING value	TUNE-STEP _{AUXHFRCO}		—	0.3 ³	—	%

Note:

1. For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_AUXHFRCOCTRL register may be used to adjust the AUXHFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the AUXHFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

4.9.6 ULFRCO

Table 4.13. ULFRCO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Oscillation frequency	f_{ULFRCO}	25°C, 3V	0.7	—	1.75	kHz
Temperature coefficient	TC _{ULFRCO}		—	0.05	—	%/°C
Supply voltage coefficient	VC _{ULFRCO}		—	-18.2	—	%/V

4.10 Analog Digital Converter (ADC)

Table 4.14. ADC

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V_{ADCIN}	Single ended	0	—	V_{REF}	V
		Differential	$-V_{\text{REF}}/2$	—	$V_{\text{REF}}/2$	V
Input range of external reference voltage, single ended and differential	V_{ADCREFIN}		1.25	—	V_{DD}	V
Input range of external negative reference voltage on channel 7	$V_{\text{ADCREFIN_CH7}}$	See V_{ADCREFIN}	0	—	$V_{\text{DD}} - 1.1$	V
Input range of external positive reference voltage on channel 6	$V_{\text{ADCREFIN_CH6}}$	See V_{ADCREFIN}	0.625	—	V_{DD}	V
Common mode input range	V_{ADCCMIN}		0	—	V_{DD}	V
Input current	I_{ADCIN}	2 pF sampling capacitors	—	<100	—	nA
Analog input common mode rejection ratio	CMRR_{ADC}		—	65	—	dB
Average active current	I_{ADC}	1 MSamples/s, 12 bit, external reference	—	351	—	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b00	—	67	—	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b01	—	63	—	μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP-MODE in ADCn_CTRL set to 0b10	—	64	—	μA
Input capacitance	C_{ADCIN}		—	2	—	pF
Input ON resistance	R_{ADCIN}		1	—	—	M Ω
Input RC filter resistance	R_{ADCFILT}		—	10	—	k Ω
Input RC filter/decoupling capacitance	C_{ADCFILT}		—	250	—	fF
Input bias current	$I_{\text{ADCBIASIN}}$	$V_{\text{SS}} < V_{\text{IN}} < V_{\text{DD}}$	-40	—	40	nA
Input offset current	$I_{\text{ADCOFFSETIN}}$	$V_{\text{SS}} < V_{\text{IN}} < V_{\text{DD}}$	-40	—	40	nA
ADC Clock Frequency	f_{ADCCLK}		—	—	13	MHz
Conversion time	t_{ADCCONV}	6 bit	7	—	—	ADCCLK Cycles
		8 bit	11	—	—	ADCCLK Cycles
		12 bit	13	—	—	ADCCLK Cycles

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG280 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.9. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	—	—	—	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	—	—	—	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

5.3.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG280 is shown in the following figure.

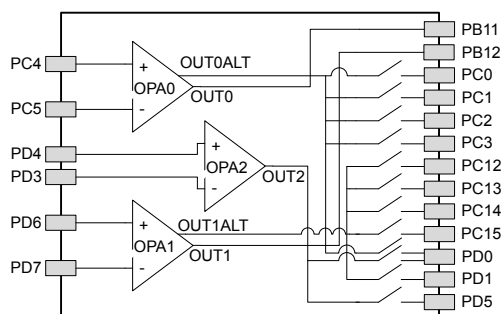


Figure 5.6. Opamp Pinout

5.7.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG332 is shown in the following figure.

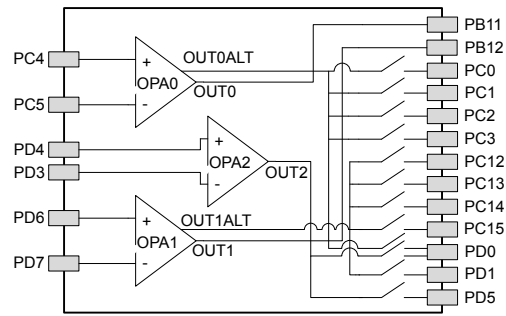


Figure 5.14. Opamp Pinout

CSP81 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
F8	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
F9	PB6			US2_CS #1	
G1	VDD_DREG	Power supply for on-chip voltage regulator.			
G2	VSS_DREG	Ground for on-chip voltage regulator.			
G3	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
G4	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
G5	PB12	DAC0_OUT1 / OPAMP_OUT1	LETIM0_OUT1 #1	I2C1_SCL #1	
G6	PB11	DAC0_OUT0 / OPAMP_OUT0	TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
G7	PA9		TIM2_CC1 #0		
G8	PC4	ACMP0_CH4 OPAMP_P0	TIM0_CDTI2 #4 LE- TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
G9	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
H1	PD8	BU_VIN			CMU_CLK1 #1
H2	PD6	ADC0_CH6 OPAMP_P1	TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
H3	PD2	ADC0_CH2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
H4	VSS	Ground.			
H5	AVSS_0	Analog ground 0.			
H6	AVDD_0	Analog power supply 0.			
H7	PA10		TIM2_CC2 #0		
H8	PC5	ACMP0_CH5 OPAMP_N0	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
H9	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
J1	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
J2	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
J3	IOVDD_3	Digital IO power supply 3.			
J4	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
J5	PB13	HFXTAL_P		US0_CLK #4/5 LEU0_TX #1	

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
74	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
75	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
76	PF0			TIM0_CC0 #5 LE- TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
77	PF1			TIM0_CC1 #5 LE- TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
78	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
79	PF3	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
80	PF4	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
81	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
82	IOVDD_5	Digital IO power supply 5.				
83	VSS	Ground.				
84	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
85	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
86	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
87	PF9	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
88	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
89	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
90	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
91	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
92	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
93	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
94	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
95	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
96	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
97	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
98	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.17.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG900 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.51. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN				PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN				PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1							Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3		PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2		PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3		PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3							Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4							Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12						Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13						Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14						Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
US0_CLK	PE12	PE5			PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4			PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6		PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0A LT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1A LT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
G1	PB5	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
G2	PB6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				
G10	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
G11	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
H1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
H2	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
H3	PD14				I2C0_SDA #3	
H4	PA7	LCD_SEG35	EBI_CSTFT #0/1/2			
H5	PA8	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8	BU_VIN				CMU_CLK1 #1
H9	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
H10	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
H11	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
J1	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
J2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.

		SYMBOL	MIN	NOM	MAX
lead thickness		c1	0.09	—	0.16
	x	D	16 BSC		
	y	E	16 BSC		
body size	x	D1	14 BSC		
	y	E1	14 BSC		
lead pitch		e	0.5 BSC		
		L	0.45	0.6	0.75
footprint		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	—	—
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	—	—
		R1	0.08	—	0.2
		S	0.2	—	—
package edge tolerance		aaa	0.2		
lead edge tolerance		bbb	0.2		
coplanarity		ccc	0.08		
lead offset		ddd	0.08		
mold flatness		eee	0.05		

The LQFP100 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>

10.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.

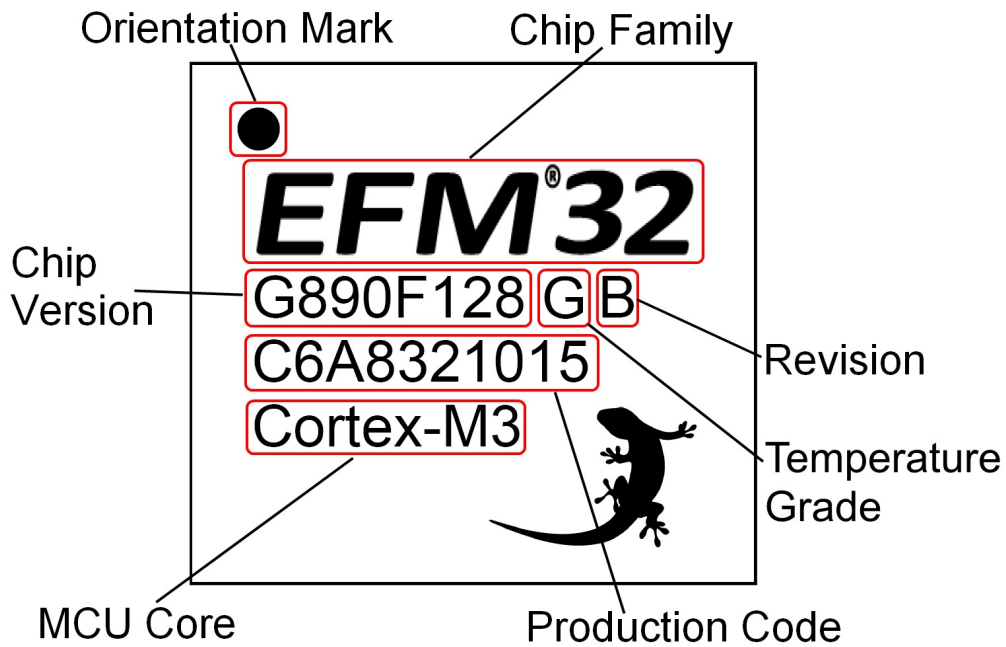


Figure 10.5. Example Chip Marking (Top View)