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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	87
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg390f64-bga112t

3.2.4 EFM32LG290

The features of the EFM32LG290 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.4. EFM32LG290 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNCR, EBI_NANDREN, EBI_NANDWEN, EBI_REn, EBI_VSNCR, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

3.2.5 EFM32LG295

The features of the EFM32LG295 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.5. EFM32LG295 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

3.2.9 EFM32LG380

The features of the EFM32LG380 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.9. EFM32LG380 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNCR, EBI_NANDREN, EBI_NANDWEN, EBI_REN, EBI_VSNCR, EBI_WEN
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O

3.2.16 EFM32LG895

The features of the EFM32LG895 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.16. EFM32LG895 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	211	225	$\mu\text{A}/\text{MHz}$
		48 MHz HFXO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	211	230	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	212	220	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	213	223	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	214	224	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	215	226	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	216	231	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	217	237	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	218	239	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	219	239	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	224	245	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	224	258	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=25^{\circ}\text{C}$	—	257	285	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD}=3.0\text{ V}$, $T_{AMB}=85^{\circ}\text{C}$	—	261	293	$\mu\text{A}/\text{MHz}$

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Voltage drift	$V_{\text{HFRCO_DRIFT}}$	$f_{\text{HFRCO}} = 28 \text{ MHz}$	—	10768	—	ppm/V
		$f_{\text{HFRCO}} = 21 \text{ MHz}$	—	8939	—	ppm/V
		$f_{\text{HFRCO}} = 14 \text{ MHz}$	—	8040	—	ppm/V
		$f_{\text{HFRCO}} = 11 \text{ MHz}$	—	7719	—	ppm/V
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$	—	8491	—	ppm/V
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$	—	-124035	—	ppm/V
Temperature drift	$T_{\text{HFRCO_DRIFT}}$	$f_{\text{HFRCO}} = 28 \text{ MHz}$	—	91	—	ppm/°C
		$f_{\text{HFRCO}} = 21 \text{ MHz}$	—	88	—	ppm/°C
		$f_{\text{HFRCO}} = 14 \text{ MHz}$	—	43	—	ppm/°C
		$f_{\text{HFRCO}} = 11 \text{ MHz}$	—	50	—	ppm/°C
		$f_{\text{HFRCO}} = 6.6 \text{ MHz}$	—	-50	—	ppm/°C
		$f_{\text{HFRCO}} = 1.2 \text{ MHz}$	—	83	—	ppm/°C
Frequency step for LSB change in TUNING value	$\text{TUNESTEP}_{\text{HFRCO}}$		—	0.3 ³	—	%

Note:

1. For devices with prod. rev. < 19, Typ = 7MHz and Min/Max values not applicable.
2. For devices with prod. rev. < 19, Typ = 1MHz and Min/Max values not applicable.
3. The TUNING field in the CMU_HFRCOCTRL register may be used to adjust the HFRCO frequency. There is enough adjustment range to ensure that the frequency bands above 7 MHz will always have some overlap across supply voltage and temperature. By using a stable frequency reference such as the LFXO or HFXO, a firmware calibration routine can vary the TUNING bits and the frequency band to maintain the HFRCO frequency at any arbitrary value between 7 MHz and 28 MHz across operating conditions.

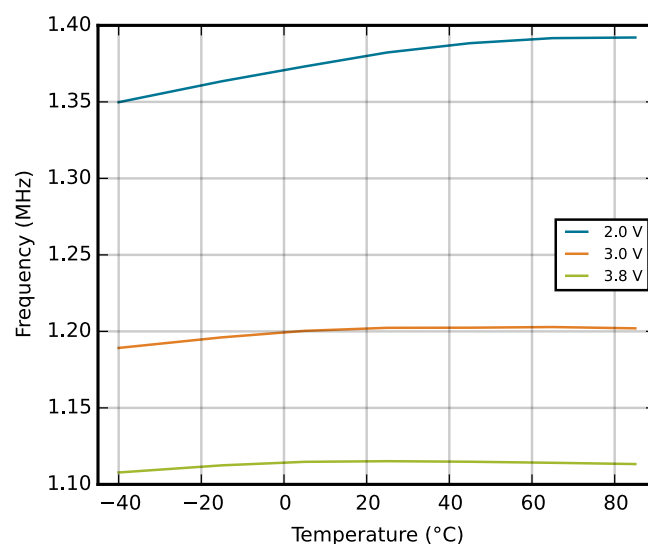
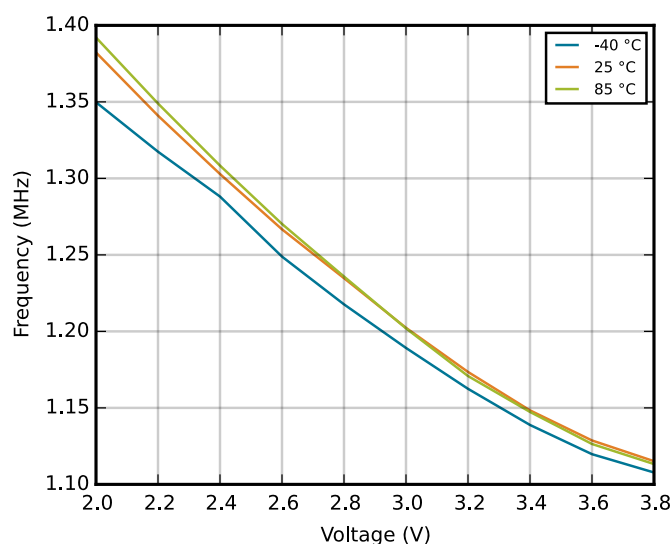


Figure 4.17. Calibrated HFRCO 1 MHz Band Frequency vs Supply Voltage and Temperature

4.10.1 Typical Performance

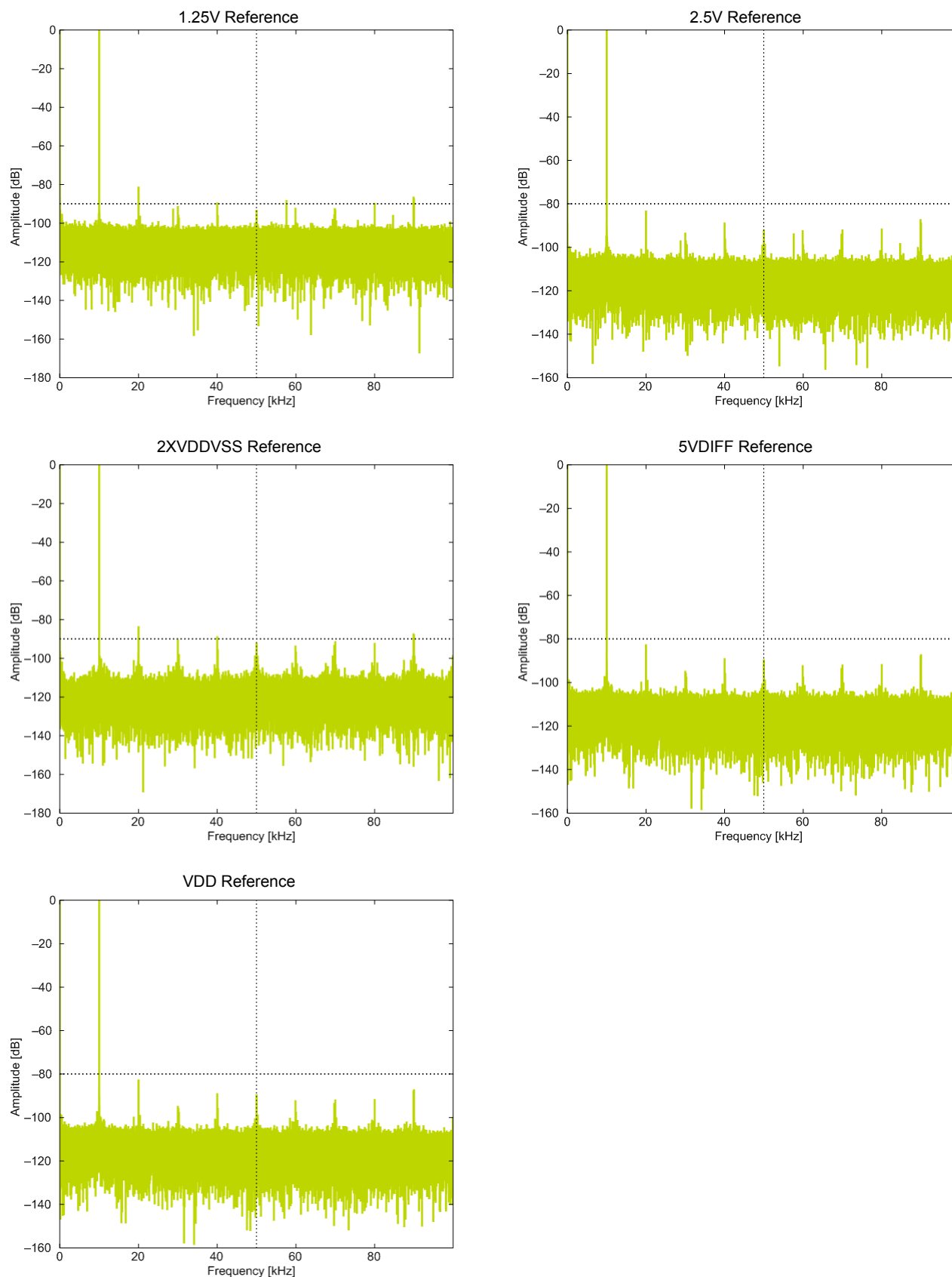


Figure 4.25. ADC Frequency Spectrum, VDD = 3 V, Temp = 25 °C

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LEU1_RX	PC7							LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4							Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5							Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8		PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9		PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10		PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
US0_CLK	PE12		PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13		PC8	PC14	PB14	PB14		USART0 chip select input / output.

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
52	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
53	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
54	PD8	BU_VIN				CMU_CLK1 #1
55	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
56	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
57	VDD_DREG	Power supply for on-chip voltage regulator.				
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
60	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
61	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
62	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
63	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
64	PE4		EBI_A11 #0/1/2		US0_CS #1	
65	PE5		EBI_A12 #0/1/2		US0_CLK #1	
66	PE6		EBI_A13 #0/1/2		US0_RX #1	
67	PE7		EBI_A14 #0/1/2		US0_TX #1	
68	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
69	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
70	PC10	ACMP1_CH2	EBI_A10 #1/2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
71	PC11	ACMP1_CH3	EBI_ALE #1/2		US0_TX #2	LES_CH11 #0
72	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
73	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
74	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4							USART2 clock input / output.
US2_CS	PC5							USART2 chip select input / output.
US2_RX	PC3							USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2							USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4							USART2 clock input / output.
US2_CS	PC5							USART2 chip select input / output.
US2_RX	PC3							USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2							USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.7.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG332 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.21. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	-	-	-	-	-	PA10	PA9	PA8	-	-	PA5	PA4	PA3	PA2	PA1	PA0
Port B	-	PB14	PB13	-	PB11	-	-	PB8	PB7	-	-	-	-	-	-	-
Port C	-	-	-	-	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	-	-	-	-	-	-	-	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	-	-	-	-	-	-	-	-
Port F	-	-	-	PF12	PF11	PF10	-	-	-	-	PF5	-	-	PF2	PF1	PF0

5.9 EFM32LG380 (LQFP100)

5.9.1 Pinout

The EFM32LG380 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

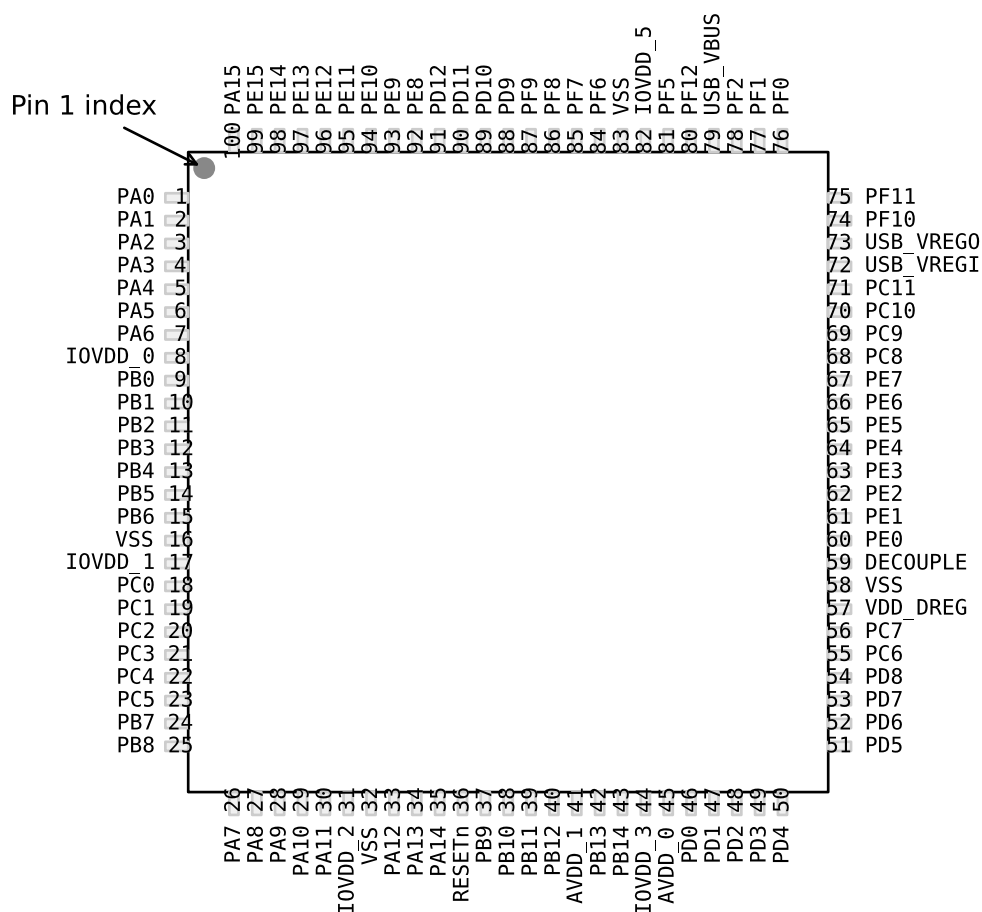


Figure 5.17. EFM32LG380 Pinout (top view, not to scale)

Table 5.25. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0		EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

5.12.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG840 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.36. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	—	—	—	—	—	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	PB12	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	PC15	PC14	PC13	PC12	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

5.12.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG840 is shown in the following figure.

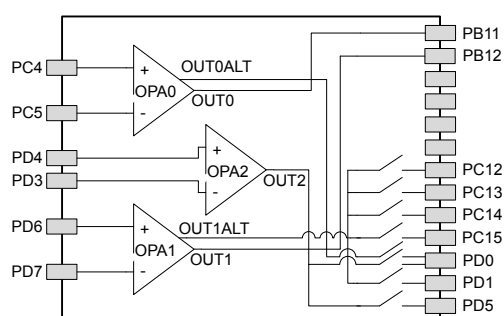


Figure 5.24. Opamp Pinout

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
47	AVDD_1	661.2	-2065.0	Analog power supply 1.				
48	AVSS_1	754.5	-2065.0	Analog ground 1.				
49	PB13	833.8	-2065.0	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
50	PB14	919.6	-2065.0	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
51	IOVSS_3	1054.9	-2065.0	Digital IO ground 3.				
52	IOVDD_3	1151.7	-2065.0	Digital IO power supply 3.				
53	AVSS_0	1254.2	-2065.0	Analog ground 0.				
54	AVDD_0	1346.8	-2065.0	Analog power supply 0.				
55	PD0	1442.7	-2065.0	ADC0_CH0 DAC0_OUT0ALT T #4/ OPAMP_OUT0 ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
56	PD1	1559.2	-2065.0	ADC0_CH1 DAC0_OUT1ALT T #4/ OPAMP_OUT1 ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
57	PD2	1646.3	-2065.0	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
58	PD3	1749.3	-2065.0	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
59	PD4	1851.4	-2065.0	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
60	PD5	2065.0	-1872.9	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
61	PD6	2065.0	-1771.3	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
62	PD7	2065.0	-1669.4	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
63	PD8	2065.0	-1561.9	BU_VIN				CMU_CLK1 #1
64	PC6	2065.0	-1470.2	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
65	PC7	2065.0	-1385.2	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
66	VSS_DREG	2065.0	-1295.5	Ground for on-chip voltage regulator.				

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0A LT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1A LT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN		PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN		PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1							Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3				PC2			Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4				PC3			Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12	PB2	PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.

14.2 Revision 1.31

December 16th, 2015

Removed Environmental section from General Operating Conditions.

Added max current consumption numbers for energy modes.

For devices with an ADC, added clarification on conditions for INL_{ADC} and DNL_{ADC} parameters.

For devices with an EBI, updated EBI ready/wait figure.

Updated memory map.

Removed DC_{HFRCO} and $DC_{AUXHFRCO}$ parameters.

For CSP81 package, updated typical and added min/max values for f_{HFRCO} and $f_{AUXHFRCO}$.

For devices in CSP81 package with a DAC, updated OPAMP table.

Fixed typos

Added OPAMP, ADC, and ACMP Input Bias Current and Input Offset Current specifications.

Added lower limit for GPIO Input Leakage Current and updated the upper limit for this specification.

Removed the "by simulation and/or technology characterization" phrase from the Electrical Characteristics Test Conditions section.

14.3 Revision 1.30

June 13th, 2014

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Removed "Preliminary" markings.

Updated electrical characteristics and updated/added plots.

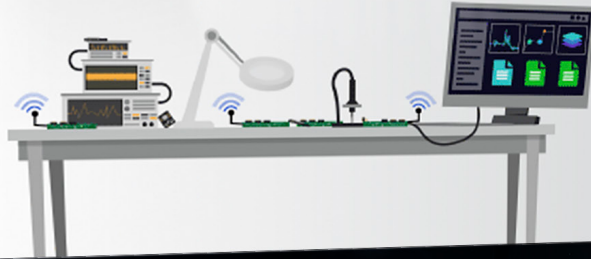
Updated orderable part numbers.

Added AUXHFRCO to block diagram and electrical characteristics.

For devices with EBI, added EBI timing chapter.

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