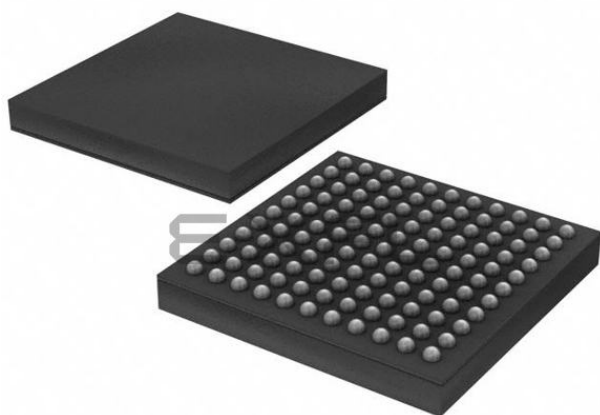




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg395f256-bga120

3.1.13 Inter-Integrated Circuit Interface (I2C)

The I²C module provides an interface between the MCU and a serial I²C-bus. It is capable of acting as both a master and a slave, and supports multi-master buses. Both standard-mode, fast-mode and fastmode plus speeds are supported, allowing transmission rates all the way from 10 kbit/s up to 1 Mbit/s. Slave arbitration and timeouts are also provided to allow implementation of an SMBus compliant system. The interface provided to software by the I²C module, allows both fine-grained control of the transmission process and close to automatic transfers. Automatic recognition of slave addresses is provided in all energy modes.

3.1.14 Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The Universal Synchronous Asynchronous serial Receiver and Transmitter (USART) is a very flexible serial I/O module. It supports full duplex asynchronous UART communication as well as RS-485, SPI, MicroWire and 3-wire. It can also interface with ISO7816 Smart-Cards, IrDA and I2S devices.

3.1.15 Pre-Programmed USB/UART Bootloader

The bootloader presented in application note AN0042 is pre-programmed in the device at factory. The bootloader enables users to program the EFM32 through a UART or a USB CDC class virtual UART without the need for a debugger. The autobaud feature, interface and commands are described further in the application note.

3.1.16 Universal Asynchronous Receiver/Transmitter (UART)

The Universal Asynchronous serial Receiver and Transmitter (UART) is a very flexible serial I/O module. It supports full- and half-duplex asynchronous UART communication.

3.1.17 Low Energy Universal Asynchronous Receiver/Transmitter (LEUART)

The unique LEUARTTM, the Low Energy UART, is a UART that allows two-way UART communication on a strict power budget. Only a 32.768 kHz clock is needed to allow UART communication up to 9600 baud/ s. The LEUART includes all necessary hardware support to make asynchronous serial communication possible with minimum of software intervention and energy consumption.

3.1.18 Timer/Counter (TIMER)

The 16-bit general purpose Timer has 3 compare/capture channels for input capture and compare/Pulse- Width Modulation (PWM) output. TIMER0 also includes a Dead-Time Insertion module suitable for motor control applications.

3.1.19 Real Time Counter (RTC)

The Real Time Counter (RTC) contains a 24-bit counter and is clocked either by a 32.768 kHz crystal oscillator, or a 32.768 kHz RC oscillator. In addition to energy modes EM0 and EM1, the RTC is also available in EM2. This makes it ideal for keeping track of time since the RTC is enabled in EM2 where most of the device is powered down.

3.1.20 Backup Real Time Counter (BURTC)

The Backup Real Time Counter (BURTC) contains a 32-bit counter and is clocked either by a 32.768 kHz crystal oscillator, a 32.768 kHz RC oscillator or a 1 kHz ULFRCO. The BURTC is available in all Energy Modes and it can also run in backup mode, making it operational even if the main power should drain out.

3.1.21 Low Energy Timer (LETIMER)

The unique LETIMERTM, the Low Energy Timer, is a 16-bit timer that is available in energy mode EM2 in addition to EM1 and EM0. Because of this, it can be used for timing and output generation when most of the device is powered down, allowing simple tasks to be performed while the power consumption of the system is kept at an absolute minimum. The LETIMER can be used to output a variety of waveforms with minimal software intervention. It is also connected to the Real Time Counter (RTC), and can be configured to start counting on compare matches from the RTC.

3.1.22 Pulse Counter (PCNT)

The Pulse Counter (PCNT) can be used for counting pulses on a single input or to decode quadrature encoded inputs. It runs off either the internal LFACLK or the PCNTn_S0IN pin as external clock source. The module may operate in energy mode EM0 - EM3.

3.2.3 EFM32LG280

The features of the EFM32LG280 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.3. EFM32LG280 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNCR, EBI_NANDREN, EBI_NANDWEN, EBI_REn, EBI_VSNCR, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

Module	Configuration	Pin Connections
AES	Full configuration	NA
GPIO	53 pins	Available pins are shown in 5.13.3 GPIO Pinout Overview
LCD	Full configuration	LCD_SEG[17:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

Module	Configuration	Pin Connections
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	85 pins	Available pins are shown in 5.14.3 GPIO Pinout Overview
LCD	Full configuration	LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

Module	Configuration	Pin Connections
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	90 pins	Available pins are shown in 5.15.3 GPIO Pinout Overview
LCD	Full configuration	LCD_SEG[35:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

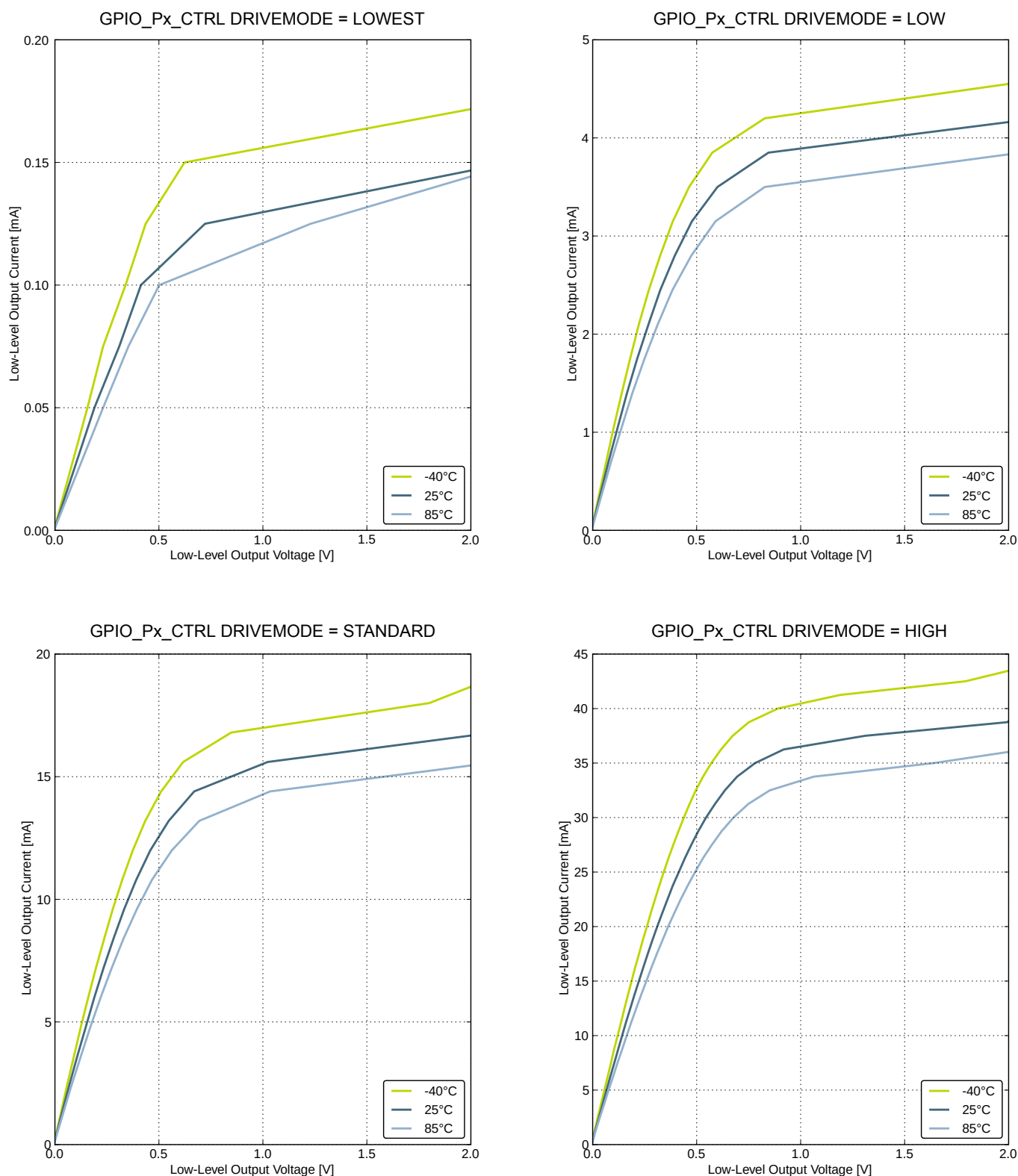


Figure 4.10. Typical Low-Level Output Current, 2V Supply Voltage

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range(SFDR)	SFDR _{DAC}	500 kSamples/s, 12 bit, single ended, internal 1.25V reference	—	62	—	dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference	—	56	—	dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference	—	61	—	dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference	—	55	—	dBc
		500 kSamples/s, 12 bit, differential, V _{DD} reference	—	60	—	dBc
Offset voltage, all packages except CSP	V _{DACOFF-SET}	After calibration, single ended	—	2	9	mV
		After calibration, differential	—	2	—	mV
Offset voltage, CSP devices	V _{DACOFF-SET}	After calibration, single ended	—	2	—	mV
		After calibration, differential	—	2	—	mV
Differential non-linearity	DNL _{DAC}		—	±1	—	LSB
Integral non-linearity	INL _{DAC}		—	±5	—	LSB
No missing codes	MC _{DAC}		—	12	—	bits
VREF output voltage	V _{REF}	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
VREF voltage drift	V _{REF_VDRIFT}	1.25 V reference	-12.4	2.3	18.2	mV/V
		2.5 V reference, VDD > 2.5 V	-24.6	5.3	35.2	mV/V
VREF temperature drift	V _{REF_TDRIFT}	1.25 V reference	-132	242	677	μV/°C
		2.5 V reference	-231	507	1271	μV/°C
VREF current consumption	I _{VREF}	1.25 V reference	—	67	97	μA
		2.5 V reference	—	55	72	μA
ADC and DAC VREF matching	V _{REF_MATCH}	1.25 V reference	—	99.85	—	%
		2.5 V reference	—	100.01	—	%

Note:

1. Measured with a static input code and no loading on the output. Includes required contribution from the voltage reference.

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative response time	$t_{\text{RESPONSE_N}}$	BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=0	—	353	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=1	—	547	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=2	—	578	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=3	—	627	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=4	—	670	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=5	—	741	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=6	—	811	—	ns
		BIASPROG=0b1111, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=7	—	926	—	ns

5.7 EFM32LG332 (TQFP64)

5.7.1 Pinout

The EFM32LG332 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

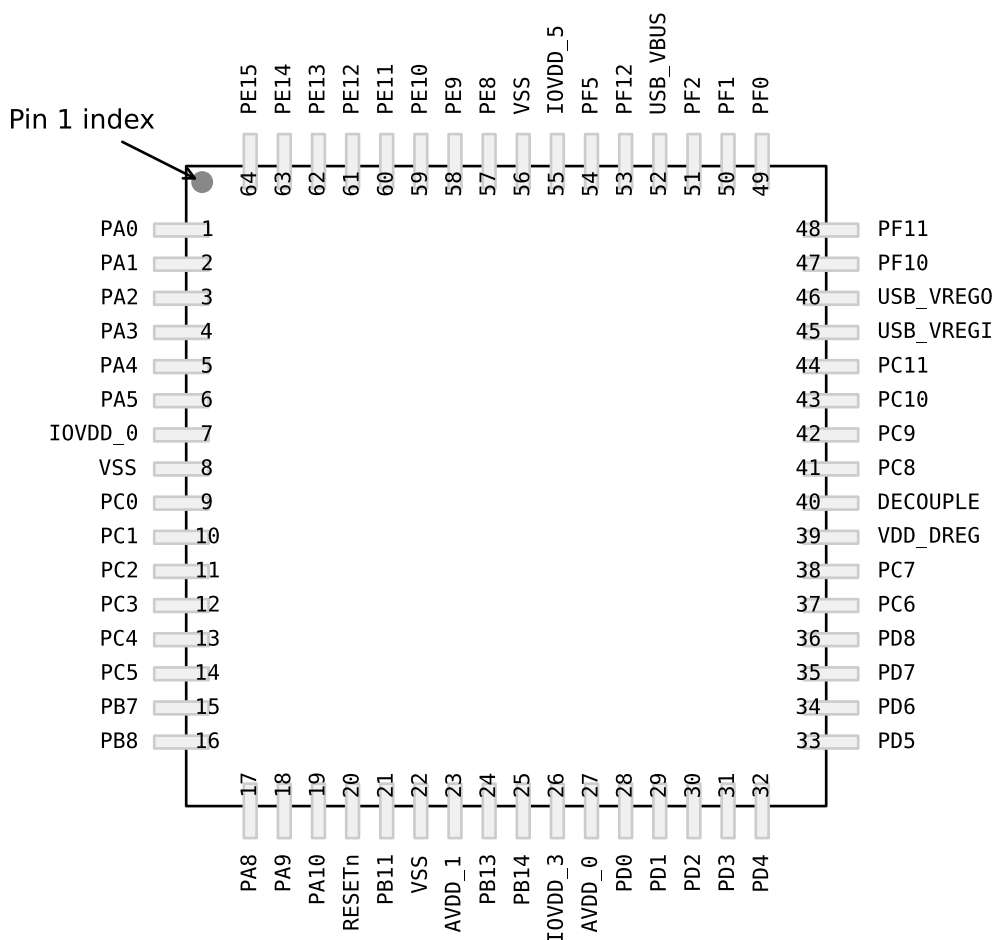


Figure 5.13. EFM32LG332 Pinout (top view, not to scale)

Table 5.19. Device Pinout

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
PCNT1_S0IN	PC4							Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5							Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1							Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3				PC2			Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4				PC3			Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8		PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9		PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10		PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
US0_CLK	PE12		PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13		PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11		PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10		PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
3	PA2		EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
4	PA3		EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
5	PA4		EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
6	PA5		EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	PA6		EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
8	IOVDD_0	Digital IO power supply 0.				
9	PB0		EBI_A16 #0/1/2	TIM1_CC0 #2		
10	PB1		EBI_A17 #0/1/2	TIM1_CC1 #2		
11	PB2		EBI_A18 #0/1/2	TIM1_CC2 #2		
12	PB3		EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
13	PB4		EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
14	PB5		EBI_A21 #0/1/2		US2_CLK #1	
15	PB6		EBI_A22 #0/1/2		US2_CS #1	
16	VSS	Ground.				
17	IOVDD_1	Digital IO power supply 1.				
18	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
19	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
20	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
21	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
22	PC4	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LE- TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
23	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
24	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
25	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
USB_VREGI	USB_V REGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_V REGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.10.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG390 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.30. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	—	—	—	—	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	—	—	PF2	PF1	PF0

5.10.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG390 is shown in the following figure.

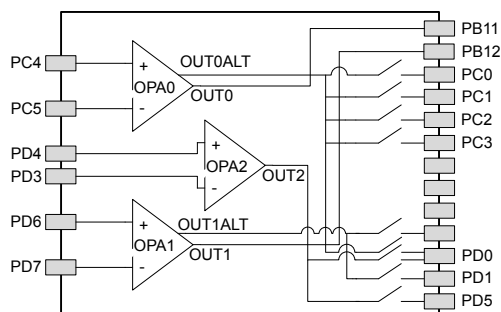


Figure 5.20. Opamp Pinout

5.15 EFM32LG890 (BGA112)

5.15.1 Pinout

The EFM32LG890 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

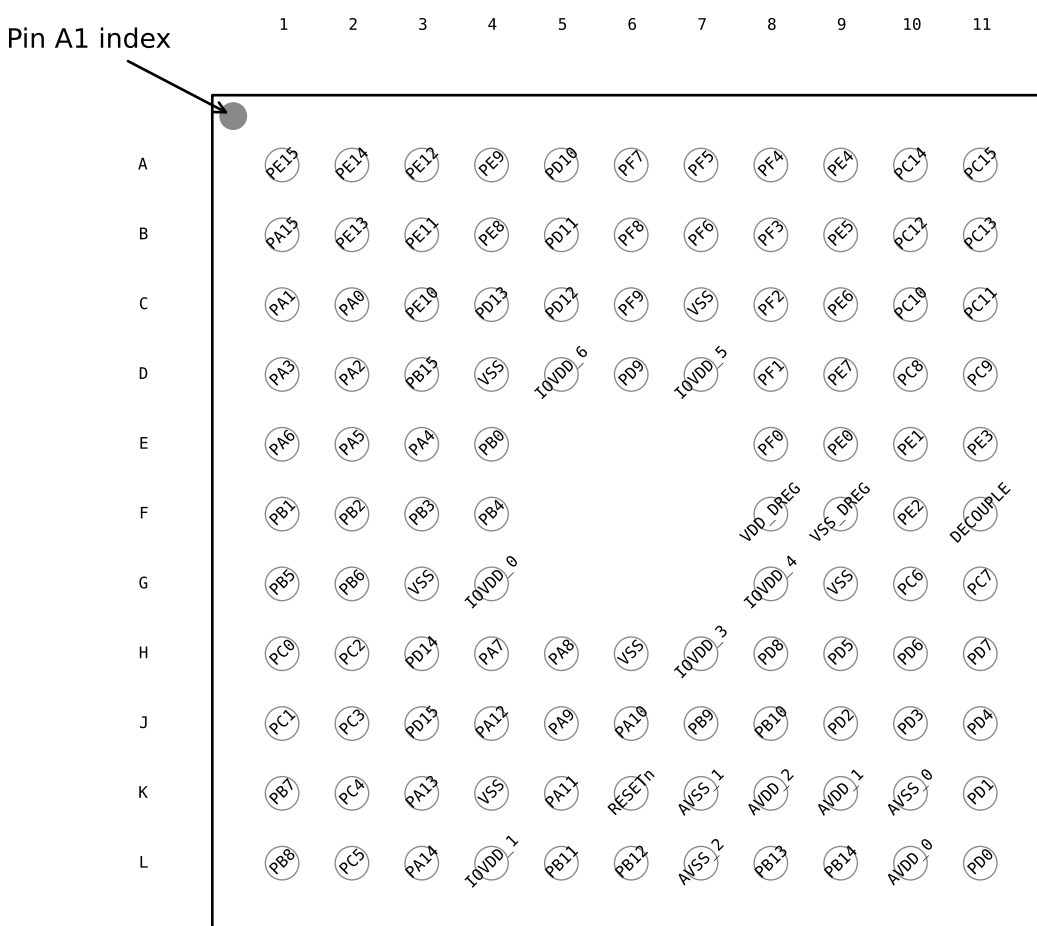


Figure 5.29. EFM32LG890 Pinout (top view, not to scale)

Table 5.43. Device Pinout

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
A2	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
L2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
L3	PA14	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
L6	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
L9	PB14	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
K13	PD8	BU_VIN				CMU_CLK1 #1
L1	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
L2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
L3	PA7	LCD_SEG35	EBI_CSTFT #0/1/2			
L4	IOVDD_5	Digital IO power supply 5.				
L5	VSS	Ground.				
L6	VSS	Ground.				
L7	IOVDD_6	Digital IO power supply 6.				
L8	PB9		EBI_A03 #0/1/2		U1_TX #2	
L9	PB10		EBI_A04 #0/1/2		U1_RX #2	
L10	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
L11	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
L12	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
L13	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
M1	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
M2	PC4	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LE- TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
M3	PA8	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
M4	PA10	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
M5	PA13	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
M6	PA14	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
M7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
M8	AVSS_1	Analog ground 1.				
M9	AVDD_2	Analog power supply 2.				

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
25	PC3	-2065.0	-1322.6	ACMP0_CH3 DAC0_OUT0ALT T #3/ OPAMP_OUT0 ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
26	PC4	-2065.0	-1484.3	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
27	PC5	-2065.0	-1586.5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
28	PB7	-2065.0	-1708.6	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
29	PB8	-2065.0	-1830.6	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
30	PA7	-1832.5	-2065.0	LCD_SEG35	EBI_CSTFT #0/1/2			
31	PA8	-1695.5	-2065.0	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
32	PA9	-1558.5	-2065.0	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
33	PA10	-1421.5	-2065.0	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
34	PA11	-1284.5	-2065.0	LCD_SEG39	EBI_HSNC #0/1/2			
35	IOVDD_2	-1147.5	-2065.0	Digital IO power supply 2.				
36	IOVSS_2	-1027.4	-2065.0	Digital IO ground 2.				
37	PA12	-907.2	-2065.0	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
38	PA13	-780.6	-2065.0	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
39	PA14	-654.0	-2065.0	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
40	RESETn	-527.4	-2065.0	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
41	PB9	-401.0	-2065.0		EBI_A03 #0/1/2		U1_TX #2	
42	PB10	-274.5	-2065.0		EBI_A04 #0/1/2		U1_RX #2	
43	PB11	260.7	-2065.0	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
44	PB12	366.0	-2065.0	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
45	AVSS_2	464.8	-2065.0	Analog ground 2.				
46	AVDD_2	560.5	-2065.0	Analog power supply 2.				

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4					UART0 Receive input.
U0_TX	PF6	PE0	PA3					UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX		PF11	PB10	PE3				UART1 Receive input.
U1_TX		PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.

10. TQFP64 Package Specifications

10.1 TQFP64 Package Dimensions

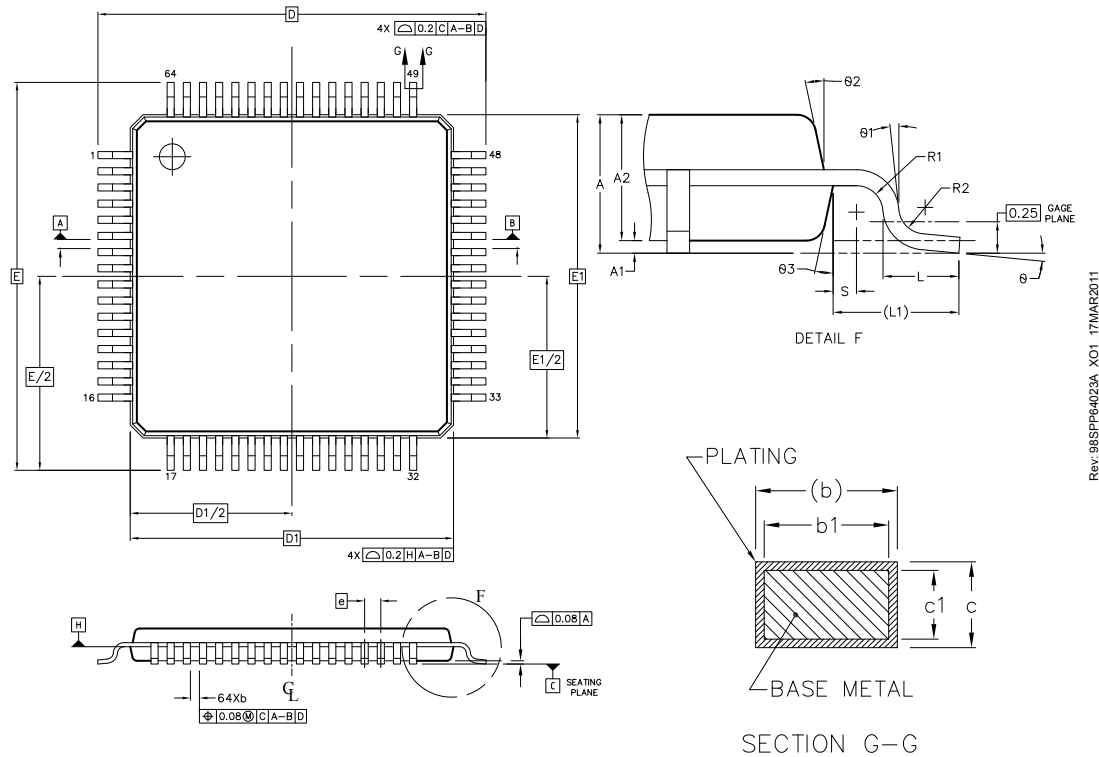


Figure 10.1. TQFP64

Note:

1. All dimensions & tolerancing confirm to ASME Y14.5M-1994.
2. The top package body size may be smaller than the bottom package body size.
3. Datum 'A,B', and 'B' to be determined at datum plane 'H'.
4. To be determined at seating place 'C'.
5. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25mm per side.'D1' and 'E1' are maximum plastic body size dimension including mold mismatch. Dimension 'D1' and 'E1' shall be determined at datum plane 'H'.
6. Detail of Pin 1 indicatifier are option all but must be located within the zone indicated.
7. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause thelead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be locatedon the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
8. Exact shape of each corner is optional.
9. These dimension apply to the flat section of the lead between 0.10 mm and 0.25 mm from the lead tip.
10. All dimensions are in millimeters.

Table 10.1. QFP64 (Dimensions in mm)

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
A	—	1.10	1.20	L1	—		
A1	0.05	—	0.15	R1	0.08	—	—
A2	0.95	1.00	1.05	R2	0.08	—	0.20

DIM	MIN	NOM	MAX	DIM	MIN	NOM	MAX
b	0.17	0.22	0.27	S	0.20	—	—
b1	0.17	0.20	0.23	θ	0°	3.5°	7°
c	0.09	—	0.20	θ1	0°	—	—
C1	0.09	—	0.16	θ2	11°	12°	13°
D	12.0 BSC			θ3	11°	12°	13°
D1	10.0 BSC						
e	0.50 BSC						
E	12.0 BSC						
E1	10.0 BSC						
L	0.45	0.60	0.75				

The TQFP64 Package is 10 by 10 mm in size and has a 0.5 mm pin pitch.

The TQFP64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.