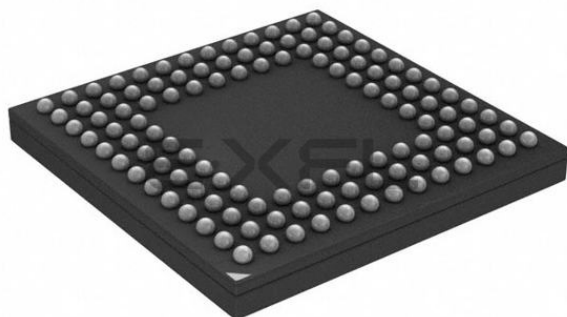




Welcome to [E-XFL.COM](https://www.e-xfl.com)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, POR, PWM, WDT
Number of I/O	93
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg395f64g-e-bga120

2. Ordering Information

The following table shows the available EFM32LG devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32LG230F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG230F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG230F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG232F64G-E-QFP64	64	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG232F128G-E-QFP64	128	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG232F256G-E-QFP64	256	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG280F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG280F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG280F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG290F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG290F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG290F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG295F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG295F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG295F256G-E-BGA120	256	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG330F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG330F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG330F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG332F64G-E-QFP64	64	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG332F128G-E-QFP64	128	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG332F256G-E-QFP64	256	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG360F64G-E-CSP81	64	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG360F128G-E-CSP81	128	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG360F256G-E-CSP81	256	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG380F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG380F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG380F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG390F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG390F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG390F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG395F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG395F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120

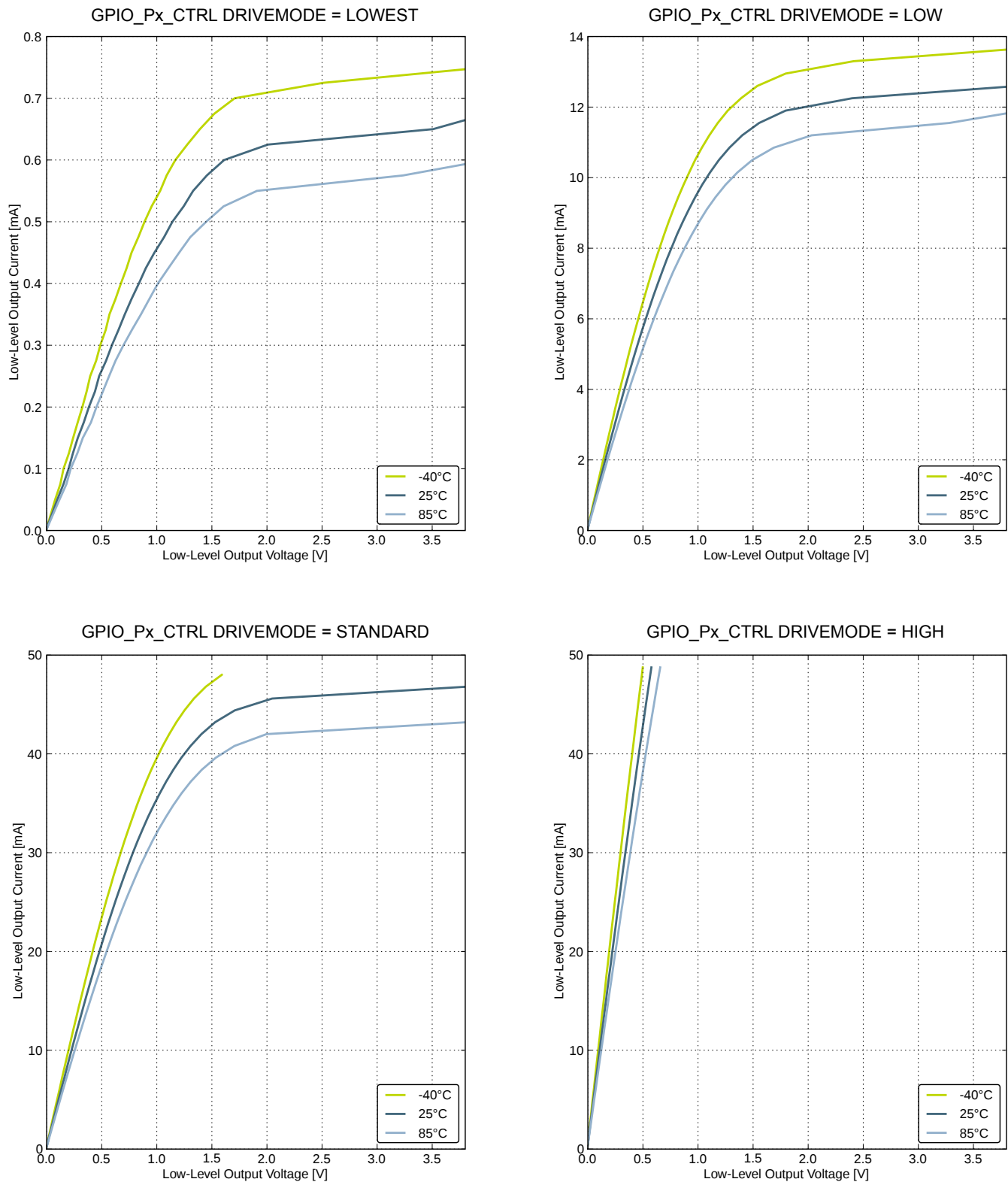


Figure 4.14. Typical Low-Level Output Current, 3.8 V Supply Voltage

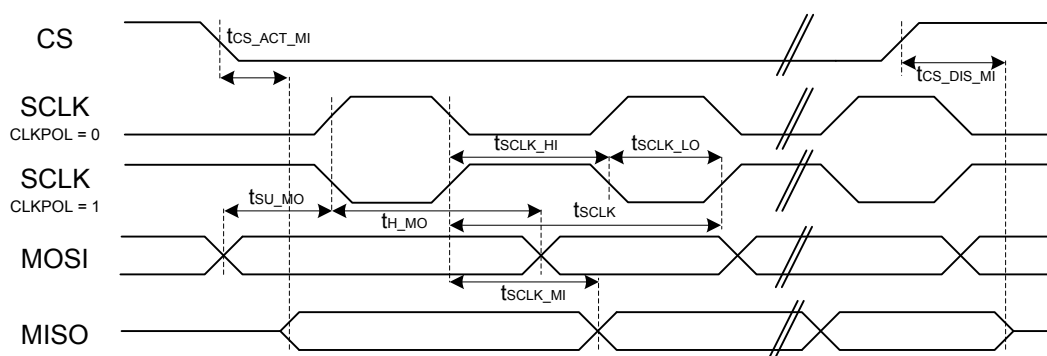


Figure 4.43. SPI Master Timing

Table 4.30. SPI Slave Timing

Parameter	Symbol	Min	Typ	Max	Unit
SCKL period	$t_{SCLK_sl}^{1\ 2}$	$6 \times t_{HFERCLK}$	—	—	ns
SCLK high period	$t_{SCLK_hi}^{1\ 2}$	$3 \times t_{HFERCLK}$	—	—	ns
SCLK low period	$t_{SCLK_lo}^{1\ 2}$	$3 \times t_{HFERCLK}$	—	—	ns
CS active to MISO	$t_{CS_ACT_MI}^{1\ 2}$	5.00	—	35.00	ns
CS disable to MISO high-impedance	$t_{CS_DIS_MI}^{1\ 2}$	5.00	—	35.00	ns
MOSI setup time	$t_{SU_MO}^{1\ 2}$	5.00	—	—	ns
MOSI hold time	$t_{H_MO}^{1\ 2}$	$2 + 2 \times t_{HFERCLK}$	—	—	ns
SCLK to MISO	$t_{SCLK_MI}^{1\ 2}$	$7 + t_{HFERCLK}$	—	$42 + 2 \times t_{HFERCLK}$	ns

Note:

1. Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)
2. Measurement done at 10% and 90% of V_{DD} (figure shows 50% of V_{DD})

Table 4.31. SPI Slave Timing with SSSEARLY and SMSDELAY

Parameter	Symbol	Min	Typ	Max	Unit
SCKL period	$t_{SCLK_sl}^{1\ 2}$	$6 \times t_{HFERCLK}$	—	—	ns
SCLK high period	$t_{SCLK_hi}^{1\ 2}$	$3 \times t_{HFERCLK}$	—	—	ns
SCLK low period	$t_{SCLK_lo}^{1\ 2}$	$3 \times t_{HFERCLK}$	—	—	ns
CS active to MISO	$t_{CS_ACT_MI}^{1\ 2}$	5.00	—	35.00	ns
CS disable to MISO	$t_{CS_DIS_MI}^{1\ 2}$	5.00	—	35.00	ns
MOSI setup time	$t_{SU_MO}^{1\ 2}$	5.00	—	—	ns
MOSI hold time	$t_{H_MO}^{1\ 2}$	$2 + 2 \times t_{HFERCLK}$	—	—	ns

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0A LT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1A LT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2	PC15	PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.

5.4.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.11. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
C5	VSS	Ground.				
C6	IOVDD_0	Digital IO power supply 0.				
C7	PF9		EBI_REn #1			ETM_TD0 #1
C8	VSS	Ground.				
C9	IOVDD_1	Digital IO power supply 1.				
C10	PF0			TIM0_CC0 #5 LE- TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
C11	PE4		EBI_A11 #0/1/2		US0_CS #1	
C12	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
C13	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
D1	PA3		EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
D2	PA2		EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
D3	PB15					ETM_TD2 #1
D11	PE5		EBI_A12 #0/1/2		US0_CLK #1	
D12	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
D13	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
E1	PA6		EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
E2	PA5		EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
E3	PA4		EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
E11	PE6		EBI_A13 #0/1/2		US0_RX #1	
E12	PC10	ACMP1_CH2	EBI_A10 #1/2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
E13	PC11	ACMP1_CH3	EBI_ALE #1/2		US0_TX #2	LES_CH11 #0
F1	PB0		EBI_A16 #0/1/2	TIM1_CC0 #2		
F2	PB1		EBI_A17 #0/1/2	TIM1_CC1 #2		
F3	PB2		EBI_A18 #0/1/2	TIM1_CC2 #2		

5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG395 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.15. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

5.5.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG295 is shown in the following figure.

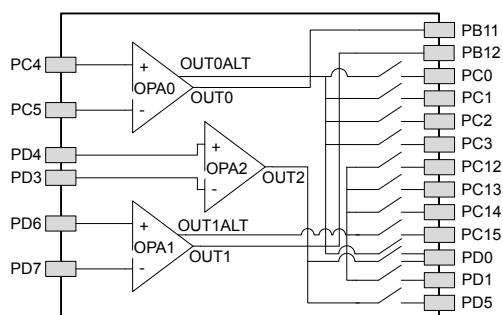


Figure 5.10. Opamp Pinout

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
G1	PB5		EBI_A21 #0/1/2		US2_CLK #1	
G2	PB6		EBI_A22 #0/1/2		US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				
G10	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
G11	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
H1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
H2	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
H3	PD14				I2C0_SDA #3	
H4	PA7		EBI_CSTFT #0/1/2			
H5	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8	BU_VIN				CMU_CLK1 #1
H9	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
H10	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
H11	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
J1	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
J2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
J3	PD15				I2C0_SCL #3	
J4	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
J5	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		

5.12.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.35. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_VIN	PD8							Battery input for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
50	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
51	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
52	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
53	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
54	PD8	BU_VIN				CMU_CLK1 #1
55	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
56	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
57	VDD_DREG	Power supply for on-chip voltage regulator.				
58	VSS	Ground.				
59	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
60	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
61	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
62	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
63	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
64	PE4	LCD_COM0	EBI_A11 #0/1/2		US0_CS #1	
65	PE5	LCD_COM1	EBI_A12 #0/1/2		US0_CLK #1	
66	PE6	LCD_COM2	EBI_A13 #0/1/2		US0_RX #1	
67	PE7	LCD_COM3	EBI_A14 #0/1/2		US0_TX #1	
68	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
69	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
70	PC10	ACMP1_CH2	EBI_A10 #1/2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
71	PC11	ACMP1_CH3	EBI_ALE #1/2		US0_TX #2	LES_CH11 #0
72	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
73	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0

5.15.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG890 is shown in the following figure.

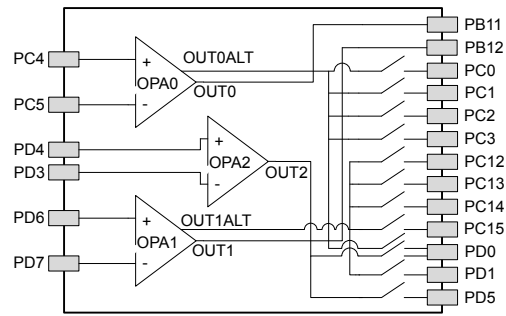


Figure 5.30. Opamp Pinout

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A3	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
A4	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
A5	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
A6	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
A7	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
A8	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
A9	PF4	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
A10	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
A11	USB_VREGI					
A12	USB_VREGO					
A13	PF11					
B1	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		
B2	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B3	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
B4	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
B5	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
B6	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
B7	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
B8	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
B9	PF3	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
B10	PF1			TIM0_CC1 #5 LE- TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
B11	PF12					
B12	USB_VBUS	USB 5.0 V VBUS input.				
B13	PF10				U1_TX #1	
C1	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C2	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
C3	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					ETM_TD1 #1

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN				PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN				PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1							Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3		PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2		PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3		PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3							Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4							Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12						Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13						Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14						Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
US0_CLK	PE12	PE5			PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4			PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6		PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
F11	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
G1	PB5	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
G2	PB6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				
G10	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
G11	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
H1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
H2	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
H3	PD14				I2C0_SDA #3	
H4	PA7	LCD_SEG35	EBI_CSTFT #0/1/2			
H5	PA8	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8	BU_VIN				CMU_CLK1 #1
H9	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
H10	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
H11	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
J1	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
J2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE		PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNCR	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREN	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEN	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REN	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNCR	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEN		PF8						External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.22.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG995 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.66. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

8. CSP81 Package Specifications

8.1 CSP81 Package Dimensions

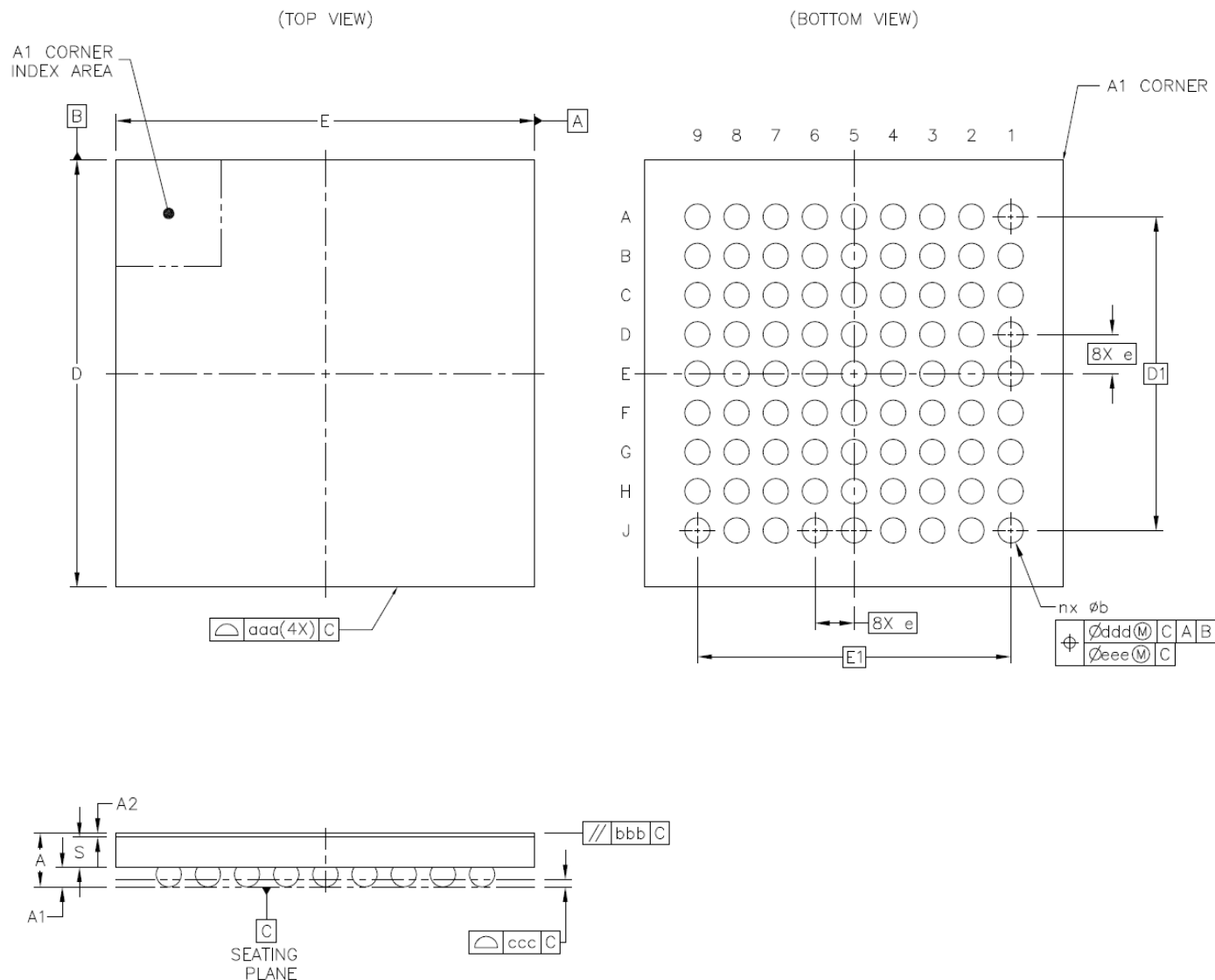


Figure 8.1. CSP81

Note:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Primary datum "C" and seating plane are defined by the spherical crowns of the solder balls.
4. Dimension "b" is measured at the maximum solder bump diameter, parallel to primary datum "C".
5. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

Table 8.1. CSP81 (Dimensions in mm)

Symbol	Min	Nom	Max
A	0.491	0.55	0.609
A1	0.17	—	0.23

10.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.

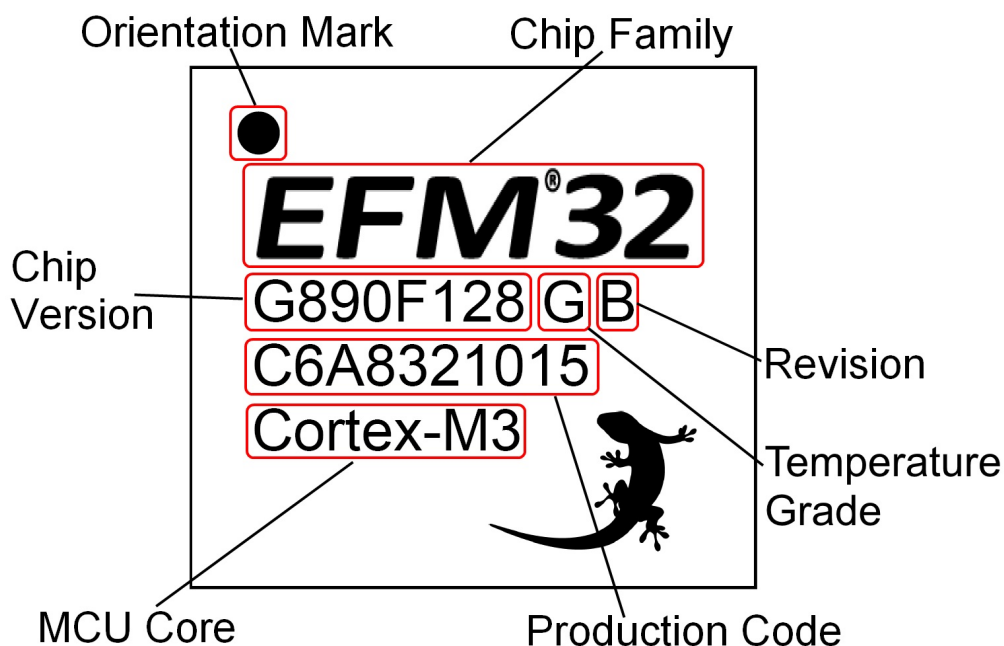


Figure 10.5. Example Chip Marking (Top View)