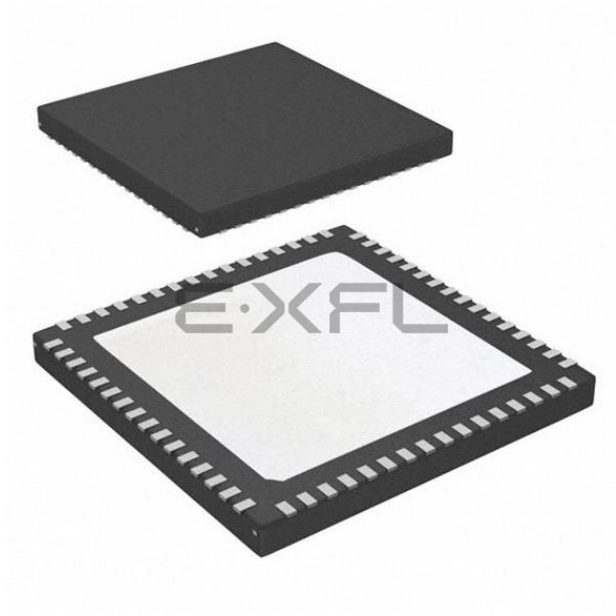
# Silicon Labs - EFM32LG840F256G-E-QFN64R Datasheet



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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Discontinued at Digi-Key |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 56 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 64-VFQFN Exposed Pad |
| Supplier Device Package | 64-QFN (9x9) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32lg840f256g-e-qfn64r |

| Module | Configuration | Pin Connections |
|---|---|---|
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |
| OPAMP | Full configuration | Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx |
| AES | Full configuration | NA |
| GPIO | 93 pins | Available pins are shown in 5.11.3 GPIO Pinout Overview |

### 3.2.18 EFM32LG940

The features of the EFM32LG940 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.18. EFM32LG940 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |
| ACMP1 | Full configuration | ACMP1_CH[7:0], ACMP1_O |
| VCMP | Full configuration | NA |
| ADC0 | Full configuration | ADC0_CH[7:0] |
| DAC0 | Full configuration | DAC0_OUT[1:0], DAC0_OUTxALT |

### 3.2.20 EFM32LG980

The features of the EFM32LG980 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.20. EFM32LG980 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

**Table 4.27. I2C Fast-mode Plus (Fm+)**

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| SCL clock frequency | $f_{SCL}$ | 0 | | 1000[1] | kHz |
| SCL clock low time | $t_{LOW}$ | 0.5 | | | µs |
| SCL clock high time | $t_{HIGH}$ | 0.26 | | | µs |
| SDA set-up time | $t_{SU,DAT}$ | 50 | | | ns |
| SDA hold time | $t_{HD,DAT}$ | 8 | | | ns |
| Repeated START condition set-up time | $t_{SU,STA}$ | 0.26 | | | µs |
| (Repeated) START condition hold time | $t_{HD,STA}$ | 0.26 | | | µs |
| STOP condition set-up time | $t_{SU,STO}$ | 0.26 | | | µs |
| Bus free time between a STOP and a START condition | $t_{BUF}$ | 0.5 | | | µs |

**Note:**
1. For the minimum HFPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32LG Reference Manual.

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A3 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| A4 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD10 | | EBI_CS1 #0/1/2 | | | |
| A6 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A7 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | | PRS_CH2 #1 |
| A8 | PF4 | | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A9 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| A10 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| A11 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| B1 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| B3 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD11 | | EBI_CS2 #0/1/2 | | | |
| B6 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B7 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B8 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| B9 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| B10 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| B11 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| C1 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| C2 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| C3 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C5 | VSS | Ground. | | | | |
| C6 | IOVDD_0 | Digital IO power supply 0. | | | | |
| C7 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |
| C8 | VSS | Ground. | | | | |
| C9 | IOVDD_1 | Digital IO power supply 1. | | | | |
| C10 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2 LEU0_TX #3 I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| C11 | PE4 | | EBI_A11 #0/1/2 | | US0_CS #1 | |
| C12 | PC14 | ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT | | TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0 | US0_CS #3 U0_TX #3 | LES_CH14 #0 |
| C13 | PC15 | ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT | | TIM0_CDTI2 #1/3 TIM1_CC2 #0 | US0_CLK #3 U0_RX #3 | LES_CH15 #0 DBG_SWO #1 |
| D1 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0 ETM_TD1 #3 |
| D2 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D11 | PE5 | | EBI_A12 #0/1/2 | | US0_CLK #1 | |
| D12 | PC12 | ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT | | | U1_TX #0 | CMU_CLK0 #1 LES_CH12 #0 |
| D13 | PC13 | ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT | | TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0 | U1_RX #0 | LES_CH13 #0 |
| E1 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| E2 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| E3 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0 ETM_TD2 #3 |
| E11 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| E12 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| E13 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| F1 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| F2 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| F3 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A3 | PE12 | | EBI_AD04 #0/1/2 | TIM1_CC2 #1 | US0_RX #3 US0_CLK #0 I2C0_SDA #6 | CMU_CLK1 #2 LES_ALTEX6 #0 |
| A4 | PE9 | | EBI_AD01 #0/1/2 | PCNT2_S1IN #1 | | |
| A5 | PD11 | | EBI_CS2 #0/1/2 | | | |
| A6 | PD9 | | EBI_CS0 #0/1/2 | | | |
| A7 | PF7 | | EBI_BL1 #0/1/2 | TIM0_CC1 #2 | U0_RX #0 | |
| A8 | PF5 | | EBI_REn #0/2 | TIM0_CDTI2 #2/5 | USB_VBUSEN #0 | PRS_CH2 #1 |
| A9 | PF4 | | EBI_WEn #0/2 | TIM0_CDTI1 #2/5 | | PRS_CH1 #1 |
| A10 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4 |
| A11 | USB_VREGI | | | | | |
| A12 | USB_VREGO | | | | | |
| A13 | PF11 | | | | U1_RX #1 USB_DP | |
| B1 | PA15 | | EBI_AD08 #0/1/2 | TIM3_CC2 #0 | | |
| B2 | PE13 | | EBI_AD05 #0/1/2 | | US0_TX #3 US0_CS #0 I2C0_SCL #6 | LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5 |
| B3 | PE11 | | EBI_AD03 #0/1/2 | TIM1_CC1 #1 | US0_RX #0 | LES_ALTEX5 #0 BOOT_RX |
| B4 | PE8 | | EBI_AD00 #0/1/2 | PCNT2_S0IN #1 | | PRS_CH3 #1 |
| B5 | PD12 | | EBI_CS3 #0/1/2 | | | |
| B6 | PD10 | | EBI_CS1 #0/1/2 | | | |
| B7 | PF8 | | EBI_WEn #1 | TIM0_CC2 #2 | | ETM_TCLK #1 |
| B8 | PF6 | | EBI_BL0 #0/1/2 | TIM0_CC0 #2 | U0_TX #0 | |
| B9 | PF3 | | EBI_ALE #0 | TIM0_CDTI0 #2/5 | | PRS_CH0 #1 ETM_TD3 #1 |
| B10 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2 LEU0_RX #3 I2C0_SCL #5 | DBG_SWDIO #0/1/2/3 GPIO_EM4WU3 |
| B11 | PF12 | | | | USB_ID | |
| B12 | USB_VBUS | USB 5.0 V VBUS input. | | | | |
| B13 | PF10 | | | | U1_TX #1 USB_DM | |
| C1 | PA1 | | EBI_AD10 #0/1/2 | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| C2 | PA0 | | EBI_AD09 #0/1/2 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| C3 | PE10 | | EBI_AD02 #0/1/2 | TIM1_CC0 #1 | US0_TX #0 | BOOT_TX |
| C4 | PD13 | | | | | ETM_TD1 #1 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LES_CH13 | PC13 | | | | | | | LESENSE channel 13. |
| LES_CH14 | PC14 | | | | | | | LESENSE channel 14. |
| LES_CH15 | PC15 | | | | | | | LESENSE channel 15. |
| LETIM0_OUT0 | PD6 | PB11 | PF0 | PC4 | | | | Low Energy Timer LETIM0, output channel 0. |
| LETIM0_OUT1 | PD7 | PB12 | PF1 | PC5 | | | | Low Energy Timer LETIM0, output channel 1. |
| LEU0_RX | PD5 | PB14 | PE15 | PF1 | PA0 | | | LEUART0 Receive input. |
| LEU0_TX | PD4 | PB13 | PE14 | PF0 | PF2 | | | LEUART0 Transmit output. Also used as receive input in half duplex communication. |
| LEU1_RX | PC7 | PA6 | | | | | | LEUART1 Receive input. |
| LEU1_TX | PC6 | PA5 | | | | | | LEUART1 Transmit output. Also used as receive input in half duplex communication. |
| LFXTAL_N | PB8 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin. |
| LFXTAL_P | PB7 | | | | | | | Low Frequency Crystal (typically 32.768 kHz) positive pin. |
| PCNT0_S0IN | PC13 | PE0 | PC0 | PD6 | | | | Pulse Counter PCNT0 input number 0. |
| PCNT0_S1IN | PC14 | PE1 | PC1 | PD7 | | | | Pulse Counter PCNT0 input number 1. |
| PCNT1_S0IN | PC4 | PB3 | | | | | | Pulse Counter PCNT1 input number 0. |
| PCNT1_S1IN | PC5 | PB4 | | | | | | Pulse Counter PCNT1 input number 1. |
| PCNT2_S0IN | PD0 | PE8 | | | | | | Pulse Counter PCNT2 input number 0. |
| PCNT2_S1IN | PD1 | PE9 | | | | | | Pulse Counter PCNT2 input number 1. |
| PRS_CH0 | PA0 | PF3 | | | | | | Peripheral Reflex System PRS, channel 0. |
| PRS_CH1 | PA1 | PF4 | | | | | | Peripheral Reflex System PRS, channel 1. |
| PRS_CH2 | PC0 | PF5 | | | | | | Peripheral Reflex System PRS, channel 2. |
| PRS_CH3 | PC1 | PE8 | | | | | | Peripheral Reflex System PRS, channel 3. |
| TIM0_CC0 | PA0 | PA0 | PF6 | PD1 | PA0 | PF0 | | Timer 0 Capture Compare input / output channel 0. |
| TIM0_CC1 | PA1 | PA1 | PF7 | PD2 | PC0 | PF1 | | Timer 0 Capture Compare input / output channel 1. |
| TIM0_CC2 | PA2 | PA2 | PF8 | PD3 | PC1 | PF2 | | Timer 0 Capture Compare input / output channel 2. |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_BCAP_N | PA13 | | | | | | | LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br><br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br><br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG1 | PF3 | | | | | | | LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG2 | PF4 | | | | | | | LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG12 | PA15 | | | | | | | LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |

### 5.13.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.38. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |

## 5.16 EFM32LG895 (BGA120)

### 5.16.1 Pinout

The EFM32LG895 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

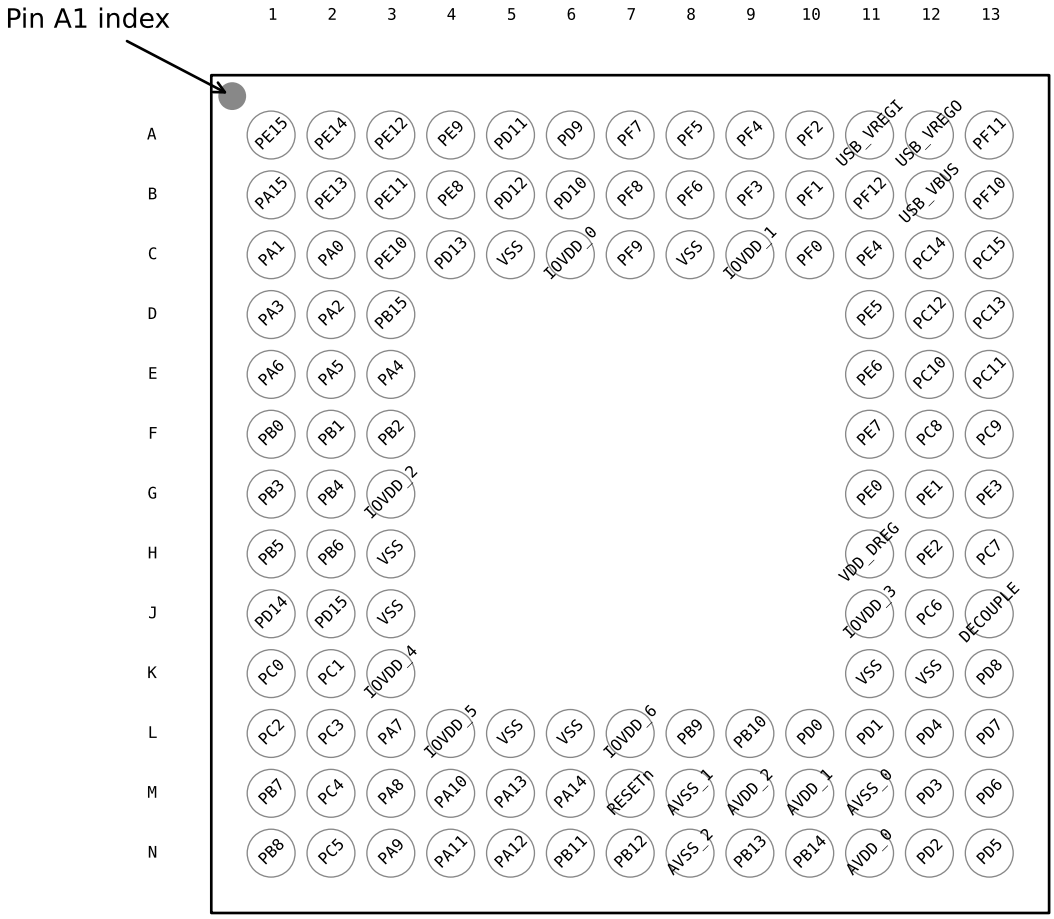


**Figure 5.31. EFM32LG895 Pinout (top view, not to scale)**

**Table 5.46. Device Pinout**

| BGA120 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| A1 | PE15 | LCD_SEG11 | EBI_AD07 #0/1/2 | TIM3_CC1 #0 | LEU0_RX #2 | |
| A2 | PE14 | LCD_SEG10 | EBI_AD06 #0/1/2 | TIM3_CC0 #0 | LEU0_TX #2 | |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | PF4 | PF8 | PF4 | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | PD13 | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |

### 5.17.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG900 is shown in the following figure.

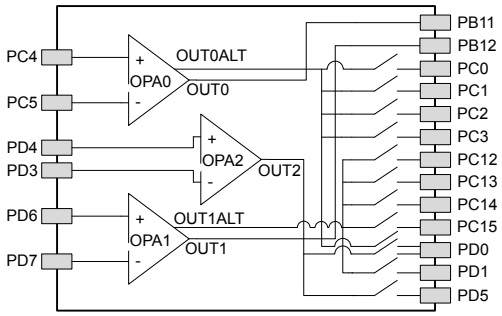


**Figure 5.34. Opamp Pinout**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |
| EBI_WEn | | PF8 | | | | | | External Bus Interface (EBI) Write Enable output. |
| ETM_TCLK | PD7 | PF8 | PC6 | PA6 | | | | Embedded Trace Module ETM clock . |
| ETM_TD0 | PD6 | PF9 | PC7 | PA2 | | | | Embedded Trace Module ETM data 0. |
| ETM_TD1 | PD3 | | PD3 | PA3 | | | | Embedded Trace Module ETM data 1. |
| ETM_TD2 | PD4 | | PD4 | PA4 | | | | Embedded Trace Module ETM data 2. |

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| F11 | DECOUPLE | Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin. | | | | |
| G1 | PB5 | LCD_SEG22/ LCD_COM6 | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| G2 | PB6 | LCD_SEG23/ LCD_COM7 | EBI_A22 #0/1/2 | | US2_CS #1 | |
| G3 | VSS | Ground. | | | | |
| G4 | IOVDD_0 | Digital IO power supply 0. | | | | |
| G8 | IOVDD_4 | Digital IO power supply 4. | | | | |
| G9 | VSS | Ground. | | | | |
| G10 | PC6 | ACMP0_CH6 | EBI_A05 #0/1/2 | | LEU1_TX #0 I2C0_SDA #2 | LES_CH6 #0 ETM_TCLK #2 |
| G11 | PC7 | ACMP0_CH7 | EBI_A06 #0/1/2 | | LEU1_RX #0 I2C0_SCL #2 | LES_CH7 #0 ETM_TD0 #2 |
| H1 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| H2 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| H3 | PD14 | | | | I2C0_SDA #3 | |
| H4 | PA7 | LCD_SEG35 | EBI_CSTFT #0/1/2 | | | |
| H5 | PA8 | LCD_SEG36 | EBI_DCLK #0/1/2 | TIM2_CC0 #0 | | |
| H6 | VSS | Ground. | | | | |
| H7 | IOVDD_3 | Digital IO power supply 3. | | | | |
| H8 | PD8 | BU_VIN | | | | CMU_CLK1 #1 |
| H9 | PD5 | ADC0_CH5 OPAMP_OUT2 #0 | | | LEU0_RX #0 | ETM_TD3 #0/2 |
| H10 | PD6 | ADC0_CH6 OPAMP_P1 | | TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3 | US1_RX #2 I2C0_SDA #1 | LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0 |
| H11 | PD7 | ADC0_CH7 OPAMP_N1 | | TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3 | US1_TX #2 I2C0_SCL #1 | CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0 |
| J1 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| J2 | PC3 | ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |

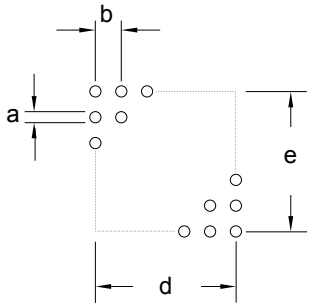


**Figure 7.4. BGA120 PCB Stencil Design**

**Table 7.3. BGA120 PCB Stencil Design Dimensions (Dimensions in mm)**

| Symbol | Dim. (mm) |
|---|---|
| a | 0.25 |
| b | 0.50 |
| d | 6.00 |
| e | 6.00 |

**Note:**

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

### 14.4 Revision 1.21

November 21st, 2013

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

For devices with a DAC, re-added missing DAC-data.

### 14.6 Revision 1.11

November 17th, 2010

This revision applies the following devices:

- EFM32G200
- EFM32G210
- EFM32G230
- EFM32G280
- EFM32G290
- EFM32G840
- EFM32G880
- EFM32G890

Corrected maximum DAC clock speed for continuous mode.

Added DAC sample-hold mode voltage drift rate.

Added pulse widths detected by the HFXO glitch detector.

Added power sequencing information to Power Management section.