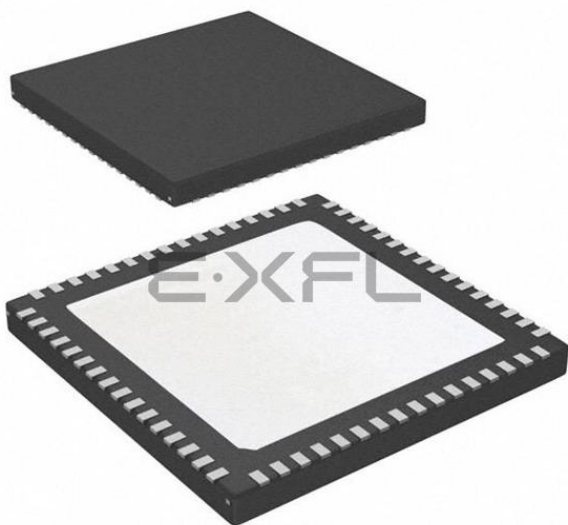




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg840f64g-e-qfn64r

3.2.17 EFM32LG900

The features of the EFM32LG900 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.17. EFM32LG900 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NAND-WEn, EBI_REn, EBI_VSNC, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O

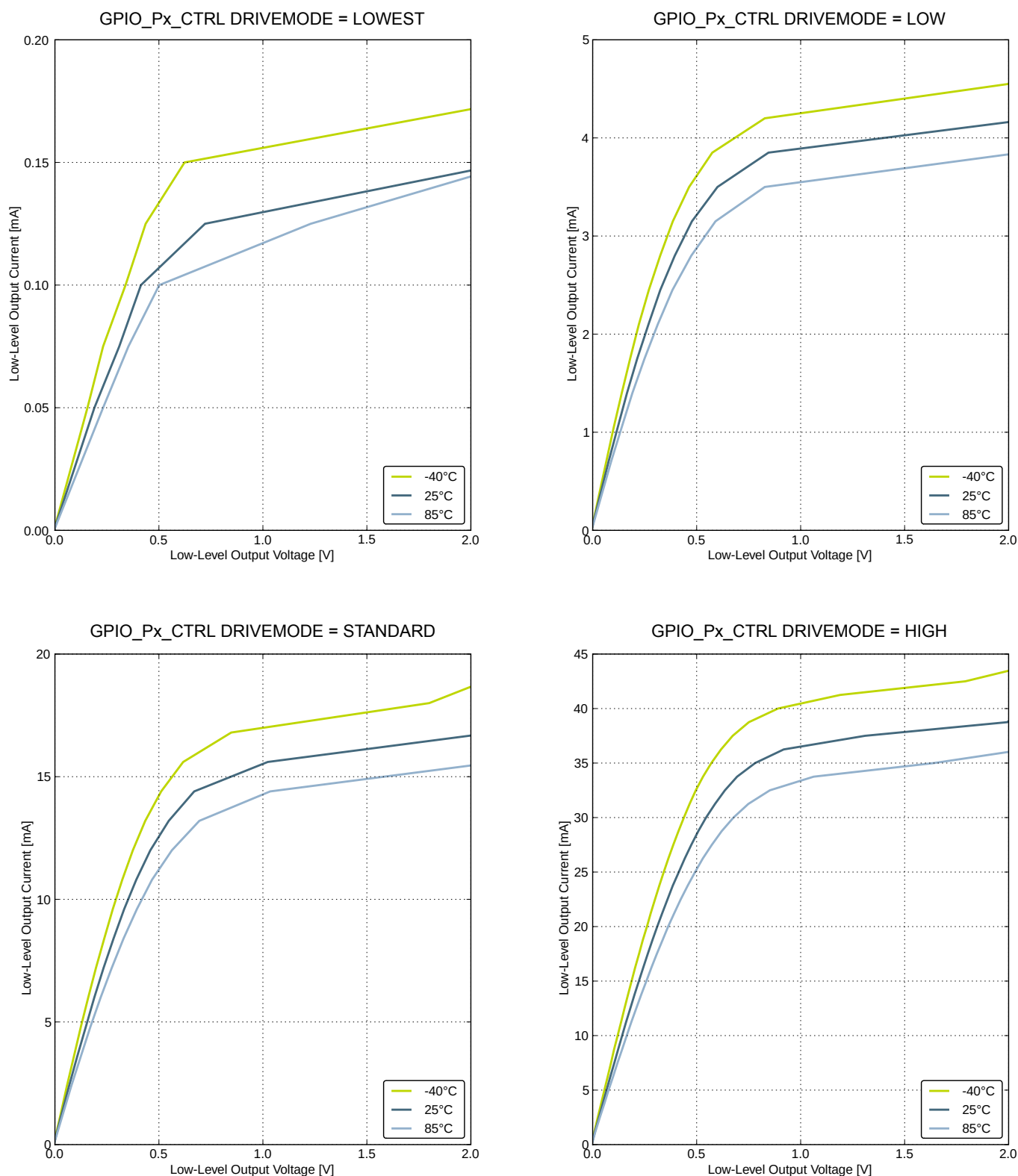


Figure 4.10. Typical Low-Level Output Current, 2V Supply Voltage

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Gain Bandwidth Product	GBW _{OPAMP}	(OPA0)BIASPROG=0x0,(OPA0)HALF-BIAS=0x1, DC bias = 0.3 V	—	0.393 ¹	—	MHz
		(OPA0)BIASPROG=0x0,(OPA0)HALF-BIAS=0x1, DC bias = 1 V	—	0.487 ¹	—	MHz
		(OPA0)BIASPROG=0x0,(OPA0)HALF-BIAS=0x1, DC bias = 2 V	—	0.392 ¹	—	MHz
		(OPA0)BIASPROG=0x0,(OPA0)HALF-BIAS=0x1, DC bias = 2.7 V	—	0.318 ¹	—	MHz
		(OPA0)BIASPROG=0x4,(OPA0)HALF-BIAS=0x1, DC bias = 0.3 V	—	1.595 ¹	—	MHz
		(OPA0)BIASPROG=0x4,(OPA0)HALF-BIAS=0x1, DC bias = 1 V	—	2.661 ¹	—	MHz
		(OPA0)BIASPROG=0x4,(OPA0)HALF-BIAS=0x1, DC bias = 2 V	—	2.566 ¹	—	MHz
		(OPA0)BIASPROG=0x4,(OPA0)HALF-BIAS=0x1, DC bias = 2.7 V	—	1.787 ¹	—	MHz
		(OPA1)BIASPROG=0x0,(OPA1)HALF-BIAS=0x1, DC bias = 0.3 V	—	0.460 ¹	—	MHz
		(OPA1)BIASPROG=0x0,(OPA1)HALF-BIAS=0x1, DC bias = 1 V	—	0.447 ¹	—	MHz
		(OPA1)BIASPROG=0x0,(OPA1)HALF-BIAS=0x1, DC bias = 2 V	—	0.372 ¹	—	MHz
		(OPA1)BIASPROG=0x0,(OPA1)HALF-BIAS=0x1, DC bias = 2.7 V	—	0.295 ¹	—	MHz
		(OPA1)BIASPROG=0x4,(OPA1)HALF-BIAS=0x1, DC bias = 0.3 V	—	1.890 ¹	—	MHz
		(OPA1)BIASPROG=0x4,(OPA1)HALF-BIAS=0x1, DC bias = 1 V	—	2.849 ¹	—	MHz
		(OPA1)BIASPROG=0x4,(OPA1)HALF-BIAS=0x1, DC bias = 2 V	—	2.561 ¹	—	MHz
		(OPA1)BIASPROG=0x4,(OPA1)HALF-BIAS=0x1, DC bias = 2.7 V	—	1.705 ¹	—	MHz
		(OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, DC bias = 0.3 V	—	0.339 ¹	—	MHz
		(OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, DC bias = 1 V	—	0.432 ¹	—	MHz
		(OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, DC bias = 2 V	—	0.347 ¹	—	MHz
		(OPA2)BIASPROG=0x0,(OPA2)HALF-BIAS=0x1, DC bias = 2.7 V	—	0.286 ¹	—	MHz
		(OPA2)BIASPROG=0x4,(OPA2)HALF-BIAS=0x1, DC bias = 0.3 V	—	1.271 ¹	—	MHz
		(OPA2)BIASPROG=0x4,(OPA2)HALF-BIAS=0x1, DC bias = 1 V	—	1.429 ¹	—	MHz
		(OPA2)BIASPROG=0x4,(OPA2)HALF-BIAS=0x1, DC bias = 2 V	—	1.283 ¹	—	MHz

4.14 Voltage Comparator (VCMP)

Table 4.18. VCMP

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input voltage range	V _{VCMPIN}		—	V _{DD}	—	V
VCMP Common Mode voltage range	V _{VCMPCM}		—	V _{DD}	—	V
Active current	I _{VCMP}	BIASPROG=0b0000 and HALF-BIAS=1 in VCMPn_CTRL register	—	0.3 ¹	0.6 ¹	μA
		BIASPROG=0b1111 and HALF-BIAS=0 in VCMPn_CTRL register. LPREF=0.	—	22 ¹	35 ¹	μA
Startup time reference generator	t _{VCMPREF}	NORMAL	—	10	—	μs
Offset voltage	V _{VCMPOFFSET}	Single ended	—	10	—	mV
		Differential	—	10	—	mV
Negative hysteresis	V _{VCMPHYST_N}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1	-46.6	-15.6	11.4	mV
Positive hysteresis	V _{VCMPHYST_P}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1	-7.5	23.4	46.6	mV
Hysteresis delta	V _{VCMPHYST_DELTA}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1	4.2	35.2	70.0	mV
Startup time	t _{VCMPSTART}		—	—	10	μs
Negative response time	t _{RESPONSE_N}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1, HYS-TSEL=0	—	372.3	—	μs
Positive response time	t _{RESPONSE_P}	BIASPROG=0b0000, HALF-BIAS=1, LPREF=1, HYS-TSEL=0	—	865.7	—	μs
Note: 1. Includes required contribution from the voltage reference.						

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

$$V_{DD} \text{ Trigger Level} = 1.667V + 0.034 \times \text{TRIGLEVEL}$$

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A3	PE12		EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
A4	PE9		EBI_AD01 #0/1/2	PCNT2_S1IN #1		
A5	PD10		EBI_CS1 #0/1/2			
A6	PF7		EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
A7	PF5		EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
A8	PF4		EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
A9	PE4		EBI_A11 #0/1/2		US0_CS #1	
A10	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
A11	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
B1	PA15		EBI_AD08 #0/1/2	TIM3_CC2 #0		
B2	PE13		EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B3	PE11		EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
B4	PE8		EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
B5	PD11		EBI_CS2 #0/1/2			
B6	PF8		EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
B7	PF6		EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
B8	PF3		EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
B9	PE5		EBI_A12 #0/1/2		US0_CLK #1	
B10	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
B11	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
C1	PA1		EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C2	PA0		EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
C3	PE10		EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					ETM_TD1 #1

5.5.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG395 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.15. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	PC15	PC14	PC13	PC12	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	PF4	PF3	PF2	PF1	PF0

5.5.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG295 is shown in the following figure.

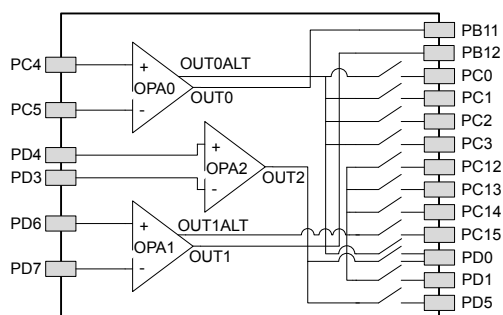


Figure 5.10. Opamp Pinout

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7		PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6		PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.

5.15.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.44. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0A LT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1A LT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.

5.16 EFM32LG895 (BGA120)

5.16.1 Pinout

The EFM32LG895 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

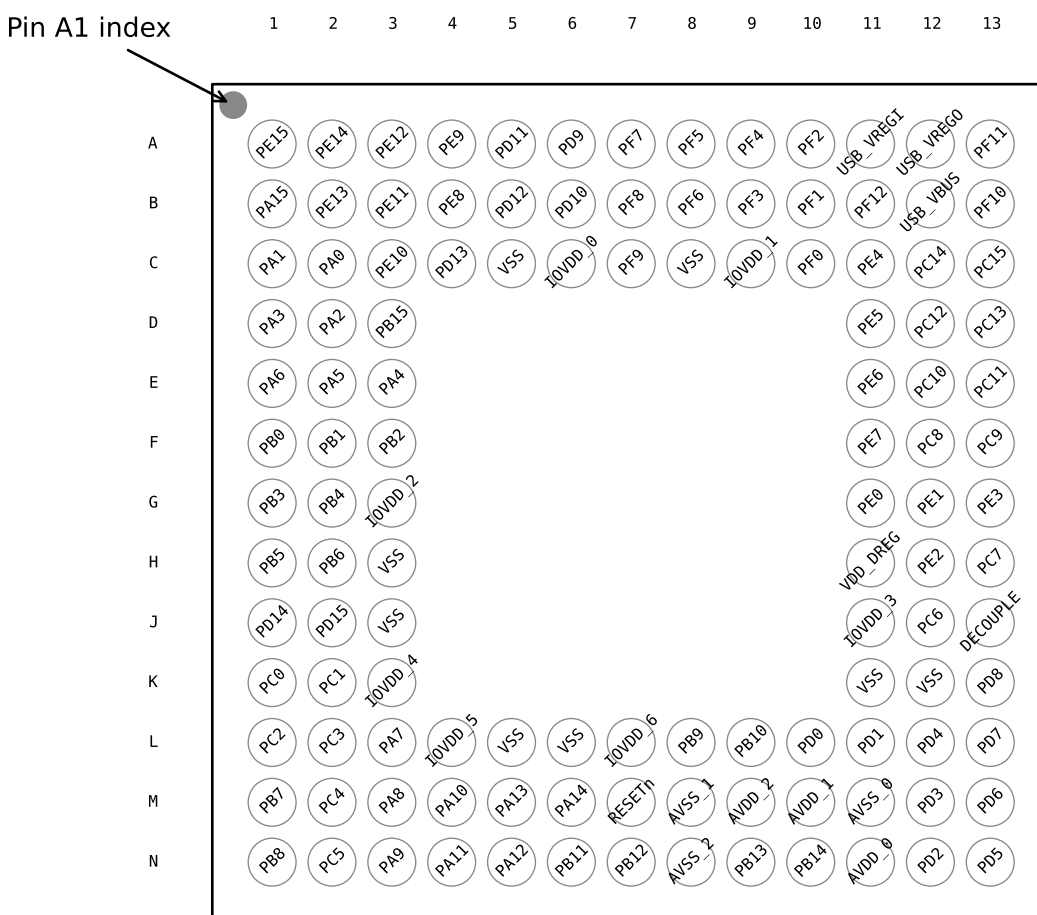


Figure 5.31. EFM32LG895 Pinout (top view, not to scale)

Table 5.46. Device Pinout

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
A2	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
M10	AVDD_1	Analog power supply 1.				
M11	AVSS_0	Analog ground 0.				
M12	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
M13	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
N1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
N2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
N3	PA9	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
N4	PA11	LCD_SEG39	EBI_HSNC #0/1/2			
N5	PA12	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
N6	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
N7	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
N8	AVSS_2	Analog ground 2.				
N9	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
N10	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
N11	AVDD_0	Analog power supply 0.				
N12	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	US1_CLK #1	DBG_SWO #3
N13	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
4	PA3	-2065.0	1439.7	LCD_SEG16	EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
5	PA4	-2065.0	1307.2	LCD_SEG17	EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
6	PA5	-2065.0	1174.7	LCD_SEG18	EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
7	PA6	-2065.0	1042.3	LCD_SEG19	EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU 1
8	IOVDD_0	-2065.0	909.8	Digital IO power supply 0.				
9	IOVSS_0	-2065.0	630.9	Digital IO ground 0.				
10	PD14	-2065.0	550.5				I2C0_SDA #3	
11	PD15	-2065.0	451.0				I2C0_SCL #3	
12	PB0	-2065.0	352.7	LCD_SEG32	EBI_A16 #0/1/2	TIM1_CC0 #2		
13	PB1	-2065.0	249.0	LCD_SEG33	EBI_A17 #0/1/2	TIM1_CC1 #2		
14	PB2	-2065.0	107.0	LCD_SEG34	EBI_A18 #0/1/2	TIM1_CC2 #2		
15	NC	-2065.0	-40.8	Do not connect.				
16	PB3	-2065.0	-215.2	LCD_SEG20/ LCD_COM4	EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
17	PB4	-2065.0	-347.7	LCD_SEG21/ LCD_COM5	EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
18	PB5	-2065.0	-504.7	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
19	PB6	-2065.0	-612.6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
20	IOVSS_1	-2065.0	-745.0	Digital IO ground 1.				
21	IOVDD_1	-2065.0	-860.7	Digital IO power supply 1.				
22	PC0	-2065.0	-994.8	ACMP0_CH0 DAC0_OUT0ALT T #0/ OPAMP_OUT0 ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
23	PC1	-2065.0	-1098.4	ACMP0_CH1 DAC0_OUT0ALT T #1/ OPAMP_OUT0 ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
24	PC2	-2065.0	-1220.4	ACMP0_CH2 DAC0_OUT0ALT T #2/ OPAMP_OUT0 ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
DAC0_OUT0ALT / OPAMP_OUT0A LT					PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1A LT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
ETM_TCLK	PD7		PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6		PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7			PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6			PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12						I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.
LES_CH9	PC9							LESENSE channel 9.
LES_CH10	PC10							LESENSE channel 10.
LES_CH11	PC11							LESENSE channel 11.
LES_CH12	PC12							LESENSE channel 12.
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.

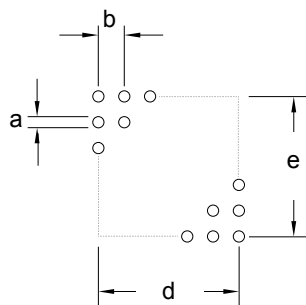


Figure 7.4. BGA120 PCB Stencil Design

Table 7.3. BGA120 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.25
b	0.50
d	6.00
e	6.00

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

13. Chip Revision, Solder Information, Errata

13.1 Chip Revision

The revision of a chip can be determined from the "Revision" field in the package marking.

13.2 Soldering Information

The latest IPC/JEDEC J-STD-020 recommendations for Pb-Free reflow soldering should be followed.

13.3 Errata

Please see the errata document for description and resolution of device errata. This document is available in Simplicity Studio and on-line at: <http://www.silabs.com/support/pages/document-library.aspx?p=MCUs--32-bit>

- VREF voltage drift (V_{REF_VDRIFT}) – added min, typ, max.
- VREF temperature drift (V_{REF_TDRIFT}) – added min, typ, max.
- VREF current consumption (I_{VREF}) – added typ, max, replacing I_{ADCREF} .
- ADC and DAC VREF matching (V_{REF_MATCH}) – added typical.

4.11 Digital Analog Converter (DAC) – Updated the footnote for active average current (I_{DAC}), and added the following new VREF specs at each voltage reference:

- VREF output voltage (V_{REF}) – added min, typ, max.
- VREF voltage drift (V_{REF_VDRIFT}) – added min, typ, max.
- VREF temperature drift (V_{REF_TDRIFT}) – added min, typ, max.
- VREF current consumption (I_{VREF}) – added typ, max.
- ADC and DAC VREF matching (V_{REF_MATCH}) – added typical.

4.12 Operational Amplifier (OPAMP) – Removed note specifying that OPAMP specs stem from simulations, and added new specifications for the following:

- Active Current (I_{OPAMP}) – new specifications at various (new) bias program settings.
- Gain Bandwidth Product (GBW_{OPAMP}) – new (typ) specifications at new bias program settings and DC bias settings.
- Input Offset Voltage (V_{OFFSET}) – specified min, typ, max for Op Amps (OPA0-1).
- Input Bias Current ($I_{OPAMPBIASIN}$) – new min and max specifications.
- Input Offset Current ($I_{OPAMPOFF-SETIN}$) – new min and max specifications.
- Slew Rate (SR_{OPAMP}) – new specifications at new bias program settings.
- Updated footnote.

4.13 Analog Comparator (ACMP) – Added new specifications for the following:

- Input Bias Current ($I_{ACMPBIASIN}$) – added min and max.
- Input Offset Current ($I_{ACMPOFFSETIN}$) – added min and max.
- Active Current (I_{ACMP}) – added two new condition settings, and footnote.
- Negative Response Time ($t_{RESPONSE_N}$) – added new specifications.
- Positive Response Times ($t_{RESPONSE_P}$) – added new specifications.
- Offset Voltage ($V_{ACMPOFFSET}$) – added specifications at new bias program settings.
- ACMP Hysteresis ($V_{ACMPHYST}$) – added specifications for negative and positive hysteresis at various bias program settings.
- VDD SCALED Input Accuracy ($V_{VDDSCALED}$) – added new specifications (typical).

4.14 Voltage Comparator (VCMP) – Added the following new specifications:

- Negative hysteresis ($V_{VCMPHYST_N}$), replacing VCMP hysteresis.
- Positive hysteresis ($V_{VCMPHYST_P}$), replacing VCMP hysteresis.
- Hysteresis Delta ($V_{VCMPHYST_DELTA}$).
- Negative Response Time ($t_{RESPONSE_N}$).
- Positive Response Time ($t_{RESPONSE_P}$).
- Footnote for active current, I_{VCMP} .

4.18 USART SPI – Corrected parameter descriptions for $t_{CS_DIS_MI}$.

4.19 Digital Peripherals – Added (typical) LE Peripheral Interface Clock Current (I_{LFCLK}) specifications with both the LFXO-LFA and LFXO-LFB clock trees.

Removed MSL information (Moisture Sensitivity Level). Instead, MSL information can be found in the Qual report that is available on the Silicon Labs website.

New formatting throughout.