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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg880f128-qfp100t

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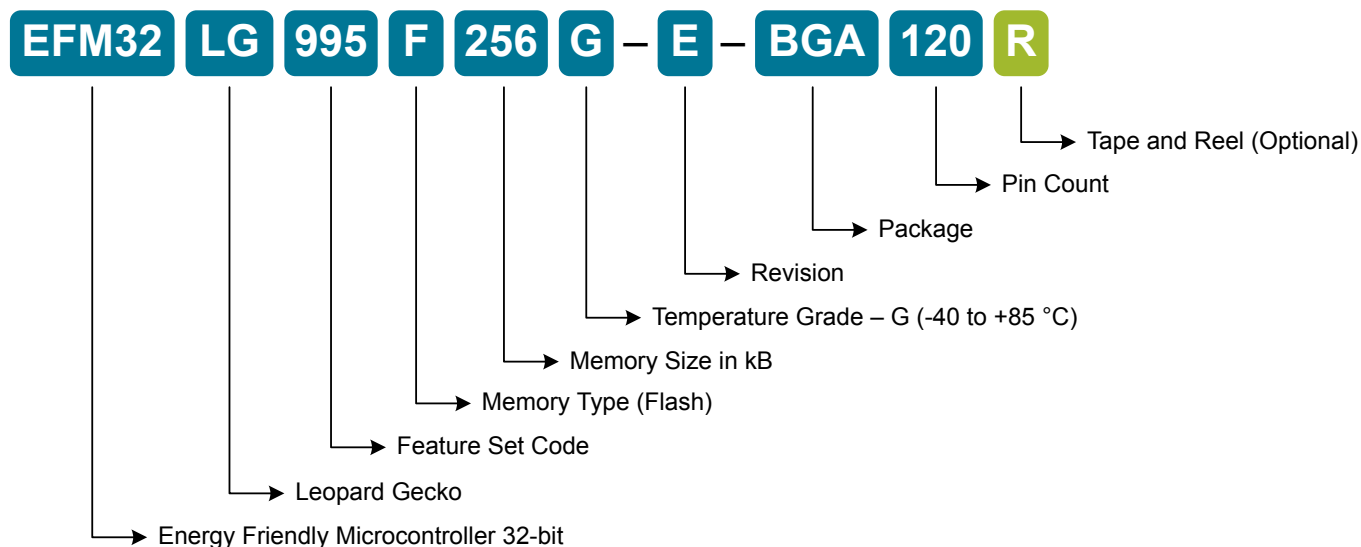


Figure 2.1. Ordering Code Decoder

Adding the suffix 'R' to the part number (e.g. EFM32LGF256G-E-BGA120R) denotes tape and reel.

Visit <http://www.silabs.com> for information on global distributors and representatives.

Module	Configuration	Pin Connections
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	86 pins	Available pins are shown in 5.10.3 GPIO Pinout Overview

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: 1. Measured with 70 pF load capacitance, 25 °C, and 3 V, using a 100 mV p-p amplitude on the input signal. 2. Simulated with 70 pF load capacitance, 25 °C, and 3 V, using a 1 mV p-p amplitude on the input signal.						

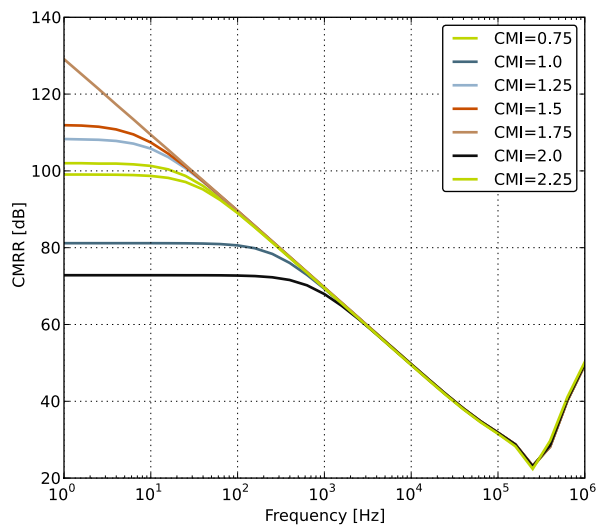


Figure 4.31. OPAMP Common Mode Rejection Ratio

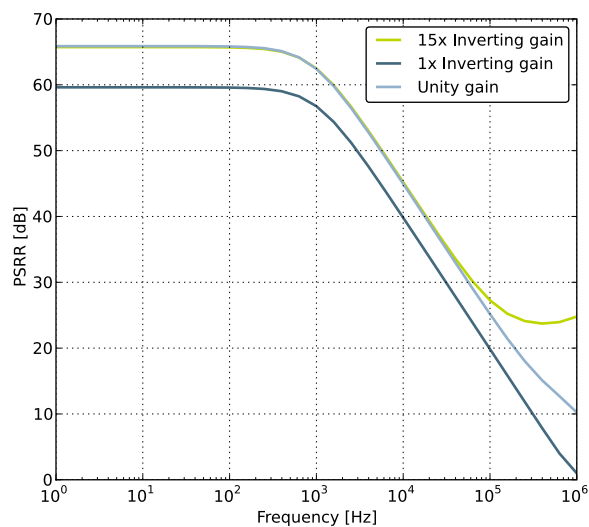


Figure 4.32. OPAMP Positive Power Supply Rejection Ratio

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
25	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
30	PD2	ADC0_CH2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
31	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 OPAMP_P1	TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 OPAMP_N1	TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
44	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0
45	USB_VREGI				
46	USB_VREGO				
47	PF10			USB_DM	
48	PF11			USB_DP	
49	PF0		TIM0_CC0 #5 LE- TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4							USART2 clock input / output.
US2_CS	PC5							USART2 chip select input / output.
US2_RX	PC3							USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2							USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.11.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.32. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15				UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14				UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX	PC13	PF11	PB10	PE3				UART1 Receive input.
U1_TX	PC12	PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
US0_RX	PE11	PE6		PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7		PE13	PB7			USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX		PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX		PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX		PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX		PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).

5.13.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG842 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.39. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	PA14	PA13	PA12	—	—	—	—	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	PC15	PC14	PC13	PC12	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	—	—	—	—	—	—	—	PF5	PF4	PF3	PF2	PF1	PF0

5.15.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.44. Alternate functionality overview

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
25	PC3	-2065.0	-1322.6	ACMP0_CH3 DAC0_OUT0ALT T #3/ OPAMP_OUT0 ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
26	PC4	-2065.0	-1484.3	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
27	PC5	-2065.0	-1586.5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
28	PB7	-2065.0	-1708.6	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
29	PB8	-2065.0	-1830.6	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
30	PA7	-1832.5	-2065.0	LCD_SEG35	EBI_CSTFT #0/1/2			
31	PA8	-1695.5	-2065.0	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
32	PA9	-1558.5	-2065.0	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
33	PA10	-1421.5	-2065.0	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
34	PA11	-1284.5	-2065.0	LCD_SEG39	EBI_HSNC #0/1/2			
35	IOVDD_2	-1147.5	-2065.0	Digital IO power supply 2.				
36	IOVSS_2	-1027.4	-2065.0	Digital IO ground 2.				
37	PA12	-907.2	-2065.0	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
38	PA13	-780.6	-2065.0	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
39	PA14	-654.0	-2065.0	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
40	RESETn	-527.4	-2065.0	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
41	PB9	-401.0	-2065.0		EBI_A03 #0/1/2		U1_TX #2	
42	PB10	-274.5	-2065.0		EBI_A04 #0/1/2		U1_RX #2	
43	PB11	260.7	-2065.0	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
44	PB12	366.0	-2065.0	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
45	AVSS_2	464.8	-2065.0	Analog ground 2.				
46	AVDD_2	560.5	-2065.0	Analog power supply 2.				

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
47	AVDD_1	661.2	-2065.0	Analog power supply 1.				
48	AVSS_1	754.5	-2065.0	Analog ground 1.				
49	PB13	833.8	-2065.0	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
50	PB14	919.6	-2065.0	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
51	IOVSS_3	1054.9	-2065.0	Digital IO ground 3.				
52	IOVDD_3	1151.7	-2065.0	Digital IO power supply 3.				
53	AVSS_0	1254.2	-2065.0	Analog ground 0.				
54	AVDD_0	1346.8	-2065.0	Analog power supply 0.				
55	PD0	1442.7	-2065.0	ADC0_CH0 DAC0_OUT0ALT T #4/ OPAMP_OUT0 ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
56	PD1	1559.2	-2065.0	ADC0_CH1 DAC0_OUT1ALT T #4/ OPAMP_OUT1 ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
57	PD2	1646.3	-2065.0	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
58	PD3	1749.3	-2065.0	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
59	PD4	1851.4	-2065.0	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
60	PD5	2065.0	-1872.9	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
61	PD6	2065.0	-1771.3	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LETIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
62	PD7	2065.0	-1669.4	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LETIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
63	PD8	2065.0	-1561.9	BU_VIN				CMU_CLK1 #1
64	PC6	2065.0	-1470.2	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
65	PC7	2065.0	-1385.2	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
66	VSS_DREG	2065.0	-1295.5	Ground for on-chip voltage regulator.				

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
24	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
25	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
26	PA7	LCD_SEG35	EBI_CSTFT #0/1/2			
27	PA8	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
28	PA9	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
29	PA10	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
30	PA11	LCD_SEG39	EBI_HSNC #0/1/2			
31	IOVDD_2	Digital IO power supply 2.				
32	VSS	Ground.				
33	PA12	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
34	PA13	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
35	PA14	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
36	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
37	PB9		EBI_A03 #0/1/2		U1_TX #2	
38	PB10		EBI_A04 #0/1/2		U1_RX #2	
39	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
40	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
41	AVDD_1	Analog power supply 1.				
42	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
43	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
44	IOVDD_3	Digital IO power supply 3.				
45	AVDD_0	Analog power supply 0.				
46	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
47	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
48	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
49	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
J3	PD15				I2C0_SCL #3	
J4	PA12	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
J5	PA9	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
J6	PA10	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
J7	PB9		EBI_A03 #0/1/2		U1_TX #2	
J8	PB10		EBI_A04 #0/1/2		U1_RX #2	
J9	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
J10	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
J11	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
K1	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
K2	PC4	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LE- TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
K3	PA13	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
K4	VSS	Ground.				
K5	PA11	LCD_SEG39	EBI_HSNC #0/1/2			
K6	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
K7	AVSS_1	Analog ground 1.				
K8	AVDD_2	Analog power supply 2.				
K9	AVDD_1	Analog power supply 1.				
K10	AVSS_0	Analog ground 0.				
K11	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
L1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
L2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
L3	PA14	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
L6	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
L7	AVSS_2	Analog ground 2.				

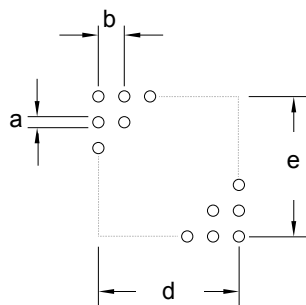


Figure 6.4. BGA112 PCB Stencil Design

Table 6.3. BGA112 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.33
b	0.80
d	8.00
e	8.00

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

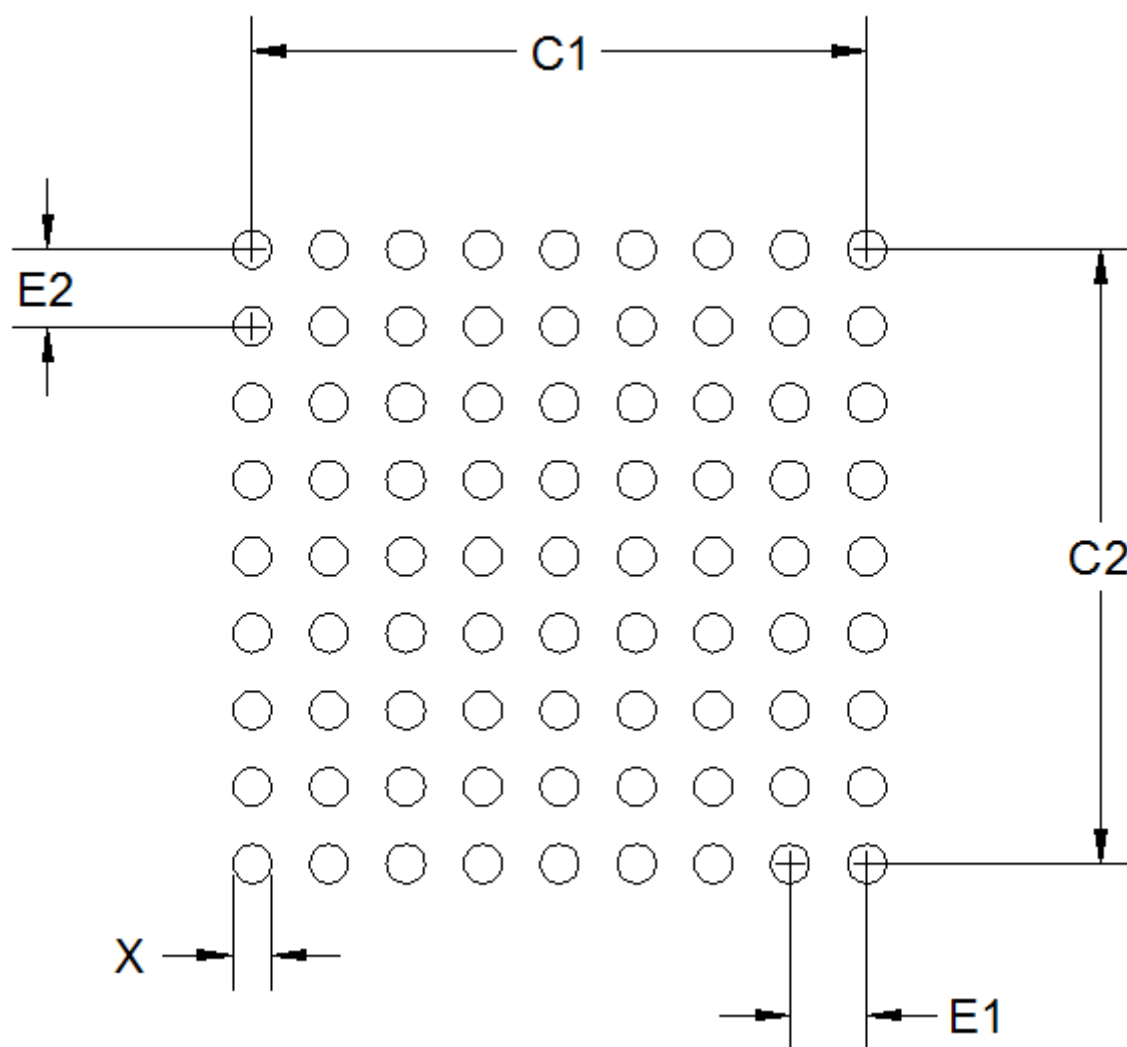


Figure 8.3. CSP81 PCB Solder Mask

Table 8.3. CSP81 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
X	0.26
C1	3.20
C2	3.20
E1	0.40
E2	0.40

		SYMBOL	MIN	NOM	MAX
lead thickness		c1	0.09	—	0.16
	x	D	16 BSC		
	y	E	16 BSC		
body size	x	D1	14 BSC		
	y	E1	14 BSC		
lead pitch		e	0.5 BSC		
		L	0.45	0.6	0.75
footprint		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	—	—
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	—	—
		R1	0.08	—	0.2
		S	0.2	—	—
package edge tolerance		aaa	0.2		
lead edge tolerance		bbb	0.2		
coplanarity		ccc	0.08		
lead offset		ddd	0.08		
mold flatness		eee	0.05		

The LQFP100 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>

Table 11.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.97	e	8.90
b	0.42	f	7.32
c	0.50	g	7.32
d	8.90	-	-

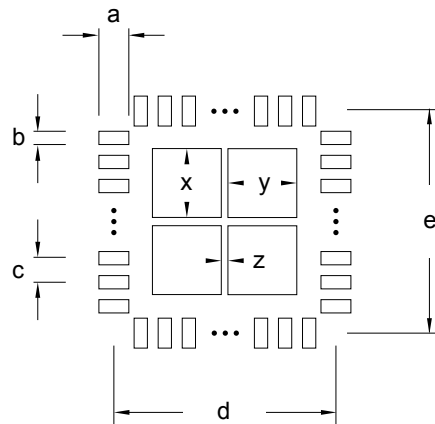


Figure 11.4. QFN64 PCB Stencil Design

Table 11.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

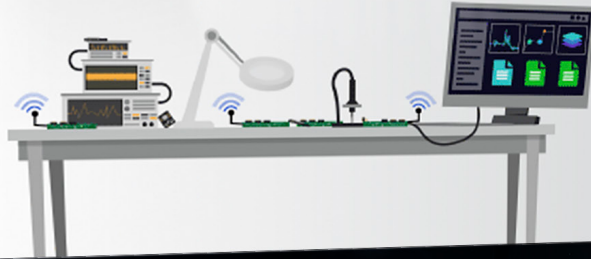
Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.75	e	8.90
b	0.22	x	2.70
c	0.50	y	2.70
d	8.90	z	0.80

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

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