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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	86
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg880f64-qfp100

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3.2.3 EFM32LG280

The features of the EFM32LG280 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.3. EFM32LG280 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNCR, EBI_NANDREN, EBI_NANDWEN, EBI_REn, EBI_VSNCR, EBI_WEn
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

Module	Configuration	Pin Connections
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	50 pins	Available pins are shown in 5.7.3 GPIO Pinout Overview

4.4.3 EM3 Current Consumption

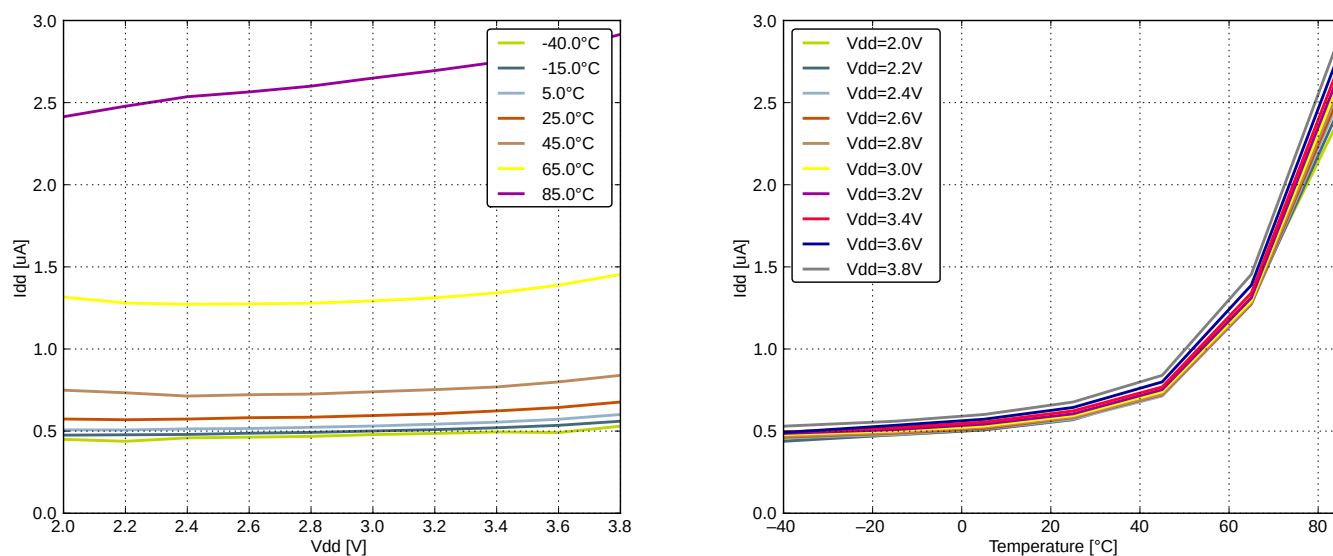


Figure 4.8. EM3 Current Consumption

4.4.4 EM4 Current Consumption

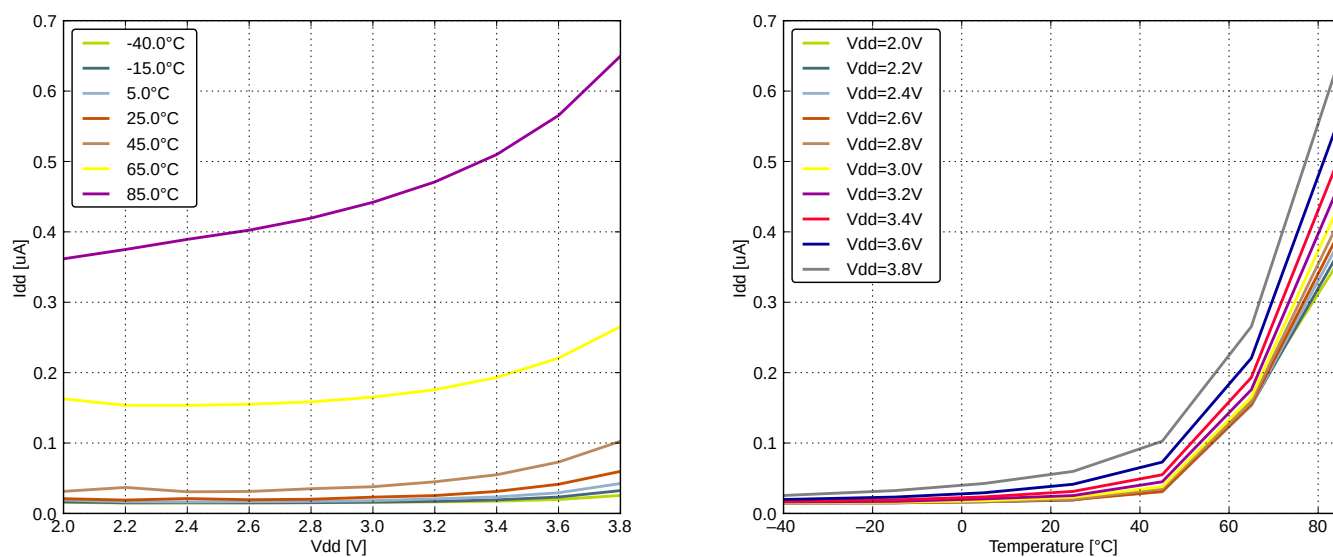


Figure 4.9. EM4 Current Consumption

4.8 General Purpose Input Output

Table 4.7. GPIO

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Input low voltage	V_{IOIL}		—	—	$0.30 \times V_{DD}$	V
Input high voltage	V_{IOIH}		$0.70 \times V_{DD}$	—	—	V
Output high voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	V_{IOOH}	Sourcing 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST	—	$0.80 \times V_{DD}$	—	V
		Sourcing 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST	—	$0.90 \times V_{DD}$	—	V
		Sourcing 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.85 \times V_{DD}$	—	V
		Sourcing 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.90 \times V_{DD}$	—	V
		Sourcing 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.75 \times V_{DD}$	—	—	V
		Sourcing 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD	$0.85 \times V_{DD}$	—	—	V
		Sourcing 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.60 \times V_{DD}$	—	—	V
		Sourcing 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	$0.80 \times V_{DD}$	—	—	V
Output low voltage (Production test condition = 3.0V, DRIVEMODE = STANDARD)	V_{IOOL}	Sinking 0.1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST	—	$0.20 \times V_{DD}$	—	V
		Sinking 0.1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW-EST	—	$0.10 \times V_{DD}$	—	V
		Sinking 1 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.10 \times V_{DD}$	—	V
		Sinking 1 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = LOW	—	$0.05 \times V_{DD}$	—	V
		Sinking 6 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	$0.30 \times V_{DD}$	V
		Sinking 6 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = STANDARD	—	—	$0.20 \times V_{DD}$	V
		Sinking 20 mA, $V_{DD}=1.98$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	$0.35 \times V_{DD}$	V
		Sinking 20 mA, $V_{DD}=3.0$ V, GPIO_Px_CTRL DRIVEMODE = HIGH	—	—	$0.25 \times V_{DD}$	V

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range(SFDR)	SFDR _{DAC}	500 kSamples/s, 12 bit, single ended, internal 1.25V reference	—	62	—	dBc
		500 kSamples/s, 12 bit, single ended, internal 2.5V reference	—	56	—	dBc
		500 kSamples/s, 12 bit, differential, internal 1.25V reference	—	61	—	dBc
		500 kSamples/s, 12 bit, differential, internal 2.5V reference	—	55	—	dBc
		500 kSamples/s, 12 bit, differential, V _{DD} reference	—	60	—	dBc
Offset voltage, all packages except CSP	V _{DACOFF-SET}	After calibration, single ended	—	2	9	mV
		After calibration, differential	—	2	—	mV
Offset voltage, CSP devices	V _{DACOFF-SET}	After calibration, single ended	—	2	—	mV
		After calibration, differential	—	2	—	mV
Differential non-linearity	DNL _{DAC}		—	±1	—	LSB
Integral non-linearity	INL _{DAC}		—	±5	—	LSB
No missing codes	MC _{DAC}		—	12	—	bits
VREF output voltage	V _{REF}	1.25 V reference	1.2	1.25	1.3	V
		2.5 V reference	2.4	2.5	2.6	V
VREF voltage drift	V _{REF_VDRIFT}	1.25 V reference	-12.4	2.3	18.2	mV/V
		2.5 V reference, VDD > 2.5 V	-24.6	5.3	35.2	mV/V
VREF temperature drift	V _{REF_TDRIFT}	1.25 V reference	-132	242	677	μV/°C
		2.5 V reference	-231	507	1271	μV/°C
VREF current consumption	I _{VREF}	1.25 V reference	—	67	97	μA
		2.5 V reference	—	55	72	μA
ADC and DAC VREF matching	V _{REF_MATCH}	1.25 V reference	—	99.85	—	%
		2.5 V reference	—	100.01	—	%

Note:

1. Measured with a static input code and no loading on the output. Includes required contribution from the voltage reference.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
F11	PE7		EBI_A14 #0/1/2		US0_TX #1	
F12	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
F13	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
G1	PB3		EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
G2	PB4		EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
G3	IOVDD_2	Digital IO power supply 2.				
G11	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
G12	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
G13	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
H1	PB5		EBI_A21 #0/1/2		US2_CLK #1	
H2	PB6		EBI_A22 #0/1/2		US2_CS #1	
H3	VSS	Ground.				
H11	VDD_DREG	Power supply for on-chip voltage regulator.				
H12	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
H13	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
J1	PD14				I2C0_SDA #3	
J2	PD15				I2C0_SCL #3	
J3	VSS	Ground.				
J11	IOVDD_3	Digital IO power supply 3.				
J12	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
J13	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
K1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
K2	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
K3	IOVDD_4	Digital IO power supply 4.				
K11	VSS	Ground.				
K12	VSS	Ground.				
K13	PD8	BU_VIN				CMU_CLK1 #1

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.
EBI_WEn	PF4	PF8	PF4					External Bus Interface (EBI) Write Enable output.
ETM_TCLK	PD7	PF8	PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6	PF9	PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3	PD13	PD3	PA3				Embedded Trace Module ETM data 1.

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
25	PB14	HFXTAL_N		US0_CS #4/5 LEU0_RX #1	
26	IOVDD_3	Digital IO power supply 3.			
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
30	PD2	ADC0_CH2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
31	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 OPAMP_P1	TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 OPAMP_N1	TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
44	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0
45	USB_VREGI				
46	USB_VREGO				
47	PF10			USB_DM	
48	PF11			USB_DP	
49	PF0		TIM0_CC0 #5 LE- TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3

5.7.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG332 is shown in the following figure.

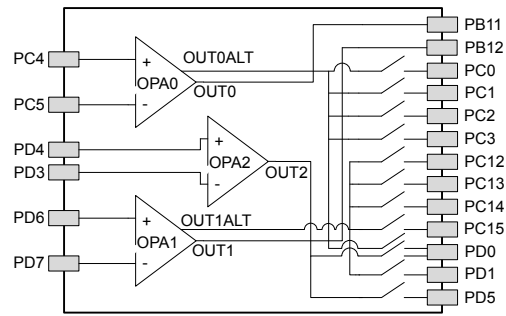


Figure 5.14. Opamp Pinout

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
M11	AVSS_0	Analog ground 0.				
M12	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
M13	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
N1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
N2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
N3	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		
N4	PA11		EBI_HSNC #0/1/2			
N5	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
N6	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
N7	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
N8	AVSS_2	Analog ground 2.				
N9	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
N10	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
N11	AVDD_0	Analog power supply 0.				
N12	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
N13	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
92	PC14	2065.0	1558.7	ACMP1_CH6 DAC0_OUT1AL T #2/ OPAMP_OUT1 ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
93	PF10	2065.0	1673.6				U1_TX #1 USB_DM	
94	PC15	2065.0	1756.6	ACMP1_CH7 DAC0_OUT1AL T #3/ OPAMP_OUT1 ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
95	PF11	2065.0	1870.0				U1_RX #1 USB_DP	
96	IOVSS_7	1846.0	2065.0	Digital IO ground 7.				
97	PF0	1739.3	2065.0			TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
98	PF1	1626.3	2065.0			TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU 3
99	PF2	1513.2	2065.0	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU 4
100	PF3	1389.7	2065.0	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
101	USB_VBUS	1242.9	2065.0	USB 5.0 V VBUS input.				
102	PF4	995.9	2065.0	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
103	PF12	886.3	2065.0				USB_ID	
104	PF5	782.2	2065.0	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
105	IOVSS_5	672.3	2065.0	Digital IO ground 5.				
106	IOVDD_5	576.7	2065.0	Digital IO power supply 5.				
107	PF6	488.4	2065.0	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
108	PF7	380.5	2065.0	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
109	PF8	275.3	2065.0	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
110	PF9	174.3	2065.0	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
111	NC	43.2	2065.0	Do not connect.				
112	PD9	-89.5	2065.0	LCD_SEG28	EBI_CS0 #0/1/2			
113	PD10	-204.5	2065.0	LCD_SEG29	EBI_CS1 #0/1/2			

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
52	USB_VBUS	USB 5.0 V VBUS input.			
53	PF12			USB_ID	
54	PF5	LCD_SEG3	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
55	IOVDD_5	Digital IO power supply 5.			
56	PE8	LCD_SEG4	PCNT2_S0IN #1		PRS_CH3 #1
57	PE9	LCD_SEG5	PCNT2_S1IN #1		
58	PE10	LCD_SEG6	TIM1_CC0 #1	US0_TX #0	BOOT_TX
59	PE11	LCD_SEG7	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
60	PE12	LCD_SEG8	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
61	PE13	LCD_SEG9		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
62	PE14	LCD_SEG10	TIM3_CC0 #0	LEU0_TX #2	
63	PE15	LCD_SEG11	TIM3_CC1 #0	LEU0_RX #2	
64	PA15	LCD_SEG12	TIM3_CC2 #0		

5.20 EFM32LG980 (LQFP100)

5.20.1 Pinout

The EFM32LG980 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

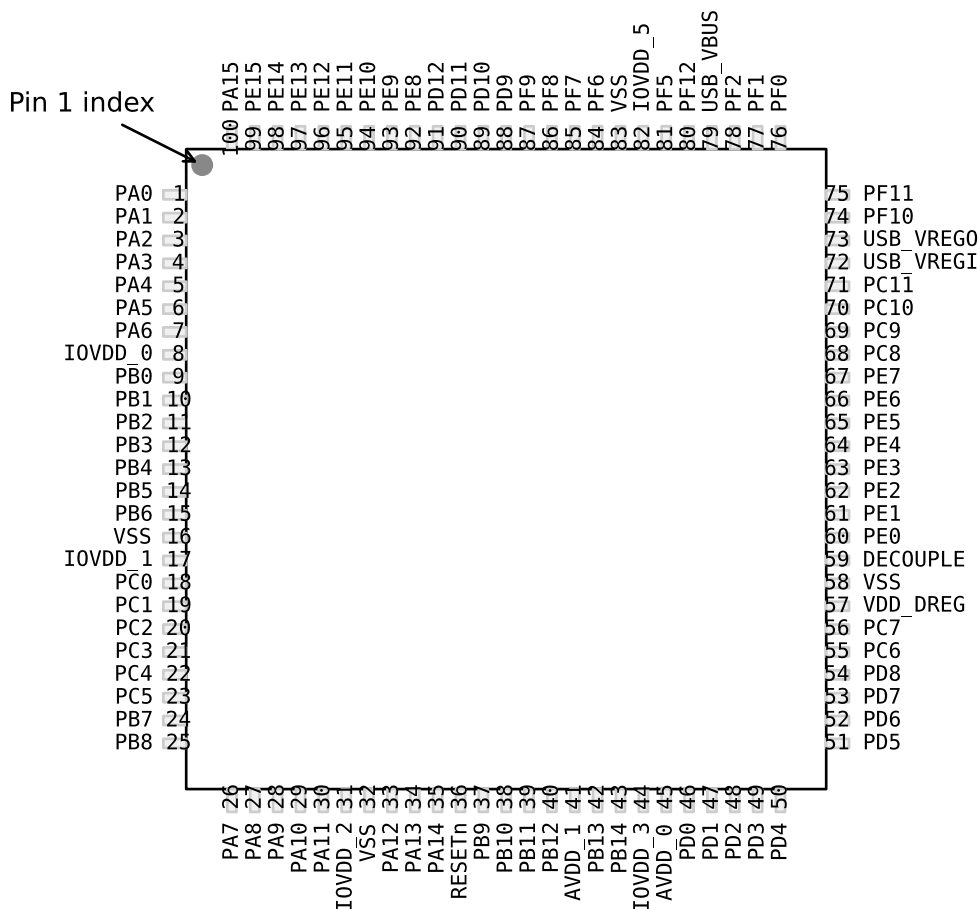


Figure 5.39. EFM32LG980 Pinout (top view, not to scale)

Table 5.58. Device Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
1	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A3	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
A4	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
A5	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
A6	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
A7	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
A8	PF12				USB_ID	
A9	PE4	LCD_COM0	EBI_A11 #0/1/2		US0_CS #1	
A10	PF10				U1_TX #1 USB_DM	
A11	PF11				U1_RX #1 USB_DP	
B1	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		
B2	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B3	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
B4	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
B5	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
B6	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
B7	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
B8	USB_VBUS	USB 5.0 V VBUS input.				
B9	PE5	LCD_COM1	EBI_A12 #0/1/2		US0_CLK #1	
B10	USB_VREGI					
B11	USB_VREGO					
C1	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C2	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
C3	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					ETM_TD1 #1
C5	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
C6	PF9	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
C7	VSS	Ground.				
C8	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
C9	PE6	LCD_COM2	EBI_A13 #0/1/2		US0_RX #1	
C10	PC10	ACMP1_CH2	EBI_A10 #1/2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0

8.2 CSP81 PCB Layout

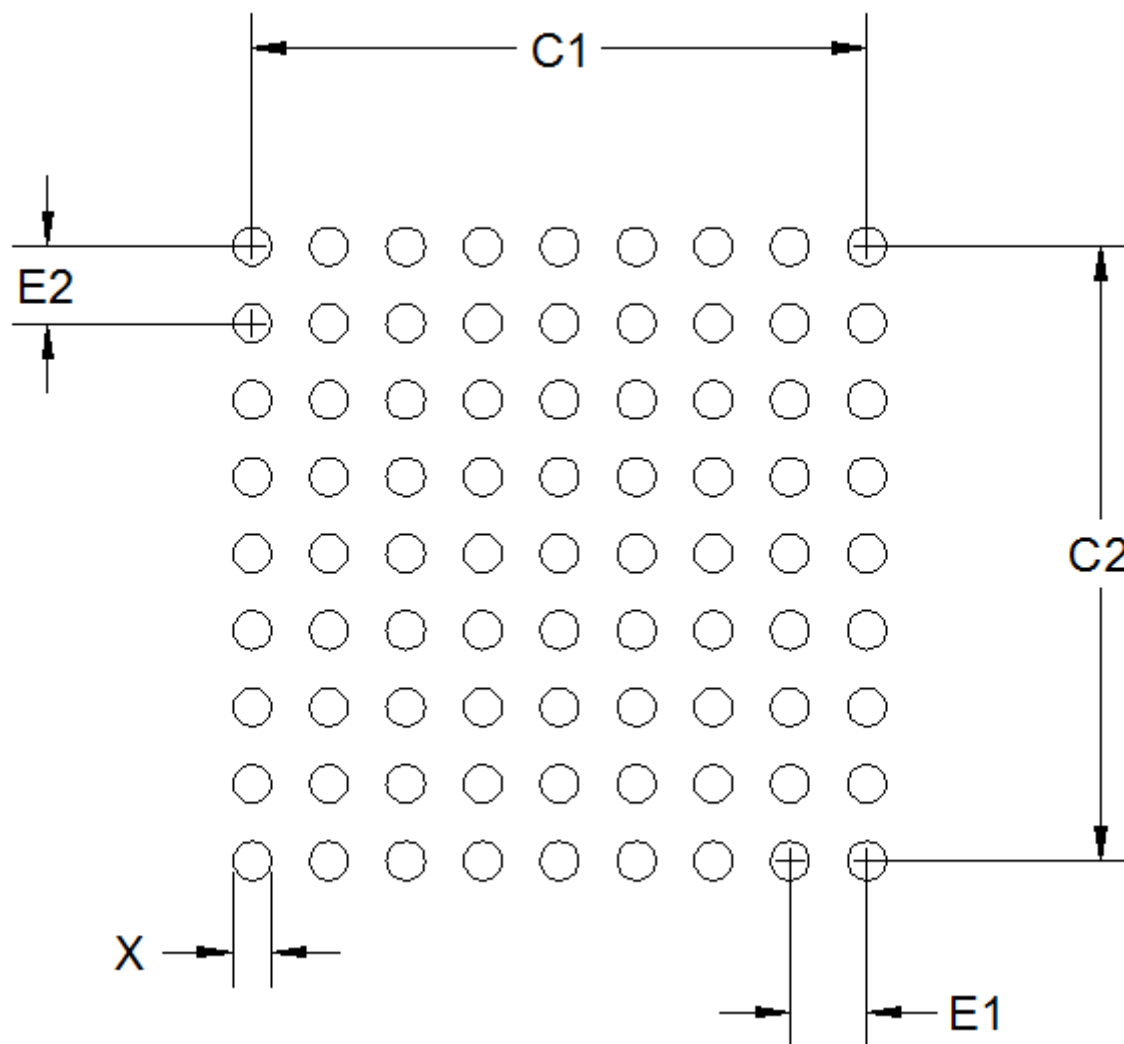


Figure 8.2. CSP81 PCB Land Pattern

Table 8.2. CSP81 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
X	0.20
C1	3.20
C2	3.20
E1	0.40
E2	0.40

14. Revision History

14.1 Revision 2.00

April 17th, 2017

Consolidated all EFM32LG data sheets:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG360
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG900
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Added a Feature List section.

[2. Ordering Information](#) – Added ordering code decoder.

[3.3 Memory Map](#) – Separated the Memory Map into two figures – one for core and code space listing and one for peripheral listing.

[4.2 Absolute Maximum Ratings](#) – Removed the footnote about storage temperature and added max source/sink current per I/O pin.

Environmental – Removed this section. Environmental specifications are available in the qualification report.

[4.4 Current Consumption](#) - Added maximum current specifications for the highest energy mode, I_{EM0} .

[4.8 General Purpose Input Output](#) – Reduced maximum input leakage current ($I_{IOLEAK, max}$).

[4.9.1 LFXO](#) – Replaced “energyAware Designer” with “Configurator tool”.

[4.9.3 LFRCO](#) – Added (min, typ, max) specifications for oscillation frequency over full power supply and full temperature range. Also added typical voltage drift and temperature drift specs.

[4.9.3 LFRCO](#) – Updated graphs for calibrated LFRCO Frequency vs. Temperature and Supply Range, and also fixed y-axis unit [kHz].

[4.9.4 HFRCO](#) – Added specifications for oscillation frequency over full power supply and temperature range, added typical voltage drift and temperature drift specs at each frequency band, and removed the duty cycle spec (DC_{HFRCO}).

[4.9.4 HFRCO](#) – Updated all HFRCO graphs (various frequency bands).

[4.9.6 ULFRCO](#) – Removed the duty cycle spec for AUXHFRCO ($DC_{AUXHFRCO}$).

[4.10 Analog Digital Converter \(ADC\)](#) – Added the following specs:

- Input bias current ($I_{ADCBiasIN}$) – added max (source and sink).
- Input offset current ($I_{ADCOFFSETIN}$) – added max (source and sink).
- VREF output voltage (V_{REF}) – added min, typ, max.

14.4 Revision 1.21

November 21st, 2013

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

Updated figures.

Updated errata-link.

Updated chip marking.

Added link to Environmental and Quality information.

For devices with a DAC, re-added missing DAC-data.