# Silicon Labs - EFM32LG890F256-BGA112 Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | ARM® Cortex®-M3 |
| Core Size | 32-Bit Single-Core |
| Speed | 48MHz |
| Connectivity | EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT |
| Number of I/O | 90 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.98V ~ 3.8V |
| Data Converters | A/D 8x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 112-LFBGA |
| Supplier Device Package | 112-BGA (10x10) |
| Purchase URL | https://www.e-xfl.com/product-detail/silicon-labs/efm32lg890f256-bga112 |

# 3. System Summary

## 3.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M3, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32LG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32LG devices. For a complete feature set and in-depth information on the modules, the reader is referred to the EFM32LG Reference Manual.

A block diagram of the EFM32LG is shown in the following figure.

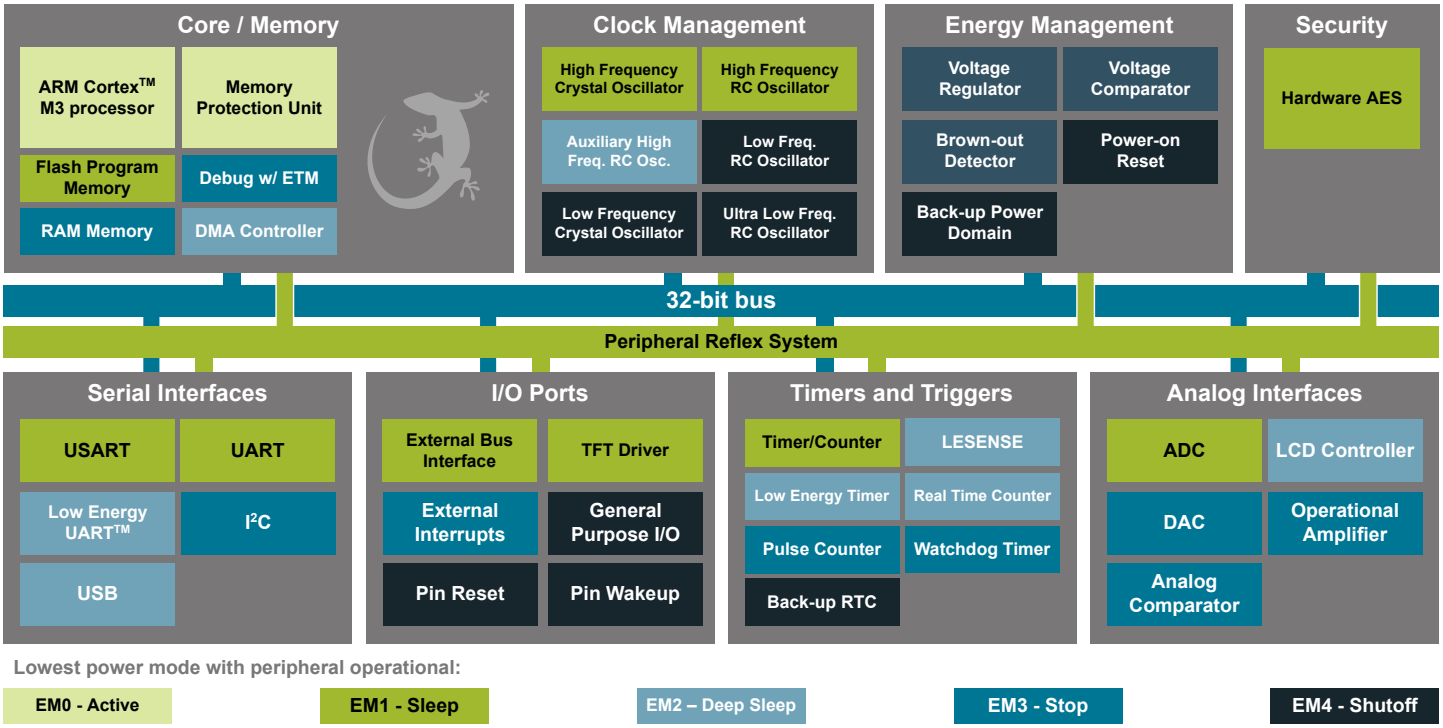


**Figure 3.1. Block Diagram**

### 3.1.1 ARM Cortex-M3 Core

The ARM Cortex-M3 includes a 32-bit RISC processor which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M3 is described in detail in EFM32LG Reference Manual.

### 3.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing . In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

### 3.1.3 Memory System Controller (MSC)

The Memory System Controller (MSC) is the program memory unit of the EFM32LG microcontroller. The flash memory is readable and writable from both the Cortex-M3 and DMA. The flash memory is divided into two blocks; the main block and the information block. Program code is normally written to the main block. Additionally, the information block is available for special user data and flash lock bits. There is also a read-only page in the information block containing system and device calibration data. Read and write operations are supported in the energy modes EM0 and EM1.

### 3.2.22 EFM32LG995

The features of the EFM32LG995 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

**Table 3.22. EFM32LG995 Configuration Summary**

| Module | Configuration | Pin Connections |
|---|---|---|
| Cortex-M3 | Full configuration | NA |
| DBG | Full configuration | DBG_SWCLK, DBG_SWDIO, DBG_SWO |
| MSC | Full configuration | NA |
| DMA | Full configuration | NA |
| RMU | Full configuration | NA |
| EMU | Full configuration | NA |
| CMU | Full configuration | CMU_OUT0, CMU_OUT1 |
| WDOG | Full configuration | NA |
| PRS | Full configuration | NA |
| USB | Full configuration | USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID |
| EBI | Full configuration | EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNC, EBI_NANDREn, EBI_NANDWEn, EBI_REn, EBI_VSNC, EBI_WEn |
| I2C0 | Full configuration | I2C0_SDA, I2C0_SCL |
| I2C1 | Full configuration | I2C1_SDA, I2C1_SCL |
| USART0 | Full configuration with IrDA | US0_TX, US0_RX. US0_CLK, US0_CS |
| USART1 | Full configuration with I2S | US1_TX, US1_RX, US1_CLK, US1_CS |
| USART2 | Full configuration with I2S | US2_TX, US2_RX, US2_CLK, US2_CS |
| UART0 | Full configuration | U0_TX, U0_RX |
| UART1 | Full configuration | U1_TX, U1_RX |
| LEUART0 | Full configuration | LEU0_TX, LEU0_RX |
| LEUART1 | Full configuration | LEU1_TX, LEU1_RX |
| TIMER0 | Full configuration with DTI | TIM0_CC[2:0], TIM0_CDTI[2:0] |
| TIMER1 | Full configuration | TIM1_CC[2:0] |
| TIMER2 | Full configuration | TIM2_CC[2:0] |
| TIMER3 | Full configuration | TIM3_CC[2:0] |
| RTC | Full configuration | NA |
| BURTC | Full configuration | NA |
| LETIMER0 | Full configuration | LET0_O[1:0] |
| PCNT0 | Full configuration, 16-bit count register | PCNT0_S[1:0] |
| PCNT1 | Full configuration, 8-bit count register | PCNT1_S[1:0] |
| PCNT2 | Full configuration, 8-bit count register | PCNT2_S[1:0] |
| ACMP0 | Full configuration | ACMP0_CH[7:0], ACMP0_O |

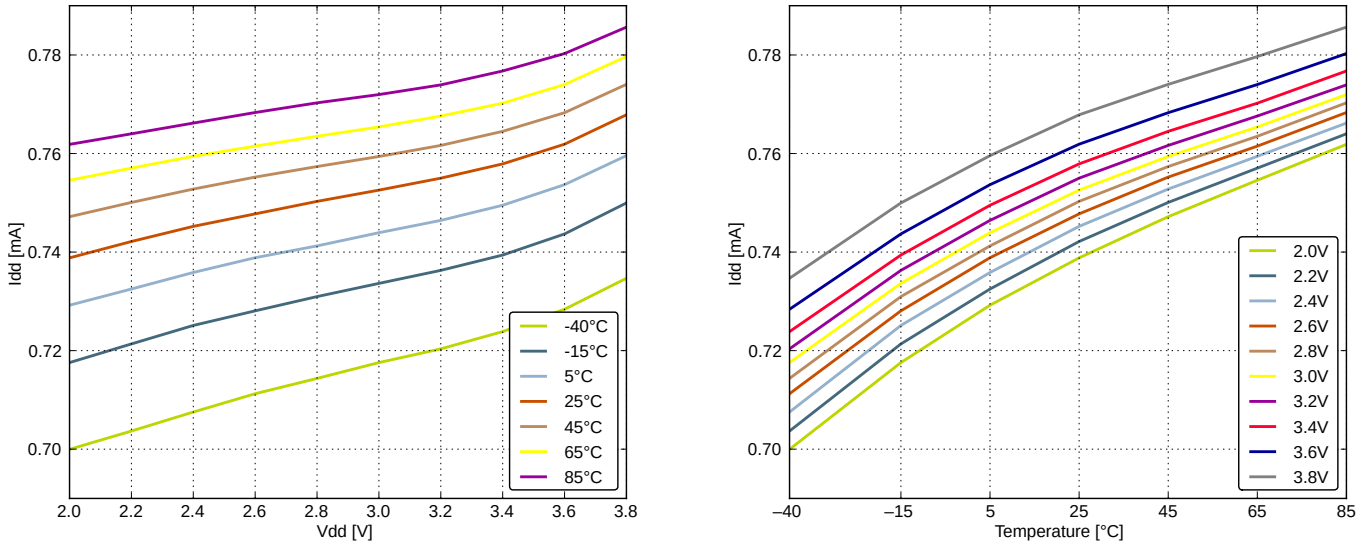


**Figure 4.5. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 11 MHz**

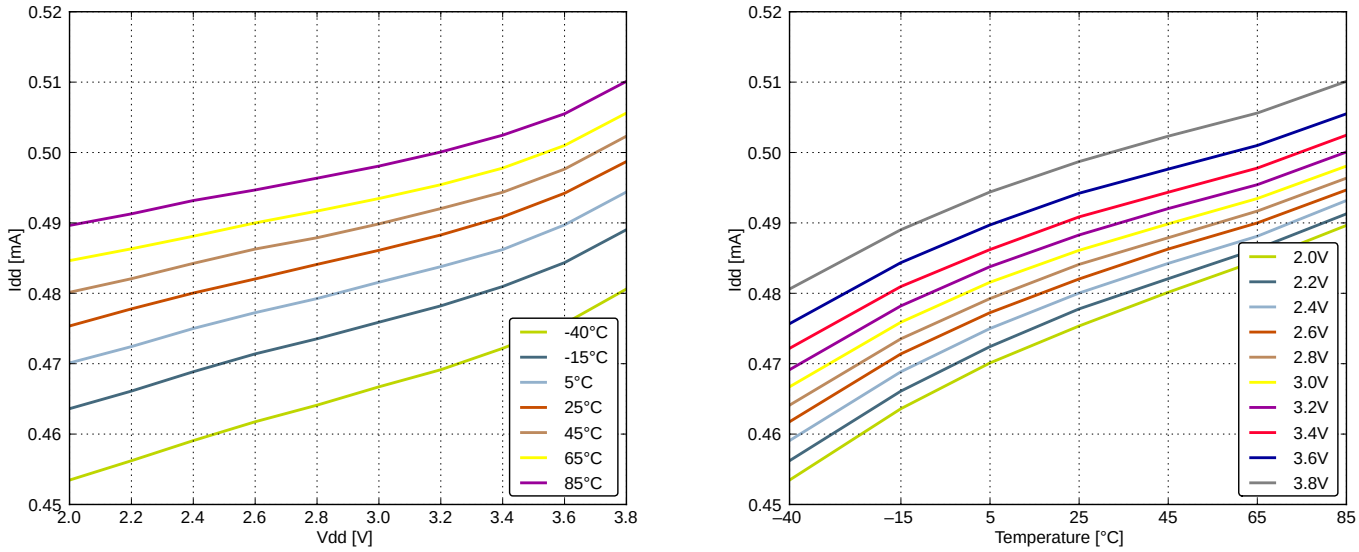


**Figure 4.6. EM1 Current Consumption with all Peripheral Clocks Disabled and HFRCO Running at 6.6 MHz**

**Table 5.1. Device Pinout**

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |
| 3 | PA2 | | TIM0_CC2 #0/1 | | CMU_CLK0 #0 ETM_TD0 #3 |
| 4 | PA3 | | TIM0_CDTI0 #0 | | LES_ALTEX2 #0 ETM_TD1 #3 |
| 5 | PA4 | | TIM0_CDTI1 #0 | | LES_ALTEX3 #0 ETM_TD2 #3 |
| 6 | PA5 | | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0 ETM_TD3 #3 |
| 7 | PA6 | | | LEU1_RX #1 | ETM_TCLK #3 GPIO_EM4WU1 |
| 8 | VSS | Ground. | | | |
| 9 | PC0 | ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT | TIM0_CC1 #4 PCNT0_S0IN #2 | US0_TX #5 US1_TX #0 I2C0_SDA #4 | LES_CH0 #0 PRS_CH2 #0 |
| 10 | PC1 | ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT | TIM0_CC2 #4 PCNT0_S1IN #2 | US0_RX #5 US1_RX #0 I2C0_SCL #4 | LES_CH1 #0 PRS_CH3 #0 |
| 11 | PC2 | ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 12 | PC3 | ACMP0_CH3DAC0_OUT0ALT #3/ OPAMP_OUT0ALT | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 13 | PC4 | ACMP0_CH4 OPAMP_P0 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0 | US2_CLK #0 I2C1_SDA #0 | LES_CH4 #0 |
| 14 | PC5 | ACMP0_CH5 OPAMP_N0 | LETIM0_OUT1 #3 PCNT1_S1IN #0 | US2_CS #0 I2C1_SCL #0 | LES_CH5 #0 |
| 15 | PB7 | LFXTAL_P | TIM1_CC0 #3 | US0_TX #4 US1_CLK #0 | |
| 16 | PB8 | LFXTAL_N | TIM1_CC1 #3 | US0_RX #4 US1_CS #0 | |
| 17 | PA8 | | TIM2_CC0 #0 | | |
| 18 | PA9 | | TIM2_CC1 #0 | | |
| 19 | PA10 | | TIM2_CC2 #0 | | |
| 20 | RESETn | Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released. | | | |
| 21 | PB11 | DAC0_OUT0 / OPAMP_OUT0 | TIM1_CC2 #3 LE-TIM0_OUT0 #1 | I2C1_SDA #1 | |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.3.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG280 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.9. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | PA11 | PA10 | PA9 | PA8 | PA7 | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | PB10 | PB9 | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | PB2 | PB1 | PB0 |
| Port C | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | PD12 | PD11 | PD10 | PD9 | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | PE3 | PE2 | PE1 | PE0 |
| Port F | — | — | — | — | — | — | PF9 | PF8 | PF7 | PF6 | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.3.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG280 is shown in the following figure.

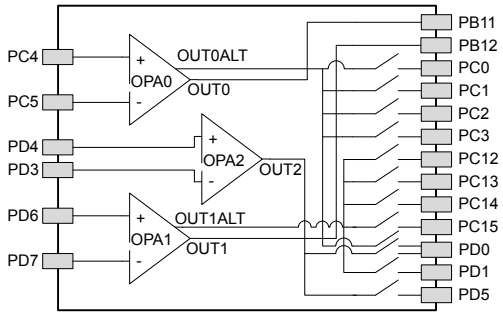


**Figure 5.6. Opamp Pinout**

| BGA112 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| C5 | PD12 | | EBI_CS3 #0/1/2 | | | |
| C6 | PF9 | | EBI_REn #1 | | | ETM_TD0 #1 |
| C7 | VSS | Ground. | | | | |
| C8 | PF2 | | EBI_ARDY #0/1/2 | TIM0_CC2 #5 | LEU0_TX #4 | ACMP1_O #0<br>DBG_SWO #0<br>GPIO_EM4WU4 |
| C9 | PE6 | | EBI_A13 #0/1/2 | | US0_RX #1 | |
| C10 | PC10 | ACMP1_CH2 | EBI_A10 #1/2 | TIM2_CC2 #2 | US0_RX #2 | LES_CH10 #0 |
| C11 | PC11 | ACMP1_CH3 | EBI_ALE #1/2 | | US0_TX #2 | LES_CH11 #0 |
| D1 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| D2 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| D3 | PB15 | | | | | ETM_TD2 #1 |
| D4 | VSS | Ground. | | | | |
| D5 | IOVDD_6 | Digital IO power supply 6. | | | | |
| D6 | PD9 | | EBI_CS0 #0/1/2 | | | |
| D7 | IOVDD_5 | Digital IO power supply 5. | | | | |
| D8 | PF1 | | | TIM0_CC1 #5 LE-TIM0_OUT1 #2 | US1_CS #2<br>LEU0_RX #3<br>I2C0_SCL #5 | DBG_SWDIO #0/1/2/3<br>GPIO_EM4WU3 |
| D9 | PE7 | | EBI_A14 #0/1/2 | | US0_TX #1 | |
| D10 | PC8 | ACMP1_CH0 | EBI_A15 #0/1/2 | TIM2_CC0 #2 | US0_CS #2 | LES_CH8 #0 |
| D11 | PC9 | ACMP1_CH1 | EBI_A09 #1/2 | TIM2_CC1 #2 | US0_CLK #2 | LES_CH9 #0<br>GPIO_EM4WU2 |
| E1 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| E2 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| E3 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| E4 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| E8 | PF0 | | | TIM0_CC0 #5 LE-TIM0_OUT0 #2 | US1_CLK #2<br>LEU0_TX #3<br>I2C0_SDA #5 | DBG_SWCLK #0/1/2/3 |
| E9 | PE0 | | EBI_A07 #0/1/2 | TIM3_CC0 #1<br>PCNT0_S0IN #1 | U0_TX #1<br>I2C1_SDA #2 | |
| E10 | PE1 | | EBI_A08 #0/1/2 | TIM3_CC1 #1<br>PCNT0_S1IN #1 | U0_RX #1<br>I2C1_SCL #2 | |
| E11 | PE3 | BU_STAT | EBI_A10 #0 | | U1_RX #3 | ACMP1_O #1 |
| F1 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |
| US2_CS | PC5 | PB6 | | | | | | USART2 chip select input / output. |
| US2_RX | PC3 | PB4 | | | | | | USART2 Asynchronous Receive.<br>USART2 Synchronous mode Master Input / Slave Output (MISO). |
| US2_TX | PC2 | PB3 | | | | | | USART2 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART2 Synchronous mode Master Output / Slave Input (MOSI). |

### 5.6.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG330 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.18. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | — | — | — | — | PA10 | PA9 | PA8 | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | — | — | PB8 | PB7 | — | — | — | — | — | — | — |
| Port C | — | — | — | — | PC11 | PC10 | PC9 | PC8 | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | — | — | — | — | — | — | — | — |
| Port F | — | — | — | PF12 | PF11 | PF10 | — | — | — | — | PF5 | — | — | PF2 | PF1 | PF0 |

### 5.6.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG330 is shown in the following figure.

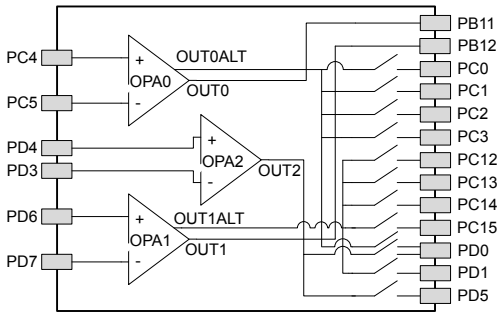


**Figure 5.12. Opamp Pinout**

### 5.7 EFM32LG332 (TQFP64)

#### 5.7.1 Pinout

The EFM32LG332 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

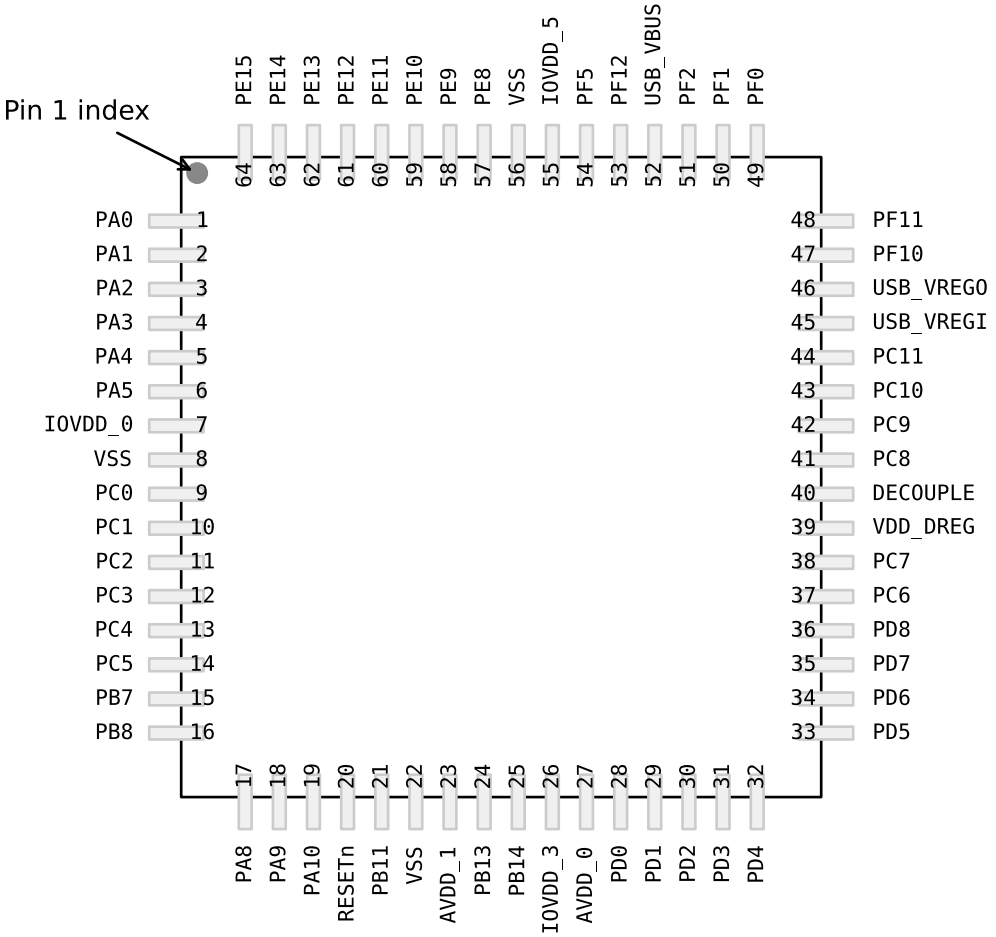


**Figure 5.13. EFM32LG332 Pinout (top view, not to scale)**

**Table 5.19. Device Pinout**

| QFP64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 1 | PA0 | | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |
| 2 | PA1 | | TIM0_CC1 #0/1 | I2C0_SCL #0 | CMU_CLK1 #0 PRS_CH1 #0 |

| LQFP100 Pin# and Name | | Pin Alternate Functionality / Description | | | | |
|---|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | EBI | Timers | Communication | Other |
| 3 | PA2 | | EBI_AD11 #0/1/2 | TIM0_CC2 #0/1 | | CMU_CLK0 #0<br>ETM_TD0 #3 |
| 4 | PA3 | | EBI_AD12 #0/1/2 | TIM0_CDTI0 #0 | U0_TX #2 | LES_ALTEX2 #0<br>ETM_TD1 #3 |
| 5 | PA4 | | EBI_AD13 #0/1/2 | TIM0_CDTI1 #0 | U0_RX #2 | LES_ALTEX3 #0<br>ETM_TD2 #3 |
| 6 | PA5 | | EBI_AD14 #0/1/2 | TIM0_CDTI2 #0 | LEU1_TX #1 | LES_ALTEX4 #0<br>ETM_TD3 #3 |
| 7 | PA6 | | EBI_AD15 #0/1/2 | | LEU1_RX #1 | ETM_TCLK #3<br>GPIO_EM4WU1 |
| 8 | IOVDD_0 | Digital IO power supply 0. | | | | |
| 9 | PB0 | | EBI_A16 #0/1/2 | TIM1_CC0 #2 | | |
| 10 | PB1 | | EBI_A17 #0/1/2 | TIM1_CC1 #2 | | |
| 11 | PB2 | | EBI_A18 #0/1/2 | TIM1_CC2 #2 | | |
| 12 | PB3 | | EBI_A19 #0/1/2 | PCNT1_S0IN #1 | US2_TX #1 | |
| 13 | PB4 | | EBI_A20 #0/1/2 | PCNT1_S1IN #1 | US2_RX #1 | |
| 14 | PB5 | | EBI_A21 #0/1/2 | | US2_CLK #1 | |
| 15 | PB6 | | EBI_A22 #0/1/2 | | US2_CS #1 | |
| 16 | VSS | Ground. | | | | |
| 17 | IOVDD_1 | Digital IO power supply 1. | | | | |
| 18 | PC0 | ACMP0_CH0<br>DAC0_OUT0ALT #0/<br>OPAMP_OUT0ALT | EBI_A23 #0/1/2 | TIM0_CC1 #4<br>PCNT0_S0IN #2 | US0_TX #5<br>US1_TX #0<br>I2C0_SDA #4 | LES_CH0 #0<br>PRS_CH2 #0 |
| 19 | PC1 | ACMP0_CH1<br>DAC0_OUT0ALT #1/<br>OPAMP_OUT0ALT | EBI_A24 #0/1/2 | TIM0_CC2 #4<br>PCNT0_S1IN #2 | US0_RX #5<br>US1_RX #0<br>I2C0_SCL #4 | LES_CH1 #0<br>PRS_CH3 #0 |
| 20 | PC2 | ACMP0_CH2<br>DAC0_OUT0ALT #2/<br>OPAMP_OUT0ALT | EBI_A25 #0/1/2 | TIM0_CDTI0 #4 | US2_TX #0 | LES_CH2 #0 |
| 21 | PC3 | ACMP0_CH3<br>DAC0_OUT0ALT #3/<br>OPAMP_OUT0ALT | EBI_NANDREn #0/1/2 | TIM0_CDTI1 #4 | US2_RX #0 | LES_CH3 #0 |
| 22 | PC4 | ACMP0_CH4<br>OPAMP_P0 | EBI_A26 #0/1/2 | TIM0_CDTI2 #4 LE-TIM0_OUT0 #3<br>PCNT1_S0IN #0 | US2_CLK #0<br>I2C1_SDA #0 | LES_CH4 #0 |
| 23 | PC5 | ACMP0_CH5<br>OPAMP_N0 | EBI_NANDWEn #0/1/2 | LETIM0_OUT1 #3<br>PCNT1_S1IN #0 | US2_CS #0<br>I2C1_SCL #0 | LES_CH5 #0 |
| 24 | PB7 | LFXTAL_P | | TIM1_CC0 #3 | US0_TX #4<br>US1_CLK #0 | |
| 25 | PB8 | LFXTAL_N | | TIM1_CC1 #3 | US0_RX #4<br>US1_CS #0 | |

### 5.12.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG840 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

**Table 5.36. GPIO Pinout**

| Port | Pin 15 | Pin 14 | Pin 13 | Pin 12 | Pin 11 | Pin 10 | Pin 9 | Pin 8 | Pin 7 | Pin 6 | Pin 5 | Pin 4 | Pin 3 | Pin 2 | Pin 1 | Pin 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Port A | PA15 | PA14 | PA13 | PA12 | — | — | — | — | — | PA6 | PA5 | PA4 | PA3 | PA2 | PA1 | PA0 |
| Port B | — | PB14 | PB13 | PB12 | PB11 | — | — | PB8 | PB7 | PB6 | PB5 | PB4 | PB3 | — | — | — |
| Port C | PC15 | PC14 | PC13 | PC12 | — | — | — | — | PC7 | PC6 | PC5 | PC4 | — | — | — | — |
| Port D | — | — | — | — | — | — | — | PD8 | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Port E | PE15 | PE14 | PE13 | PE12 | PE11 | PE10 | PE9 | PE8 | PE7 | PE6 | PE5 | PE4 | — | — | — | — |
| Port F | — | — | — | — | — | — | — | — | — | — | PF5 | PF4 | PF3 | PF2 | PF1 | PF0 |

### 5.12.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG840 is shown in the following figure.

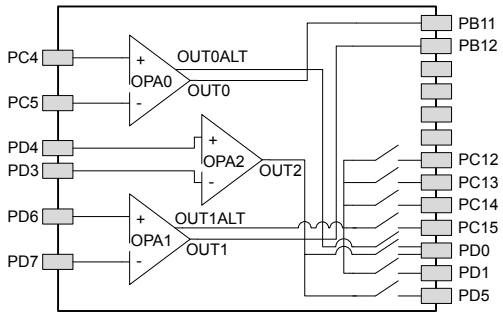


**Figure 5.24. Opamp Pinout**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_A04 | PB10 | PB10 | PB10 | | | | | External Bus Interface (EBI) address output pin 04. |
| EBI_A05 | PC6 | PC6 | PC6 | | | | | External Bus Interface (EBI) address output pin 05. |
| EBI_A06 | PC7 | PC7 | PC7 | | | | | External Bus Interface (EBI) address output pin 06. |
| EBI_A07 | PE0 | PE0 | PE0 | | | | | External Bus Interface (EBI) address output pin 07. |
| EBI_A08 | PE1 | PE1 | PE1 | | | | | External Bus Interface (EBI) address output pin 08. |
| EBI_A09 | PE2 | PC9 | PC9 | | | | | External Bus Interface (EBI) address output pin 09. |
| EBI_A10 | PE3 | PC10 | PC10 | | | | | External Bus Interface (EBI) address output pin 10. |
| EBI_A11 | PE4 | PE4 | PE4 | | | | | External Bus Interface (EBI) address output pin 11. |
| EBI_A12 | PE5 | PE5 | PE5 | | | | | External Bus Interface (EBI) address output pin 12. |
| EBI_A13 | PE6 | PE6 | PE6 | | | | | External Bus Interface (EBI) address output pin 13. |
| EBI_A14 | PE7 | PE7 | PE7 | | | | | External Bus Interface (EBI) address output pin 14. |
| EBI_A15 | PC8 | PC8 | PC8 | | | | | External Bus Interface (EBI) address output pin 15. |
| EBI_A16 | PB0 | PB0 | PB0 | | | | | External Bus Interface (EBI) address output pin 16. |
| EBI_A17 | PB1 | PB1 | PB1 | | | | | External Bus Interface (EBI) address output pin 17. |
| EBI_A18 | PB2 | PB2 | PB2 | | | | | External Bus Interface (EBI) address output pin 18. |
| EBI_A19 | PB3 | PB3 | PB3 | | | | | External Bus Interface (EBI) address output pin 19. |
| EBI_A20 | PB4 | PB4 | PB4 | | | | | External Bus Interface (EBI) address output pin 20. |
| EBI_A21 | PB5 | PB5 | PB5 | | | | | External Bus Interface (EBI) address output pin 21. |
| EBI_A22 | PB6 | PB6 | PB6 | | | | | External Bus Interface (EBI) address output pin 22. |
| EBI_A23 | PC0 | PC0 | PC0 | | | | | External Bus Interface (EBI) address output pin 23. |
| EBI_A24 | PC1 | PC1 | PC1 | | | | | External Bus Interface (EBI) address output pin 24. |
| EBI_A25 | PC2 | PC2 | PC2 | | | | | External Bus Interface (EBI) address output pin 25. |
| EBI_A26 | PC4 | PC4 | PC4 | | | | | External Bus Interface (EBI) address output pin 26. |
| EBI_A27 | PD2 | PD2 | PD2 | | | | | External Bus Interface (EBI) address output pin 27. |
| EBI_AD00 | PE8 | PE8 | PE8 | | | | | External Bus Interface (EBI) address and data input / output pin 00. |
| EBI_AD01 | PE9 | PE9 | PE9 | | | | | External Bus Interface (EBI) address and data input / output pin 01. |
| EBI_AD02 | PE10 | PE10 | PE10 | | | | | External Bus Interface (EBI) address and data input / output pin 02. |
| EBI_AD03 | PE11 | PE11 | PE11 | | | | | External Bus Interface (EBI) address and data input / output pin 03. |
| EBI_AD04 | PE12 | PE12 | PE12 | | | | | External Bus Interface (EBI) address and data input / output pin 04. |
| EBI_AD05 | PE13 | PE13 | PE13 | | | | | External Bus Interface (EBI) address and data input / output pin 05. |
| EBI_AD06 | PE14 | PE14 | PE14 | | | | | External Bus Interface (EBI) address and data input / output pin 06. |

### 5.15.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

**Note:** Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

**Table 5.44. Alternate functionality overview**

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ACMP0_CH0 | PC0 | | | | | | | Analog comparator ACMP0, channel 0. |
| ACMP0_CH1 | PC1 | | | | | | | Analog comparator ACMP0, channel 1. |
| ACMP0_CH2 | PC2 | | | | | | | Analog comparator ACMP0, channel 2. |
| ACMP0_CH3 | PC3 | | | | | | | Analog comparator ACMP0, channel 3. |
| ACMP0_CH4 | PC4 | | | | | | | Analog comparator ACMP0, channel 4. |
| ACMP0_CH5 | PC5 | | | | | | | Analog comparator ACMP0, channel 5. |
| ACMP0_CH6 | PC6 | | | | | | | Analog comparator ACMP0, channel 6. |
| ACMP0_CH7 | PC7 | | | | | | | Analog comparator ACMP0, channel 7. |
| ACMP0_O | PE13 | PE2 | PD6 | | | | | Analog comparator ACMP0, digital output. |
| ACMP1_CH0 | PC8 | | | | | | | Analog comparator ACMP1, channel 0. |
| ACMP1_CH1 | PC9 | | | | | | | Analog comparator ACMP1, channel 1. |
| ACMP1_CH2 | PC10 | | | | | | | Analog comparator ACMP1, channel 2. |
| ACMP1_CH3 | PC11 | | | | | | | Analog comparator ACMP1, channel 3. |
| ACMP1_CH4 | PC12 | | | | | | | Analog comparator ACMP1, channel 4. |
| ACMP1_CH5 | PC13 | | | | | | | Analog comparator ACMP1, channel 5. |
| ACMP1_CH6 | PC14 | | | | | | | Analog comparator ACMP1, channel 6. |
| ACMP1_CH7 | PC15 | | | | | | | Analog comparator ACMP1, channel 7. |
| ACMP1_O | PF2 | PE3 | PD7 | | | | | Analog comparator ACMP1, digital output. |
| ADC0_CH0 | PD0 | | | | | | | Analog to digital converter ADC0, input channel number 0. |
| ADC0_CH1 | PD1 | | | | | | | Analog to digital converter ADC0, input channel number 1. |
| ADC0_CH2 | PD2 | | | | | | | Analog to digital converter ADC0, input channel number 2. |
| ADC0_CH3 | PD3 | | | | | | | Analog to digital converter ADC0, input channel number 3. |
| ADC0_CH4 | PD4 | | | | | | | Analog to digital converter ADC0, input channel number 4. |
| ADC0_CH5 | PD5 | | | | | | | Analog to digital converter ADC0, input channel number 5. |
| ADC0_CH6 | PD6 | | | | | | | Analog to digital converter ADC0, input channel number 6. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| ADC0_CH7 | PD7 | | | | | | | Analog to digital converter ADC0, input channel number 7. |
| BOOT_RX | PE11 | | | | | | | Bootloader RX. |
| BOOT_TX | PE10 | | | | | | | Bootloader TX. |
| BU_STAT | PE3 | | | | | | | Backup Power Domain status, whether or not the system is in backup mode |
| BU_VIN | PD8 | | | | | | | Battery input for Backup Power Domain |
| BU_VOUT | PE2 | | | | | | | Power output for Backup Power Domain |
| CMU_CLK0 | PA2 | PC12 | PD7 | | | | | Clock Management Unit, clock output number 0. |
| CMU_CLK1 | PA1 | PD8 | PE12 | | | | | Clock Management Unit, clock output number 1. |
| OPAMP_N0 | PC5 | | | | | | | Operational Amplifier 0 external negative input. |
| OPAMP_N1 | PD7 | | | | | | | Operational Amplifier 1 external negative input. |
| OPAMP_N2 | PD3 | | | | | | | Operational Amplifier 2 external negative input. |
| DAC0_OUT0 / OPAMP_OUT0 | PB11 | | | | | | | Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0. |
| DAC0_OUT0ALT / OPAMP_OUT0ALT | PC0 | PC1 | PC2 | PC3 | PD0 | | | Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0. |
| DAC0_OUT1 / OPAMP_OUT1 | PB12 | | | | | | | Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1. |
| DAC0_OUT1ALT / OPAMP_OUT1ALT | PC12 | PC13 | PC14 | PC15 | PD1 | | | Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1. |
| OPAMP_OUT2 | PD5 | PD0 | | | | | | Operational Amplifier 2 output. |
| OPAMP_P0 | PC4 | | | | | | | Operational Amplifier 0 external positive input. |
| OPAMP_P1 | PD6 | | | | | | | Operational Amplifier 1 external positive input. |
| OPAMP_P2 | PD4 | | | | | | | Operational Amplifier 2 external positive input. |
| DBG_SWCLK | PF0 | PF0 | PF0 | PF0 | | | | Debug-interface Serial Wire clock input.<br>Note that this function is enabled to pin out of reset, and has a built-in pull down. |
| DBG_SWDIO | PF1 | PF1 | PF1 | PF1 | | | | Debug-interface Serial Wire data input / output.<br>Note that this function is enabled to pin out of reset, and has a built-in pull up. |
| DBG_SWO | PF2 | | PD1 | PD2 | | | | Debug-interface Serial Wire viewer Output.<br>Note that this function is not enabled after reset, and must be enabled by software to be used. |
| EBI_A00 | PA12 | PA12 | PA12 | | | | | External Bus Interface (EBI) address output pin 00. |
| EBI_A01 | PA13 | PA13 | PA13 | | | | | External Bus Interface (EBI) address output pin 01. |
| EBI_A02 | PA14 | PA14 | PA14 | | | | | External Bus Interface (EBI) address output pin 02. |
| EBI_A03 | PB9 | PB9 | PB9 | | | | | External Bus Interface (EBI) address output pin 03. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| EBI_AD07 | PE15 | PE15 | PE15 | | | | | External Bus Interface (EBI) address and data input / output pin 07. |
| EBI_AD08 | PA15 | PA15 | PA15 | | | | | External Bus Interface (EBI) address and data input / output pin 08. |
| EBI_AD09 | PA0 | PA0 | PA0 | | | | | External Bus Interface (EBI) address and data input / output pin 09. |
| EBI_AD10 | PA1 | PA1 | PA1 | | | | | External Bus Interface (EBI) address and data input / output pin 10. |
| EBI_AD11 | PA2 | PA2 | PA2 | | | | | External Bus Interface (EBI) address and data input / output pin 11. |
| EBI_AD12 | PA3 | PA3 | PA3 | | | | | External Bus Interface (EBI) address and data input / output pin 12. |
| EBI_AD13 | PA4 | PA4 | PA4 | | | | | External Bus Interface (EBI) address and data input / output pin 13. |
| EBI_AD14 | PA5 | PA5 | PA5 | | | | | External Bus Interface (EBI) address and data input / output pin 14. |
| EBI_AD15 | PA6 | PA6 | PA6 | | | | | External Bus Interface (EBI) address and data input / output pin 15. |
| EBI_ALE | PF3 | PC11 | PC11 | | | | | External Bus Interface (EBI) Address Latch Enable output. |
| EBI_ARDY | PF2 | PF2 | PF2 | | | | | External Bus Interface (EBI) Hardware Ready Control input. |
| EBI_BL0 | PF6 | PF6 | PF6 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 0. |
| EBI_BL1 | PF7 | PF7 | PF7 | | | | | External Bus Interface (EBI) Byte Lane/Enable pin 1. |
| EBI_CS0 | PD9 | PD9 | PD9 | | | | | External Bus Interface (EBI) Chip Select output 0. |
| EBI_CS1 | PD10 | PD10 | PD10 | | | | | External Bus Interface (EBI) Chip Select output 1. |
| EBI_CS2 | PD11 | PD11 | PD11 | | | | | External Bus Interface (EBI) Chip Select output 2. |
| EBI_CS3 | PD12 | PD12 | PD12 | | | | | External Bus Interface (EBI) Chip Select output 3. |
| EBI_CSTFT | PA7 | PA7 | PA7 | | | | | External Bus Interface (EBI) Chip Select output TFT. |
| EBI_DCLK | PA8 | PA8 | PA8 | | | | | External Bus Interface (EBI) TFT Dot Clock pin. |
| EBI_DTEN | PA9 | PA9 | PA9 | | | | | External Bus Interface (EBI) TFT Data Enable pin. |
| EBI_HSNC | PA11 | PA11 | PA11 | | | | | External Bus Interface (EBI) TFT Horizontal Synchronization pin. |
| EBI_NANDREn | PC3 | PC3 | PC3 | | | | | External Bus Interface (EBI) NAND Read Enable output. |
| EBI_NANDWEn | PC5 | PC5 | PC5 | | | | | External Bus Interface (EBI) NAND Write Enable output. |
| EBI_REn | PF5 | PF9 | PF5 | | | | | External Bus Interface (EBI) Read Enable output. |
| EBI_VSNC | PA10 | PA10 | PA10 | | | | | External Bus Interface (EBI) TFT Vertical Synchronization pin. |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| TIM0_CDTI0 | PA3 | PC13 | PF3 | PC13 | PC2 | PF3 | | Timer 0 Complimentary Deat Time Insertion channel 0. |
| TIM0_CDTI1 | PA4 | PC14 | PF4 | PC14 | PC3 | PF4 | | Timer 0 Complimentary Deat Time Insertion channel 1. |
| TIM0_CDTI2 | PA5 | PC15 | PF5 | PC15 | PC4 | PF5 | | Timer 0 Complimentary Deat Time Insertion channel 2. |
| TIM1_CC0 | PC13 | PE10 | PB0 | PB7 | PD6 | | | Timer 1 Capture Compare input / output channel 0. |
| TIM1_CC1 | PC14 | PE11 | PB1 | PB8 | PD7 | | | Timer 1 Capture Compare input / output channel 1. |
| TIM1_CC2 | PC15 | PE12 | PB2 | PB11 | PC13 | | | Timer 1 Capture Compare input / output channel 2. |
| TIM2_CC0 | PA8 | PA12 | PC8 | | | | | Timer 2 Capture Compare input / output channel 0. |
| TIM2_CC1 | PA9 | PA13 | PC9 | | | | | Timer 2 Capture Compare input / output channel 1. |
| TIM2_CC2 | PA10 | PA14 | PC10 | | | | | Timer 2 Capture Compare input / output channel 2. |
| TIM3_CC0 | PE14 | PE0 | | | | | | Timer 3 Capture Compare input / output channel 0. |
| TIM3_CC1 | PE15 | PE1 | | | | | | Timer 3 Capture Compare input / output channel 1. |
| TIM3_CC2 | PA15 | PE2 | | | | | | Timer 3 Capture Compare input / output channel 2. |
| U0_RX | PF7 | PE1 | PA4 | PC15 | | | | UART0 Receive input. |
| U0_TX | PF6 | PE0 | PA3 | PC14 | | | | UART0 Transmit output. Also used as receive input in half duplex communication. |
| U1_RX | PC13 | PF11 | PB10 | PE3 | | | | UART1 Receive input. |
| U1_TX | PC12 | PF10 | PB9 | PE2 | | | | UART1 Transmit output. Also used as receive input in half duplex communication. |
| US0_CLK | PE12 | PE5 | PC9 | PC15 | PB13 | PB13 | | USART0 clock input / output. |
| US0_CS | PE13 | PE4 | PC8 | PC14 | PB14 | PB14 | | USART0 chip select input / output. |
| US0_RX | PE11 | PE6 | PC10 | PE12 | PB8 | PC1 | | USART0 Asynchronous Receive.<br>USART0 Synchronous mode Master Input / Slave Output (MISO). |
| US0_TX | PE10 | PE7 | PC11 | PE13 | PB7 | PC0 | | USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART0 Synchronous mode Master Output / Slave Input (MOSI). |
| US1_CLK | PB7 | PD2 | PF0 | | | | | USART1 clock input / output. |
| US1_CS | PB8 | PD3 | PF1 | | | | | USART1 chip select input / output. |
| US1_RX | PC1 | PD1 | PD6 | | | | | USART1 Asynchronous Receive.<br>USART1 Synchronous mode Master Input / Slave Output (MISO). |
| US1_TX | PC0 | PD0 | PD7 | | | | | USART1 Asynchronous Transmit.Also used as receive input in half duplex communication.<br>USART1 Synchronous mode Master Output / Slave Input (MOSI). |
| US2_CLK | PC4 | PB5 | | | | | | USART2 clock input / output. |

### 5.18 EFM32LG940 (QFN64)

#### 5.18.1 Pinout

The EFM32LG940 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

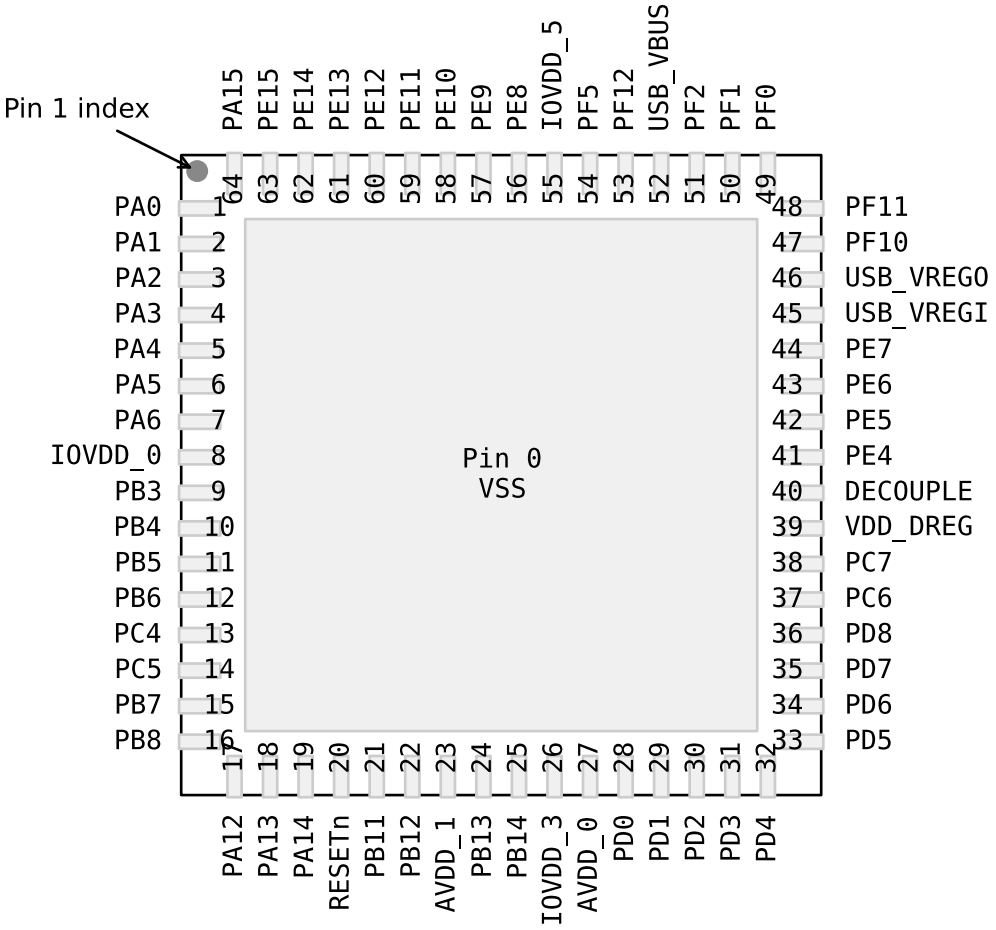


**Figure 5.35. EFM32LG940 Pinout (top view, not to scale)**

**Table 5.52. Device Pinout**

| QFN64 Pin# and Name | | Pin Alternate Functionality / Description | | | |
|---|---|---|---|---|---|
| Pin # | Pin Name | Analog | Timers | Communication | Other |
| 0 | VSS | Ground. | | | |
| 1 | PA0 | LCD_SEG13 | TIM0_CC0 #0/1/4 | LEU0_RX #4 I2C0_SDA #0 | PRS_CH0 #0 GPIO_EM4WU0 |

| Alternate | LOCATION | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Functionality | 0 | 1 | 2 | 3 | 4 | 5 | 6 | Description |
| LCD_BCAP_P | PA12 | | | | | | | LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P. |
| LCD_BEXT | PA14 | | | | | | | LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS.<br>An external LCD voltage may also be applied to this pin if the booster is not enabled.<br>If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO. |
| LCD_COM0 | PE4 | | | | | | | LCD driver common line number 0. |
| LCD_COM1 | PE5 | | | | | | | LCD driver common line number 1. |
| LCD_COM2 | PE6 | | | | | | | LCD driver common line number 2. |
| LCD_COM3 | PE7 | | | | | | | LCD driver common line number 3. |
| LCD_SEG0 | PF2 | | | | | | | LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG3 | PF5 | | | | | | | LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0. |
| LCD_SEG4 | PE8 | | | | | | | LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG5 | PE9 | | | | | | | LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG6 | PE10 | | | | | | | LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG7 | PE11 | | | | | | | LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1. |
| LCD_SEG8 | PE12 | | | | | | | LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG9 | PE13 | | | | | | | LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG10 | PE14 | | | | | | | LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG11 | PE15 | | | | | | | LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2. |
| LCD_SEG13 | PA0 | | | | | | | LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG14 | PA1 | | | | | | | LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG15 | PA2 | | | | | | | LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3. |
| LCD_SEG16 | PA3 | | | | | | | LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |
| LCD_SEG17 | PA4 | | | | | | | LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4. |

### 7.3 BGA120 Package Marking

In the illustration below package fields and position are shown.

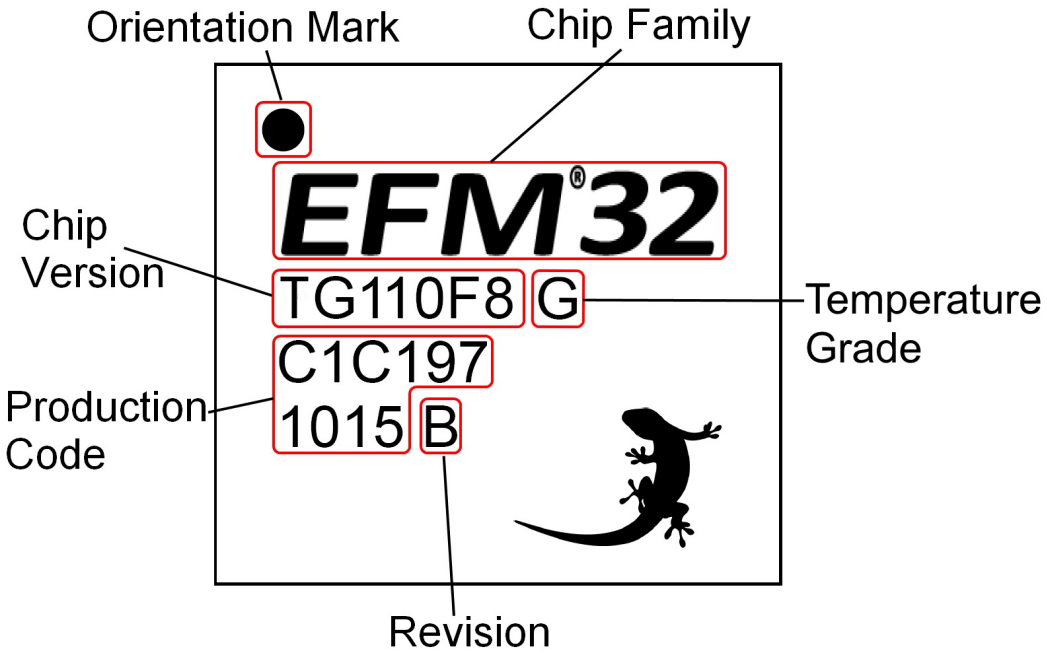


**Figure 7.5. Example Chip Marking (Top View)**

### 10.3 TQFP64 Package Marking

In the illustration below package fields and position are shown.

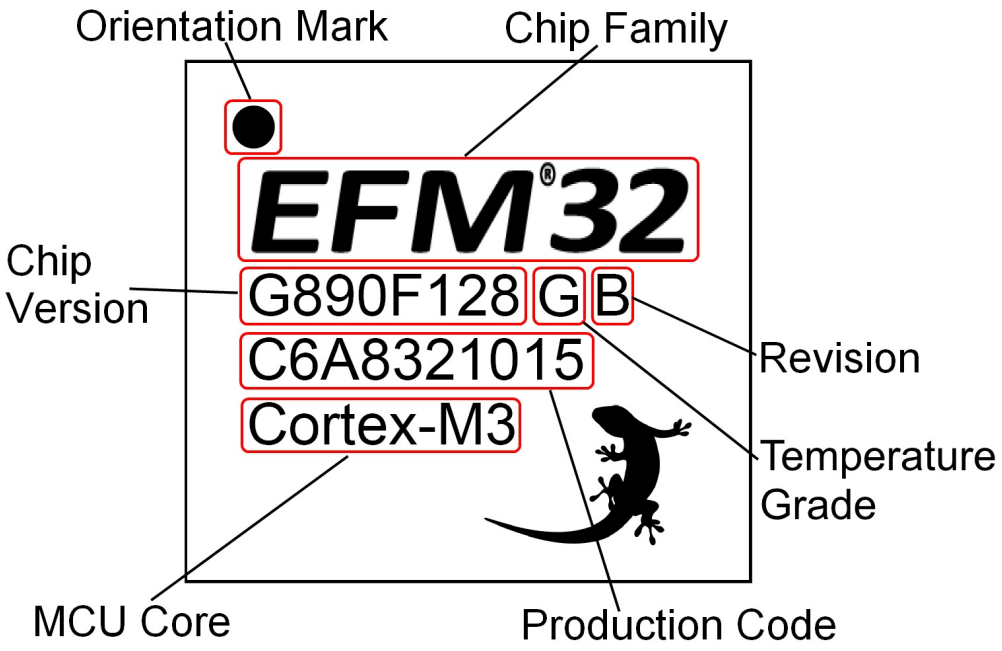


**Figure 10.5. Example Chip Marking (Top View)**