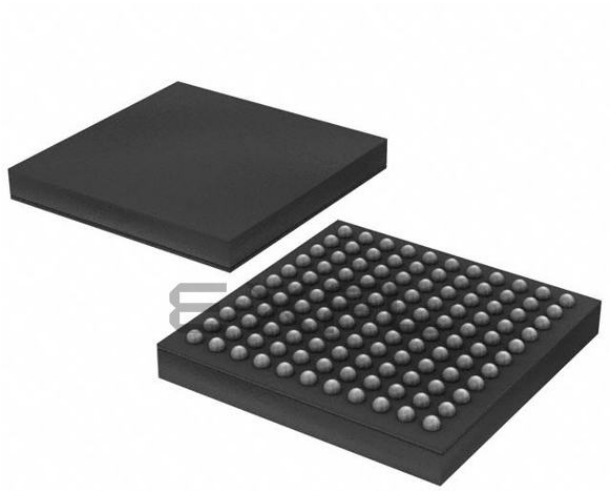

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I²C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg895f256-bga120

2. Ordering Information

The following table shows the available EFM32LG devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (ºC)	Package
EFM32LG230F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG230F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG230F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG232F64G-E-QFP64	64	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG232F128G-E-QFP64	128	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG232F256G-E-QFP64	256	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG280F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG280F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG280F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG290F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG290F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG290F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG295F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG295F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG295F256G-E-BGA120	256	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG330F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG330F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG330F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG332F64G-E-QFP64	64	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG332F128G-E-QFP64	128	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG332F256G-E-QFP64	256	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG360F64G-E-CSP81	64	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG360F128G-E-CSP81	128	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG360F256G-E-CSP81	256	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG380F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG380F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG380F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG390F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG390F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG390F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG395F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG395F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120

Module	Configuration	Pin Connections
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	93 pins	Available pins are shown in 5.11.3 GPIO Pinout Overview

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	1 MSamples/s, 12 bit, single ended, internal 1.25 V reference	—	64	—	dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5 V reference	—	76	—	dBc
		1 MSamples/s, 12 bit, single ended, VDD reference	—	73	—	dBc
		1 MSamples/s, 12 bit, differential, internal 1.25 V reference	—	66	—	dBc
		1 MSamples/s, 12 bit, differential, internal 2.5 V reference	—	77	—	dBc
		1 MSamples/s, 12 bit, differential, VDD reference	—	76	—	dBc
		1 MSamples/s, 12 bit, differential, 2xVDD reference	—	75	—	dBc
		1 MSamples/s, 12 bit, differential, 5 V reference	—	69	—	dBc
		200 kSamples/s, 12 bit, single ended, internal 1.25 V reference	—	75	—	dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5 V reference	—	75	—	dBc
		200 kSamples/s, 12 bit, single ended, VDD reference	—	76	—	dBc
		200 kSamples/s, 12 bit, differential, internal 1.25 V reference	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, internal 2.5 V reference	—	79	—	dBc
		200 kSamples/s, 12 bit, differential, 5 V reference	—	78	—	dBc
Spurious-Free Dynamic Range (SFDR)	$SFDR_{ADC}$	200 kSamples/s, 12 bit, differential, VDD reference	68	79	—	dBc
		200 kSamples/s, 12 bit, differential, 2xVDD reference	—	79	—	dBc
Offset voltage	$V_{ADCOFFSET}$	After calibration, single ended	-3.5	0.3	3	mV
		After calibration, differential	—	0.3	—	mV
Thermometer output gradient	$TGRAD_{ADCTH}$		—	-1.92	—	mV/°C
			—	-6.3	—	ADC Codes/°C
Differential non-linearity (DNL)	DNL_{ADC}		-1	±0.7	4	LSB
Integral non-linearity (INL), End point method	INL_{ADC}		—	±1.2	±3	LSB
Missing codes	MC_{ADC}		11.999[1]	12	—	bits
Gain error drift	$GAIN_{ED}$	1.25 V reference	—	0.01[2]	0.033[3]	%/°C
		2.5 V reference	—	0.01[2]	0.03[3]	%/°C

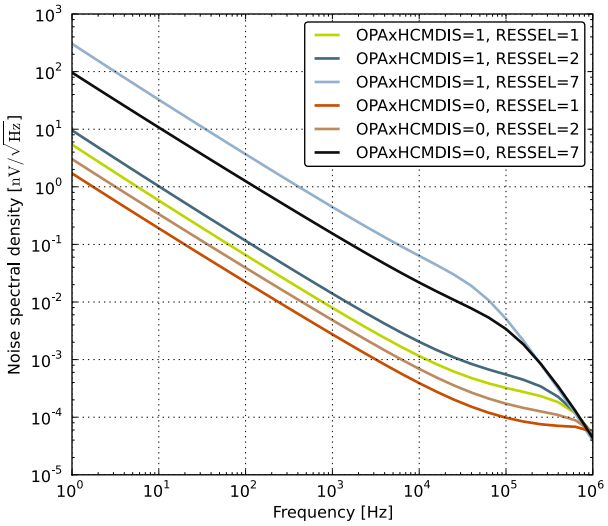

Figure 4.35. OPAMP Voltage Noise Spectral Density(Non-Unity Gain)

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
30	PD2	ADC0_CH2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
31	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 OPAMP_P1	TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 OPAMP_N1	TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
42	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
43	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
44	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0
45	USB_VREGI				
46	USB_VREGO				
47	PF10			USB_DM	
48	PF11			USB_DP	
49	PF0		TIM0_CC0 #5 LE-TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
50	PF1		TIM0_CC1 #5 LE-TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
G1	PB5		EBI_A21 #0/1/2		US2_CLK #1	
G2	PB6		EBI_A22 #0/1/2		US2_CS #1	
G3	VSS	Ground.				
G4	IOVDD_0	Digital IO power supply 0.				
G8	IOVDD_4	Digital IO power supply 4.				
G9	VSS	Ground.				
G10	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
G11	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
H1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
H2	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
H3	PD14				I2C0_SDA #3	
H4	PA7		EBI_CSTFT #0/1/2			
H5	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
H6	VSS	Ground.				
H7	IOVDD_3	Digital IO power supply 3.				
H8	PD8	BU_VIN				CMU_CLK1 #1
H9	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2
H10	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
H11	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
J1	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
J2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
J3	PD15				I2C0_SCL #3	
J4	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
J5	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
J6	PA10		EBI_VSNC #0/1/2	TIM2_CC2 #0		
J7	PB9		EBI_A03 #0/1/2		U1_TX #2	
J8	PB10		EBI_A04 #0/1/2		U1_RX #2	
J9	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
J10	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
J11	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
K1	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
K2	PC4	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LE- TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
K3	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
K4	VSS	Ground.				
K5	PA11		EBI_HSNC #0/1/2			
K6	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
K7	AVSS_1	Analog ground 1.				
K8	AVDD_2	Analog power supply 2.				
K9	AVDD_1	Analog power supply 1.				
K10	AVSS_0	Analog ground 0.				
K11	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
L1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
L2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
L3	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
L6	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
L9	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.10.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG390 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.30. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	PA15	PA14	PA13	PA12	PA11	PA10	PA9	PA8	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
Port B	PB15	PB14	PB13	PB12	PB11	PB10	PB9	PB8	PB7	PB6	PB5	PB4	PB3	PB2	PB1	PB0
Port C	—	—	—	—	PC11	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
Port D	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Port F	—	—	—	PF12	PF11	PF10	PF9	PF8	PF7	PF6	PF5	—	—	PF2	PF1	PF0

5.10.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG390 is shown in the following figure.

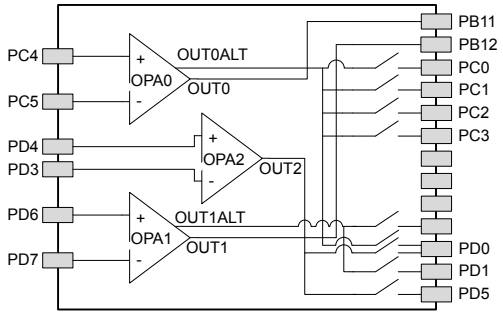

Figure 5.20. Opamp Pinout

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
C5	VSS	Ground.				
C6	IOVDD_0	Digital IO power supply 0.				
C7	PF9		EBI_REn #1			ETM_TD0 #1
C8	VSS	Ground.				
C9	IOVDD_1	Digital IO power supply 1.				
C10	PF0			TIM0_CC0 #5 LE-TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
C11	PE4		EBI_A11 #0/1/2		US0_CS #1	
C12	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
C13	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
D1	PA3		EBI_AD12 #0/1/2	TIM0_CDTI0 #0	U0_TX #2	LES_ALTEX2 #0 ETM_TD1 #3
D2	PA2		EBI_AD11 #0/1/2	TIM0_CC2 #0/1		CMU_CLK0 #0 ETM_TD0 #3
D3	PB15					ETM_TD2 #1
D11	PE5		EBI_A12 #0/1/2		US0_CLK #1	
D12	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
D13	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
E1	PA6		EBI_AD15 #0/1/2		LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
E2	PA5		EBI_AD14 #0/1/2	TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
E3	PA4		EBI_AD13 #0/1/2	TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
E11	PE6		EBI_A13 #0/1/2		US0_RX #1	
E12	PC10	ACMP1_CH2	EBI_A10 #1/2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
E13	PC11	ACMP1_CH3	EBI_ALE #1/2		US0_TX #2	LES_CH11 #0
F1	PB0		EBI_A16 #0/1/2	TIM1_CC0 #2		
F2	PB1		EBI_A17 #0/1/2	TIM1_CC1 #2		
F3	PB2		EBI_A18 #0/1/2	TIM1_CC2 #2		

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
L1	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	EBI_A25 #0/1/2	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0
L2	PC3	ACMP0_CH3 DAC0_OUT0ALT #3/ OPAMP_OUT0ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
L3	PA7		EBI_CSTFT #0/1/2			
L4	IOVDD_5	Digital IO power supply 5.				
L5	VSS	Ground.				
L6	VSS	Ground.				
L7	IOVDD_6	Digital IO power supply 6.				
L8	PB9		EBI_A03 #0/1/2		U1_TX #2	
L9	PB10		EBI_A04 #0/1/2		U1_RX #2	
L10	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
L11	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
L12	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
L13	PD7	ADC0_CH7 OPAMP_N1		TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
M1	PB7	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
M2	PC4	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LE-TIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
M3	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
M4	PA10		EBI_VSNC #0/1/2	TIM2_CC2 #0		
M5	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
M6	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
M7	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
M8	AVSS_1	Analog ground 1.				
M9	AVDD_2	Analog power supply 2.				
M10	AVDD_1	Analog power supply 1.				

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
M11	AVSS_0	Analog ground 0.				
M12	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
M13	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
N1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
N2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
N3	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		
N4	PA11		EBI_HSNC #0/1/2			
N5	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
N6	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE-TIM0_OUT0 #1	I2C1_SDA #1	
N7	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
N8	AVSS_2	Analog ground 2.				
N9	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
N10	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
N11	AVDD_0	Analog power supply 0.				
N12	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
N13	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A3	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
A4	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
A5	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
A6	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
A7	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
A8	PF4	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
A9	PE4	LCD_COM0	EBI_A11 #0/1/2		US0_CS #1	
A10	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3U0_TX #3	LES_CH14 #0
A11	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
B1	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		
B2	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
B3	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
B4	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
B5	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
B6	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
B7	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
B8	PF3	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
B9	PE5	LCD_COM1	EBI_A12 #0/1/2		US0_CLK #1	
B10	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
B11	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT		TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0	U1_RX #0	LES_CH13 #0
C1	PA1	LCD_SEG14	EBI_AD10 #0/1/2	TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0
C2	PA0	LCD_SEG13	EBI_AD09 #0/1/2	TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
C3	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
C4	PD13					ETM_TD1 #1

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2	PC12	PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0ALT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT	PC12	PC13	PC14	PC15	PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
30	PD2	ADC0_CH2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
31	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 OPAMP_P1	TIM1_CC0 #4 LE-TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 OPAMP_N1	TIM1_CC1 #4 LE-TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C_{DECOUPLE}$ is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	USB_VREGI				
46	USB_VREGO				
47	PF10			USB_DM	
48	PF11			USB_DP	
49	PF0		TIM0_CC0 #5 LE-TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
50	PF1		TIM0_CC1 #5 LE-TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
51	PF2	LCD_SEG0	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
DAC0_OUT0ALT / OPAMP_OUT0ALT					PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
ETM_TCLK	PD7		PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6		PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFXTAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFXTAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7			PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6			PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12						I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.

5.19.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG942 is shown in the following figure.

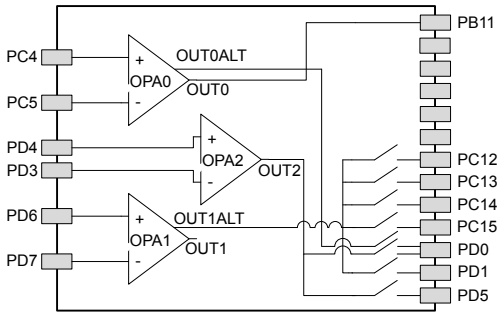

Figure 5.38. Opamp Pinout

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
77	PF1			TIM0_CC1 #5 LE-TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
78	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
79	USB_VBUS	USB 5.0 V VBUS input.				
80	PF12				USB_ID	
81	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
82	IOVDD_5	Digital IO power supply 5.				
83	VSS	Ground.				
84	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
85	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
86	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
87	PF9	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
88	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
89	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
90	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
91	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
92	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
93	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
94	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
95	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
96	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
97	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
98	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
99	PE15	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
100	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		

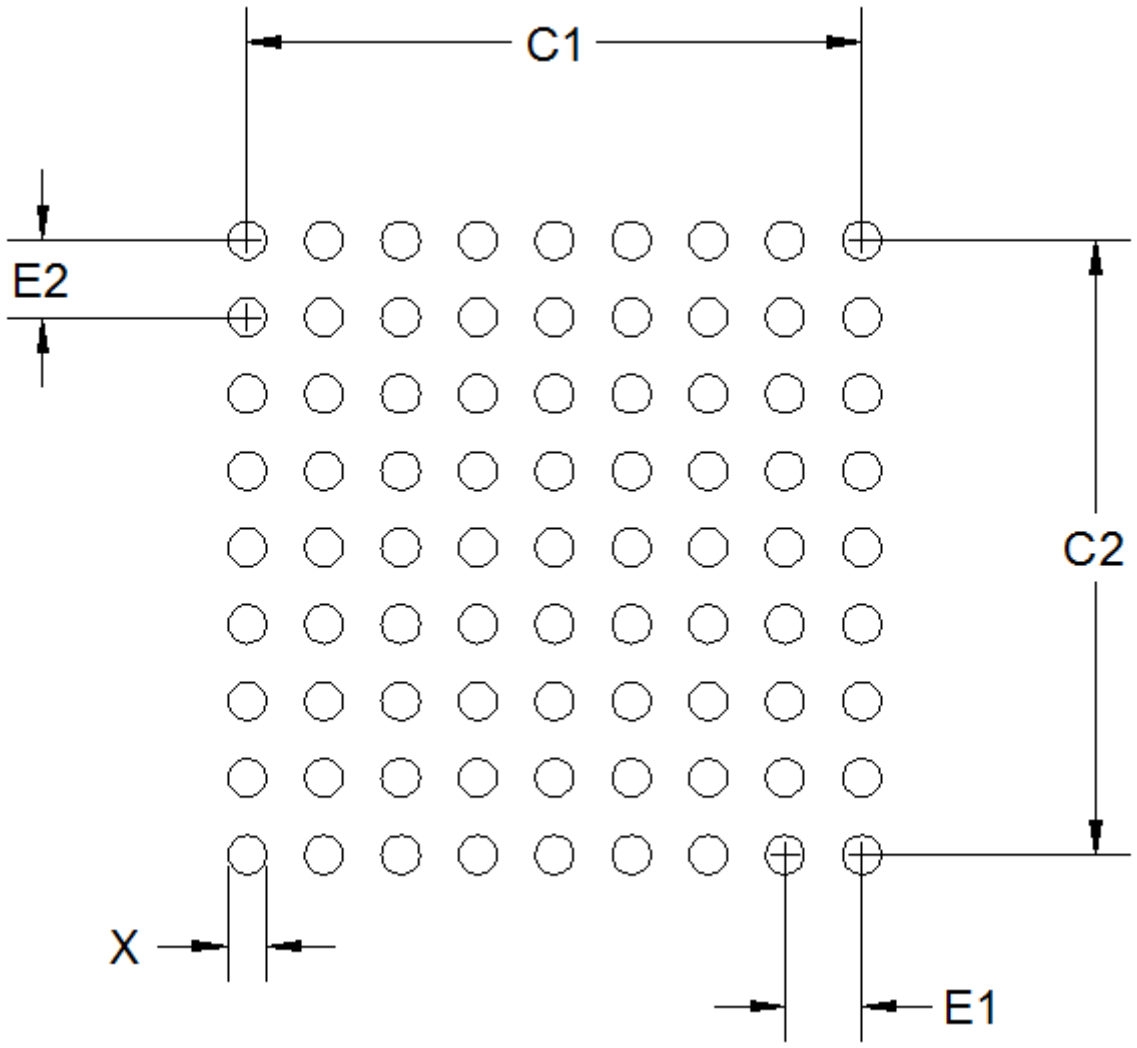

Figure 8.3. CSP81 PCB Solder Mask

Table 8.3. CSP81 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
X	0.26
C1	3.20
C2	3.20
E1	0.40
E2	0.40

Table 11.3. QFN64 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.97	e	8.90
b	0.42	f	7.32
c	0.50	g	7.32
d	8.90	-	-

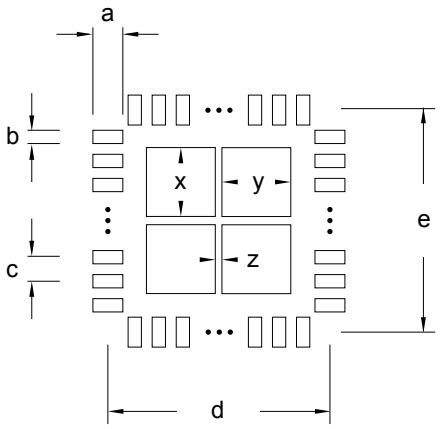

Figure 11.4. QFN64 PCB Stencil Design

Table 11.4. QFN64 PCB Stencil Design Dimensions (Dimensions in mm)

Symbol	Dim. (mm)	Symbol	Dim. (mm)
a	0.75	e	8.90
b	0.22	x	2.70
c	0.50	y	2.70
d	8.90	z	0.80

Note:

1. The drawings are not to scale.
2. All dimensions are in millimeters.
3. All drawings are subject to change without notice.
4. The PCB Land Pattern drawing is in compliance with IPC-7351B.
5. Stencil thickness 0.125 mm.
6. For detailed pin-positioning, see Pin Definitions.

12. Wafer Specifications

12.1 Bonding Instructions

All pads should be bonded out, with the exception of the pads labeled “NC” and listed as “Do not connect” in Padout. Gold bond wires are recommended for these devices.

All three voltage regulator output decouple pads (DEC_0, DEC_1, DEC_2) must be bonded out andelectrically connected on the PCB. In the packaged devices, these three pads are all bonded to a single DECOUPLE pin.

If the USB feature of EFM32LG900 will be used, all of the USB pads must be bonded out, and

- both USB_VREGO_0 and USB_VREGO_1 must be bonded out and electrically connected on the PCB. In the packaged devices, these two pads are both bonded to a single USB_VREGO pin.
- both USB_VREGI_0 and USB_VREGI_1 must be bonded out and electrically connected on the PCB. In the packaged devices, these two pads are both bonded to a single USB_VREGI pin.

12.2 Wafer Description

Table 12.1. Wafer and Die Information

Parameter	Value
Device Family	EFM32LG (Leopard Gecko)
Wafer Diameter	8 in
Die Dimensions (Outer edge of seal ring)	4230 µm × 4230 µm
Wafer Thickness (No backgrind)	725 µm ±15 µm (28.54 mil ±1 mil)
Wafer Identification	Notch
Scribe Street Width	80 µm × 160 µm
Die Per Wafer[1]	Contact sales for information
Passivation	Standard
Wafer Packaging Detail	Wafer Jar
Bond Pad Dimensions	65 µm (parallel to die edge) × 66 µm
Bond Pad Pitch Minimum	76 µm
Maximum Processing Temperature	250°C
Electronic Die Map Format	.txt

Note:
1. This is the Expected Known Good Die yielded per wafer and represents the batch order quantity (one wafer).

12.2.1 Environmental

Bare silicon die are susceptible to mechanical damage and may be sensitive to light. When bare die must be used in an environment exposed to light, it may be necessary to cover the top and sides with an opaque material.

For additional Quality and Environmental information, please see: http://www.silabs.com/support/quality/pages/default.aspx.