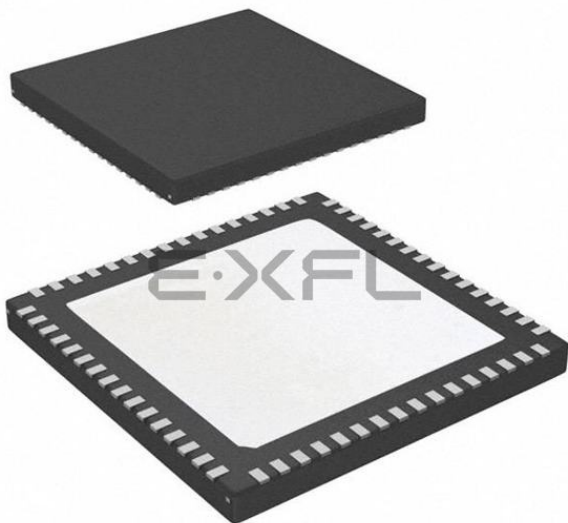




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Details

Product Status	Obsolete
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	53
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-WFQFN Exposed Pad
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg940f64-qfn64

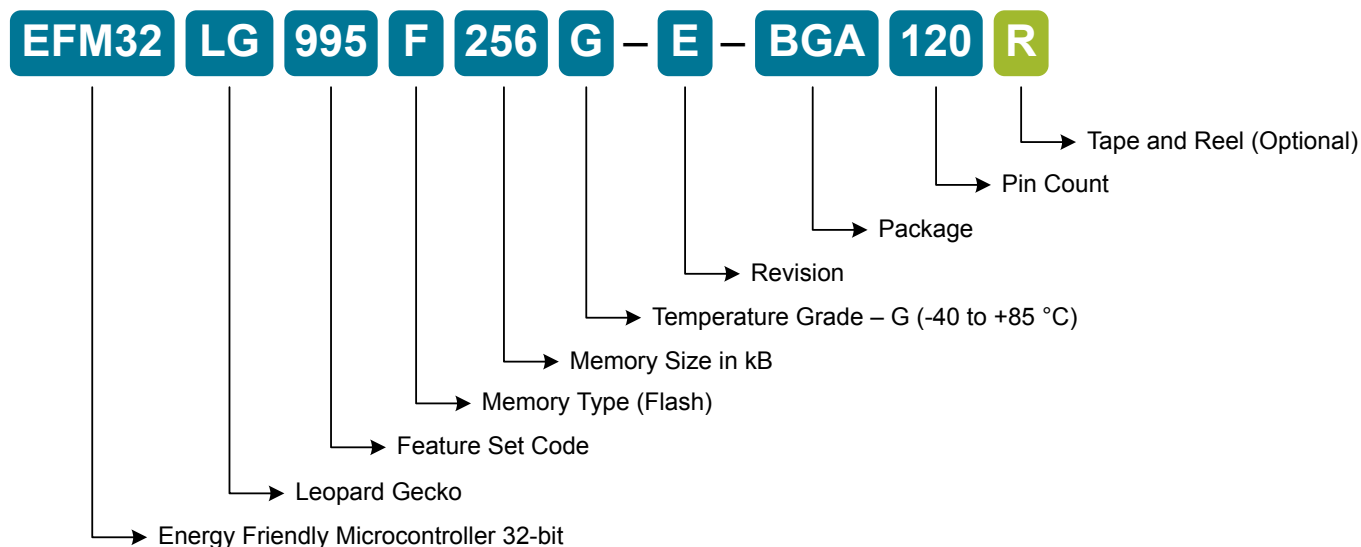


Figure 2.1. Ordering Code Decoder

Adding the suffix 'R' to the part number (e.g. EFM32LGF256G-E-BGA120R) denotes tape and reel.

Visit <http://www.silabs.com> for information on global distributors and representatives.

Module	Configuration	Pin Connections
AES	Full configuration	NA
GPIO	53 pins	Available pins are shown in 5.2.3 GPIO Pinout Overview

Module	Configuration	Pin Connections
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	81 pins	Available pins are shown in 5.20.3 GPIO Pinout Overview
LCD	Full configuration	LCD_SEG[33:0], LCD_COM[7:0], LCD_BCAP_P, LCD_BCAP_N, LCD_BEXT

4.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 4.4. Energy Modes Transitions

Parameter	Symbol	Min	Typ	Max	Unit
Transition time from EM1 to EM0	t_{EM10}	—	0	—	HFCORECLK cycles
Transition time from EM2 to EM0	t_{EM20}	—	2	—	μs
Transition time from EM3 to EM0	t_{EM30}	—	2	—	μs
Transition time from EM4 to EM0	t_{EM40}	—	163	—	μs

4.6 Power Management

The EFM32LG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, *AN0002 EFM32 Hardware Design Considerations*.

Table 4.5. Power Management

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
BOD threshold on falling external supply voltage	$V_{BODextthr-}$		1.74	—	1.96	V
BOD threshold on rising external supply voltage	$V_{BODextthr+}$		—	1.85	1.98	V
Power-on Reset (POR) threshold on rising external supply voltage	$V_{PORthr+}$		—	—	1.98	V
Delay from reset is released until program execution starts	t_{RESET}	Applies to Power-on Reset, Brown-out Reset and pin reset.	—	163	—	μs
Voltage regulator decoupling capacitor.	$C_{DECOUPLE}$	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND	—	1	—	μF
USB voltage regulator out decoupling capacitor.	C_{USB_VREGO}	X5R capacitor recommended. Apply between USB_VREGO pin and GROUND	—	1	—	μF
USB voltage regulator in decoupling capacitor.	C_{USB_VREGI}	X5R capacitor recommended. Apply between USB_VREGI pin and GROUND	—	4.7	—	μF

4.7 Flash

Table 4.6. Flash

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Flash erase cycles before failure	EC _{FLASH}		20000	—	—	cycles
Flash data retention	RET _{FLASH}	T _{AMB} <150 °C	10000	—	—	h
		T _{AMB} <85 °C	10	—	—	years
		T _{AMB} <70 °C	20	—	—	years
Word (32-bit) programming time	t _{W_PROG}		20	—	—	μs
Page erase time	t _{PERASE}		20	20.4	20.8	ms
Device erase time	t _{DERASE}		40	40.8	41.6	ms
Erase current	I _{ERASE}		—	—	7 ¹	mA
Write current	I _{WRITE}		—	—	7 ¹	mA
Supply voltage during flash erase and write	V _{FLASH}		1.98	—	3.8	V
Note: 1. Measured at 25 °C.						

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Note: - Measured with 70 pF load capacitance, 25 °C, and 3 V, using a 100 mV p-p amplitude on the input signal. - Simulated with 70 pF load capacitance, 25 °C, and 3 V, using a 1 mV p-p amplitude on the input signal.						

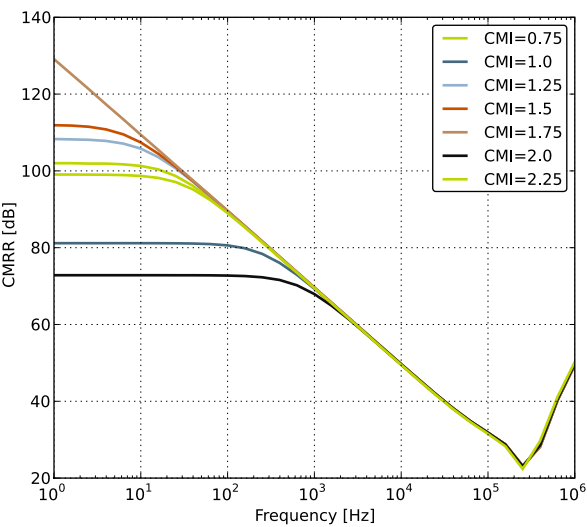


Figure 4.31. OPAMP Common Mode Rejection Ratio

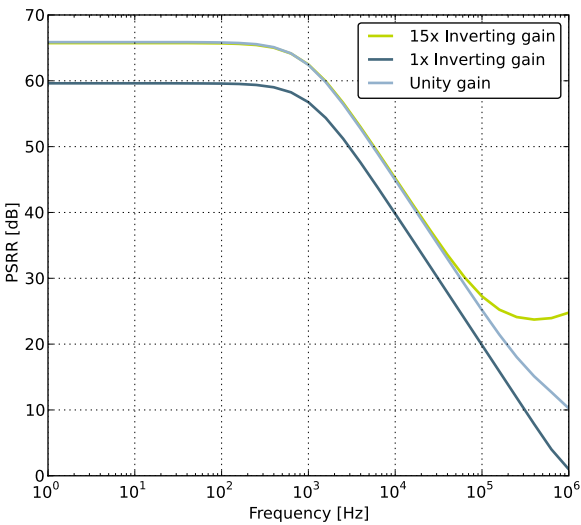


Figure 4.32. OPAMP Positive Power Supply Rejection Ratio

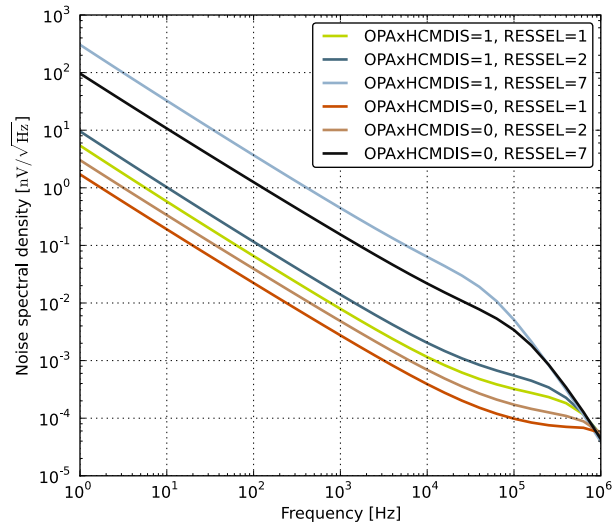


Figure 4.35. OPAMP Voltage Noise Spectral Density(Non-Unity Gain)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Negative response time	$t_{\text{RESPONSE_N}}$	BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=0	—	843	—	ns
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=1	—	1499	—	ns
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=2	—	1590	—	ns
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=3	—	1746	—	ns
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=4	—	1876	—	ns
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=5	—	2104	—	ns
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=6	—	2323	—	ns
		BIASPROG=0b0100, FULL-BIAS=0, HALFBIAS=1, Overdrive = 100 mV, LPREF=0, HYSTSEL=7	—	2691	—	ns

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE	PF3	PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.

5.6 EFM32LG330 (QFN64)

5.6.1 Pinout

The EFM32LG330 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

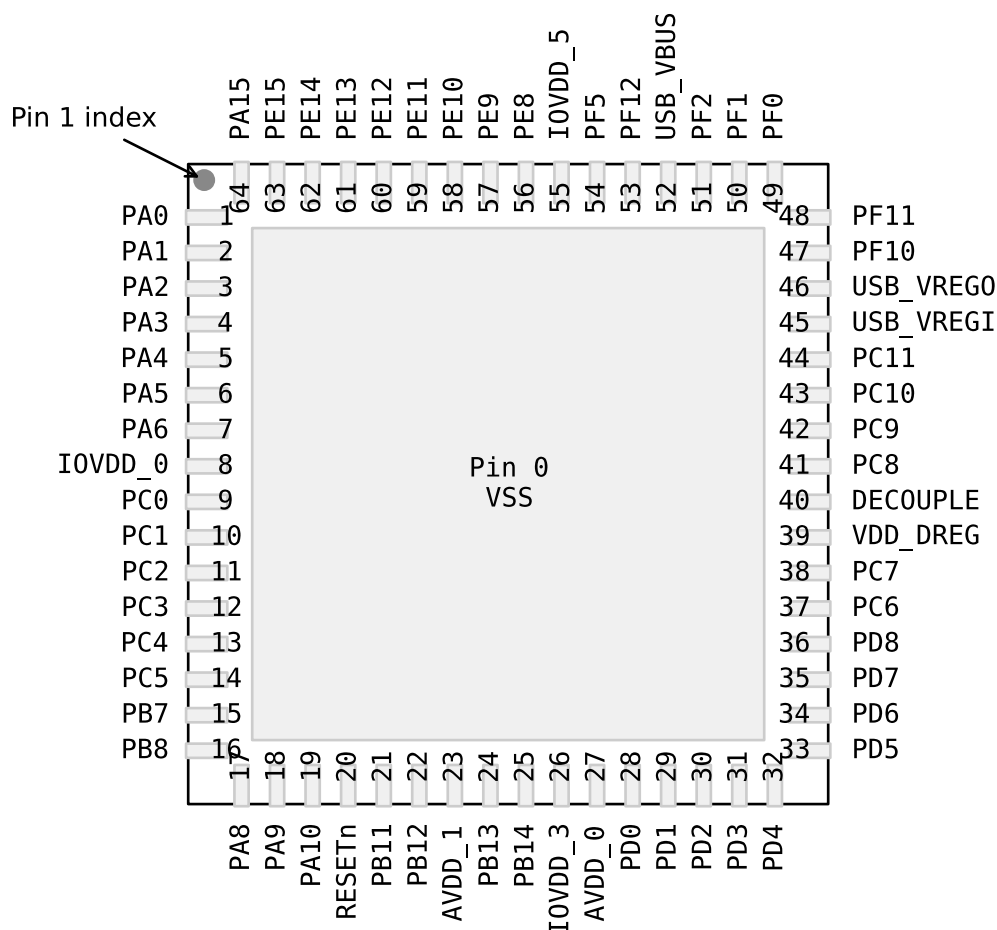


Figure 5.11. EFM32LG330 Pinout (top view, not to scale)

Table 5.16. Device Pinout

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
0	VSS	Ground.			
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0

CSP81 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
D1	PC10	ACMP1_CH2	TIM2_CC2 #2	US0_RX #2	LES_CH10 #0
D2	PC11	ACMP1_CH3		US0_TX #2	LES_CH11 #0
D3	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT		U1_TX #0	CMU_CLK0 #1 LES_CH12 #0
D4	PC9	ACMP1_CH1	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
D5	PC8	ACMP1_CH0	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
D6	PA4		TIM0_CDTI1 #0	U0_RX #2	LES_ALTEX3 #0 ETM_TD2 #3
D7	PA5		TIM0_CDTI2 #0	LEU1_TX #1	LES_ALTEX4 #0 ETM_TD3 #3
D8	PA6			LEU1_RX #1	ETM_TCLK #3 GPIO_EM4WU1
D9	IOVDD_0	Digital IO power supply 0.			
E1	PE4			US0_CS #1	
E2	PE5			US0_CLK #1	
E3	PE3	BU_STAT		U1_RX #3	ACMP1_O #1
E4	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
E5	PE15		TIM3_CC1 #0	LEU0_RX #2	
E6	PB5			US2_CLK #1	
E7	PB3		PCNT1_S0IN #1	US2_TX #1	
E8	PB4		PCNT1_S1IN #1	US2_RX #1	
E9	VSS	Ground.			
F1	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size $C^{DECOUPLE}$ is required at this pin.			
F2	PE2	BU_VOUT	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
F3	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
F4	PD7	ADC0_CH7 OPAMP_N1	TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
F5	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
F6	PA8		TIM2_CC0 #0		
F7	PC2	ACMP0_CH2 DAC0_OUT0ALT #2/ OPAMP_OUT0ALT	TIM0_CDTI0 #4	US2_TX #0	LES_CH2 #0

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
M11	AVSS_0	Analog ground 0.				
M12	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
M13	PD6	ADC0_CH6 OPAMP_P1		TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
N1	PB8	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
N2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
N3	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		
N4	PA11		EBI_HSNC #0/1/2			
N5	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
N6	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
N7	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
N8	AVSS_2	Analog ground 2.				
N9	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
N10	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
N11	AVDD_0	Analog power supply 0.				
N12	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
N13	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
92	PC14	2065.0	1558.7	ACMP1_CH6 DAC0_OUT1AL T #2/ OPAMP_OUT1 ALT		TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3 U0_TX #3	LES_CH14 #0
93	PF10	2065.0	1673.6				U1_TX #1 USB_DM	
94	PC15	2065.0	1756.6	ACMP1_CH7 DAC0_OUT1AL T #3/ OPAMP_OUT1 ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
95	PF11	2065.0	1870.0				U1_RX #1 USB_DP	
96	IOVSS_7	1846.0	2065.0	Digital IO ground 7.				
97	PF0	1739.3	2065.0			TIM0_CC0 #5 LETIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
98	PF1	1626.3	2065.0			TIM0_CC1 #5 LETIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU 3
99	PF2	1513.2	2065.0	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU 4
100	PF3	1389.7	2065.0	LCD_SEG1	EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
101	USB_VBUS	1242.9	2065.0	USB 5.0 V VBUS input.				
102	PF4	995.9	2065.0	LCD_SEG2	EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
103	PF12	886.3	2065.0				USB_ID	
104	PF5	782.2	2065.0	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
105	IOVSS_5	672.3	2065.0	Digital IO ground 5.				
106	IOVDD_5	576.7	2065.0	Digital IO power supply 5.				
107	PF6	488.4	2065.0	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
108	PF7	380.5	2065.0	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
109	PF8	275.3	2065.0	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
110	PF9	174.3	2065.0	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
111	NC	43.2	2065.0	Do not connect.				
112	PD9	-89.5	2065.0	LCD_SEG28	EBI_CS0 #0/1/2			
113	PD10	-204.5	2065.0	LCD_SEG29	EBI_CS1 #0/1/2			

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
114	PD11	-313.8	2065.0	LCD_SEG30	EBI_CS2 #0/1/2			
115	PD12	-426.2	2065.0	LCD_SEG31	EBI_CS3 #0/1/2			
116	PD13	-534.7	2065.0					ETM_TD1 #1
117	PD15	-644.6	2065.0					ETM_TD2 #1
118	PE8	-745.8	2065.0	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
119	PE9	-867.9	2065.0	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
120	PE10	-976.1	2065.0	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
121	PE11	-1085.3	2065.0	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
122	IOVDD_6	-1196.1	2065.0	Digital IO power supply 6.				
123	IOVSS_6	-1289.0	2065.0	Digital IO ground 6.				
124	PE12	-1385.4	2065.0	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
125	PE13	-1518.2	2065.0	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU 5
126	PE14	-1626.4	2065.0	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
127	PE15	-1729.6	2065.0	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
128	PA15	-1844.0	2065.0	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		

5.17.2 Alternate Functionality Padout

A wide selection of alternate functionality is available for multiplexing to various pads. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the padout is shown in the column corresponding to LOCATION 0.

Table 5.50. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.

9. LQFP100 Package Specifications

9.1 LQFP100 Package Dimensions

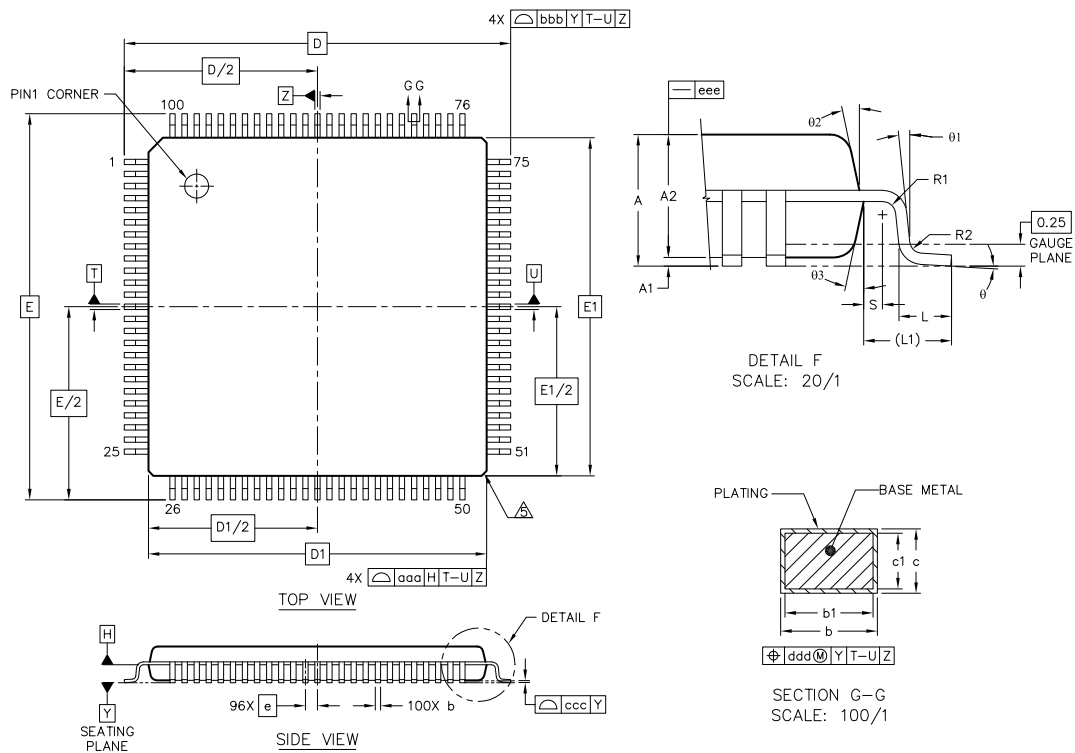


Figure 9.1. LQFP100

Note:

1. Datum 'T', 'U' and 'Z' to be determined at datum plane 'H'.
2. Datum 'D' and 'E' to be determined at seating plane datum 'Y'.
3. Dimension 'D1' and 'E1' do not include mold protrusions. Allowable protrusion is 0.25 per side. Dimensions 'D1' and 'E1' do include mold mismatch and are determined at datum plane datum 'H'.
4. Dimension 'b' does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum 'b' dimension by more than 0.08 mm. Dambar can not be located on the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.
5. Exact shape of each corner is optional.

Table 9.1. LQFP100 (Dimensions in mm)

	SYMBOL	MIN	NOM	MAX
total thickness	A	—	—	1.6
stand off	A1	0.05	—	0.15
mold thickness	A2	1.35	1.4	1.45
lead width (plating)	b	0.17	0.2	0.27
lead width	b1	0.17	—	0.23
L/F thickness (plating)	c	0.09	—	0.2

Symbol	Min	Nom	Max
e	0.50 BSC		
L	0.40	0.45	0.50
L1	0.00	—	0.10
aaa	0.10		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		

The QFN64 Package uses Nickel-Palladium-Gold preplated leadframe.

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.

14.8 Revision 1.00

This revision applies the following devices:

- EFM32LG230
- EFM32LG232
- EFM32LG280
- EFM32LG290
- EFM32LG295
- EFM32LG330
- EFM32LG332
- EFM32LG380
- EFM32LG390
- EFM32LG395
- EFM32LG840
- EFM32LG842
- EFM32LG880
- EFM32LG890
- EFM32LG895
- EFM32LG940
- EFM32LG942
- EFM32LG980
- EFM32LG990
- EFM32LG995

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

For BGA112 and BGA120 packages, corrected BGA solder balls material from Sn96.5/Ag3/Cu0.5 to SAC105.

This revision applies the following devices:

- EFM32LG360
- EFM32LG900

October 15th, 2014

Initial release.

14.9 Revision 0.92

May 25th, 2012

This revision applies the following devices:

- EFM32LG290
- EFM32LG295
- EFM32LG390
- EFM32LG395
- EFM32LG890
- EFM32LG895
- EFM32LG990
- EFM32LG995

Corrected BGA solder balls material description.

Corrected EM3 current consumption in the Electrical Characteristics section.