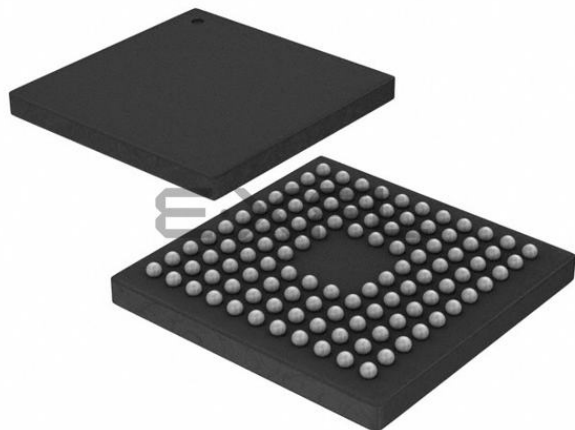




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	87
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	112-LFBGA
Supplier Device Package	112-BGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg990f256g-e-bga112r

2. Ordering Information

The following table shows the available EFM32LG devices.

Table 2.1. Ordering Information

Ordering Code	Flash (kB)	RAM (kB)	Max Speed (MHz)	Supply Voltage (V)	Temperature (°C)	Package
EFM32LG230F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG230F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG230F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG232F64G-E-QFP64	64	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG232F128G-E-QFP64	128	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG232F256G-E-QFP64	256	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG280F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG280F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG280F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG290F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG290F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG290F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG295F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG295F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG295F256G-E-BGA120	256	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG330F64G-E-QFN64	64	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG330F128G-E-QFN64	128	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG330F256G-E-QFN64	256	32	48	1.98 - 3.8	-40 - 85	QFN64
EFM32LG332F64G-E-QFP64	64	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG332F128G-E-QFP64	128	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG332F256G-E-QFP64	256	32	48	1.98 - 3.8	-40 - 85	TQFP64
EFM32LG360F64G-E-CSP81	64	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG360F128G-E-CSP81	128	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG360F256G-E-CSP81	256	32	48	1.98 - 3.8	-40 - 85	CSP81
EFM32LG380F64G-E-QFP100	64	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG380F128G-E-QFP100	128	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG380F256G-E-QFP100	256	32	48	1.98 - 3.8	-40 - 85	LQFP100
EFM32LG390F64G-E-BGA112	64	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG390F128G-E-BGA112	128	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG390F256G-E-BGA112	256	32	48	1.98 - 3.8	-40 - 85	BGA112
EFM32LG395F64G-E-BGA120	64	32	48	1.98 - 3.8	-40 - 85	BGA120
EFM32LG395F128G-E-BGA120	128	32	48	1.98 - 3.8	-40 - 85	BGA120

3.2.5 EFM32LG295

The features of the EFM32LG295 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.5. EFM32LG295 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
EBI	Full configuration	EBI_A[27:0], EBI_AD[15:0], EBI_ARDY, EBI_ALE, EBI_BL[1:0], EBI_CS[3:0], EBI_CSTFT, EBI_DCLK, EBI_DTEN, EBI_HSNCR, EBI_NANDREN, EBI_NANDWEN, EBI_REN, EBI_VSNCR, EBI_WEN
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
UART0	Full configuration	U0_TX, U0_RX
UART1	Full configuration	U1_TX, U1_RX
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O

Module	Configuration	Pin Connections
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	93 pins	Available pins are shown in 5.11.3 GPIO Pinout Overview

3.2.18 EFM32LG940

The features of the EFM32LG940 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.18. EFM32LG940 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
USB	Full configuration	USB_VBUS, USB_VBUSEN, USB_VREGI, USB_VREGO, USB_DM, USB_DMPU, USB_DP, USB_ID
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT

4.4 Current Consumption

Table 4.3. Current Consumption

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
EM0 current. No prescaling. Running prime number calculation code from Flash. (Production test condition = 14 MHz)	I_{EM0}	48 MHz HFXO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	211	225	$\mu\text{A}/\text{MHz}$
		48 MHz HFXO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	211	230	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	212	220	$\mu\text{A}/\text{MHz}$
		28 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	213	223	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	214	224	$\mu\text{A}/\text{MHz}$
		21 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	215	226	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	216	231	$\mu\text{A}/\text{MHz}$
		14 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	217	237	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	218	239	$\mu\text{A}/\text{MHz}$
		11 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	219	239	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	224	245	$\mu\text{A}/\text{MHz}$
		6.6 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	224	258	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 25^{\circ}\text{C}$	—	257	285	$\mu\text{A}/\text{MHz}$
		1.2 MHz HFRCO, all peripheral clocks disabled, $V_{DD} = 3.0\text{ V}$, $T_{AMB} = 85^{\circ}\text{C}$	—	261	293	$\mu\text{A}/\text{MHz}$

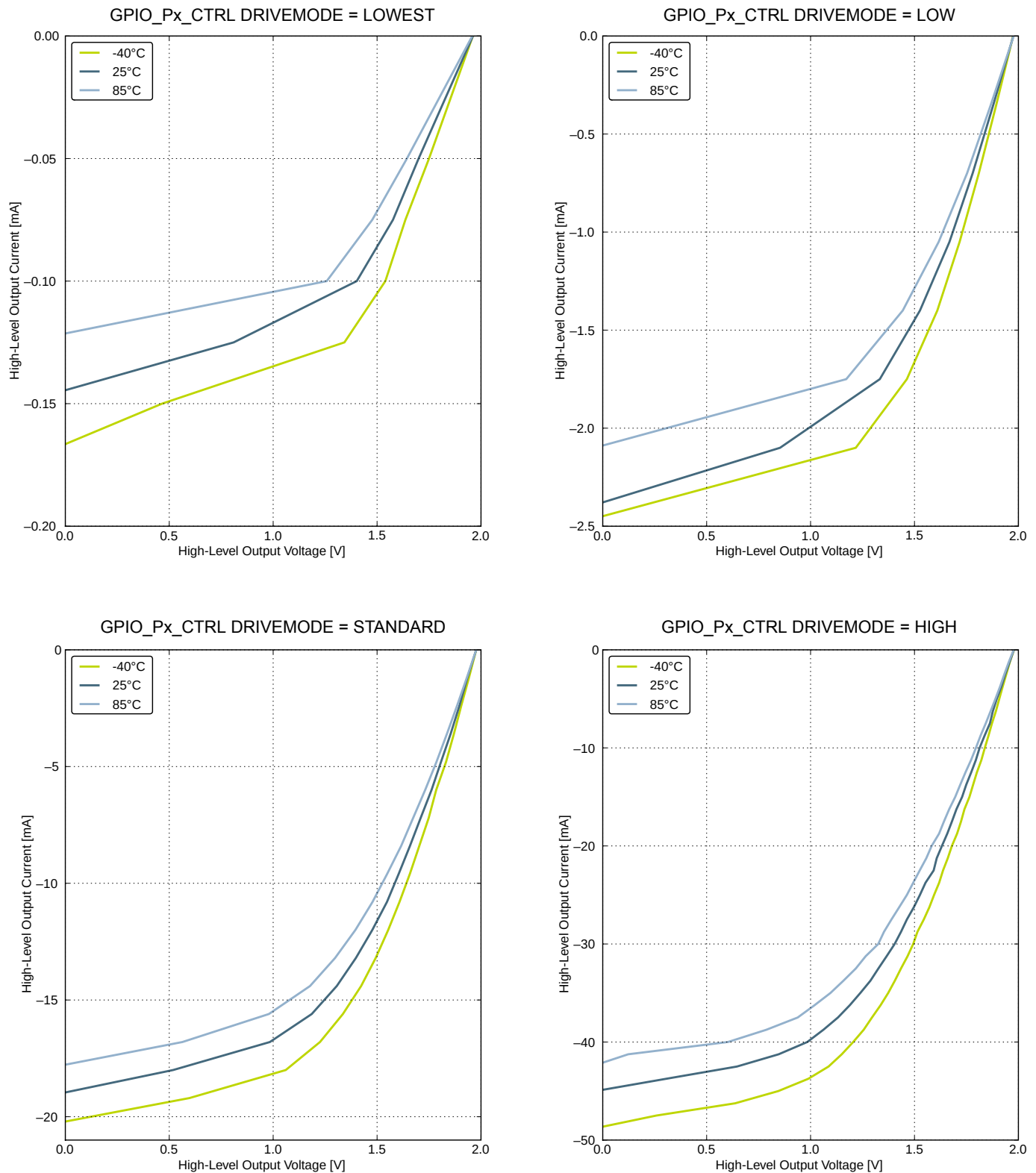


Figure 4.11. Typical High-Level Output Current, 2 V Supply Voltage

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
26	PA7		EBI_CSTFT #0/1/2			
27	PA8		EBI_DCLK #0/1/2	TIM2_CC0 #0		
28	PA9		EBI_DTEN #0/1/2	TIM2_CC1 #0		
29	PA10		EBI_VSNC #0/1/2	TIM2_CC2 #0		
30	PA11		EBI_HSNC #0/1/2			
31	IOVDD_2	Digital IO power supply 2.				
32	VSS	Ground.				
33	PA12		EBI_A00 #0/1/2	TIM2_CC0 #1		
34	PA13		EBI_A01 #0/1/2	TIM2_CC1 #1		
35	PA14		EBI_A02 #0/1/2	TIM2_CC2 #1		
36	RESETn	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
37	PB9		EBI_A03 #0/1/2		U1_TX #2	
38	PB10		EBI_A04 #0/1/2		U1_RX #2	
39	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
40	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
41	AVDD_1	Analog power supply 1.				
42	PB13	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
43	PB14	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
44	IOVDD_3	Digital IO power supply 3.				
45	AVDD_0	Analog power supply 0.				
46	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	
47	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT		TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
48	PD2	ADC0_CH2	EBI_A27 #0/1/2	TIM0_CC1 #3	USB_DMPU #0 US1_CLK #1	DBG_SWO #3
49	PD3	ADC0_CH3 OPAMP_N2		TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
50	PD4	ADC0_CH4 OPAMP_P2			LEU0_TX #0	ETM_TD2 #0/2
51	PD5	ADC0_CH5 OPAMP_OUT2 #0			LEU0_RX #0	ETM_TD3 #0/2

5.3.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.8. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH0	PC0							Analog comparator ACMP0, channel 0.
ACMP0_CH1	PC1							Analog comparator ACMP0, channel 1.
ACMP0_CH2	PC2							Analog comparator ACMP0, channel 2.
ACMP0_CH3	PC3							Analog comparator ACMP0, channel 3.
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13	PE2	PD6					Analog comparator ACMP0, digital output.
ACMP1_CH0	PC8							Analog comparator ACMP1, channel 0.
ACMP1_CH1	PC9							Analog comparator ACMP1, channel 1.
ACMP1_CH2	PC10							Analog comparator ACMP1, channel 2.
ACMP1_CH3	PC11							Analog comparator ACMP1, channel 3.
ACMP1_CH4	PC12							Analog comparator ACMP1, channel 4.
ACMP1_CH5	PC13							Analog comparator ACMP1, channel 5.
ACMP1_CH6	PC14							Analog comparator ACMP1, channel 6.
ACMP1_CH7	PC15							Analog comparator ACMP1, channel 7.
ACMP1_O	PF2	PE3	PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LES_CH13	PC13							LESENSE channel 13.
LES_CH14	PC14							LESENSE channel 14.
LES_CH15	PC15							LESENSE channel 15.
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13	PE0	PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14	PE1	PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
U0_RX	PF7	PE1	PA4					UART0 Receive input.
U0_TX	PF6	PE0	PA3					UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX		PF11	PB10	PE3				UART1 Receive input.
U1_TX		PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9		PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8		PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX	PC3	PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX	PC2	PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
L2	PC5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
L3	PA14	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
L6	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
L9	PB14	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	

BGA120 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
F11	PE7	LCD_COM3	EBI_A14 #0/1/2		US0_TX #1	
F12	PC8	ACMP1_CH0	EBI_A15 #0/1/2	TIM2_CC0 #2	US0_CS #2	LES_CH8 #0
F13	PC9	ACMP1_CH1	EBI_A09 #1/2	TIM2_CC1 #2	US0_CLK #2	LES_CH9 #0 GPIO_EM4WU2
G1	PB3	LCD_SEG20/ LCD_COM4	EBI_A19 #0/1/2	PCNT1_S0IN #1	US2_TX #1	
G2	PB4	LCD_SEG21/ LCD_COM5	EBI_A20 #0/1/2	PCNT1_S1IN #1	US2_RX #1	
G3	IOVDD_2	Digital IO power supply 2.				
G11	PE0		EBI_A07 #0/1/2	TIM3_CC0 #1 PCNT0_S0IN #1	U0_TX #1 I2C1_SDA #2	
G12	PE1		EBI_A08 #0/1/2	TIM3_CC1 #1 PCNT0_S1IN #1	U0_RX #1 I2C1_SCL #2	
G13	PE3	BU_STAT	EBI_A10 #0		U1_RX #3	ACMP1_O #1
H1	PB5	LCD_SEG22/ LCD_COM6	EBI_A21 #0/1/2		US2_CLK #1	
H2	PB6	LCD_SEG23/ LCD_COM7	EBI_A22 #0/1/2		US2_CS #1	
H3	VSS	Ground.				
H11	VDD_DREG	Power supply for on-chip voltage regulator.				
H12	PE2	BU_VOUT	EBI_A09 #0	TIM3_CC2 #1	U1_TX #3	ACMP0_O #1
H13	PC7	ACMP0_CH7	EBI_A06 #0/1/2		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
J1	PD14				I2C0_SDA #3	
J2	PD15				I2C0_SCL #3	
J3	VSS	Ground.				
J11	IOVDD_3	Digital IO power supply 3.				
J12	PC6	ACMP0_CH6	EBI_A05 #0/1/2		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
J13	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.				
K1	PC0	ACMP0_CH0 DAC0_OUT0ALT #0/ OPAMP_OUT0ALT	EBI_A23 #0/1/2	TIM0_CC1 #4 PCNT0_S0IN #2	US0_TX #5 US1_TX #0 I2C0_SDA #4	LES_CH0 #0 PRS_CH2 #0
K2	PC1	ACMP0_CH1 DAC0_OUT0ALT #1/ OPAMP_OUT0ALT	EBI_A24 #0/1/2	TIM0_CC2 #4 PCNT0_S1IN #2	US0_RX #5 US1_RX #0 I2C0_SCL #4	LES_CH1 #0 PRS_CH3 #0
K3	IOVDD_4	Digital IO power supply 4.				
K11	VSS	Ground.				
K12	VSS	Ground.				

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ETM_TD2	PD4	PB15	PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5	PF3	PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU2	PC9							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7	PD15	PC1	PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6	PD14	PC0	PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12	PE1					I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11	PE0					I2C1 Serial Data input / output.
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG1	PF3							LCD segment line 1. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG2	PF4							LCD segment line 2. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.

Water Pads and Coordinates				Pad Alternative Functionality / Description				
Pad #	Pad Name	X (μm)	Y (μm)	Analog	EBI	Timers	Communica- tion	Other
25	PC3	-2065.0	-1322.6	ACMP0_CH3 DAC0_OUT0ALT T #3/ OPAMP_OUT0 ALT	EBI_NANDREn #0/1/2	TIM0_CDTI1 #4	US2_RX #0	LES_CH3 #0
26	PC4	-2065.0	-1484.3	ACMP0_CH4 OPAMP_P0	EBI_A26 #0/1/2	TIM0_CDTI2 #4 LETIM0_OUT0 #3 PCNT1_S0IN #0	US2_CLK #0 I2C1_SDA #0	LES_CH4 #0
27	PC5	-2065.0	-1586.5	ACMP0_CH5 OPAMP_N0	EBI_NANDWEEn #0/1/2	LETIM0_OUT1 #3 PCNT1_S1IN #0	US2_CS #0 I2C1_SCL #0	LES_CH5 #0
28	PB7	-2065.0	-1708.6	LFXTAL_P		TIM1_CC0 #3	US0_TX #4 US1_CLK #0	
29	PB8	-2065.0	-1830.6	LFXTAL_N		TIM1_CC1 #3	US0_RX #4 US1_CS #0	
30	PA7	-1832.5	-2065.0	LCD_SEG35	EBI_CSTFT #0/1/2			
31	PA8	-1695.5	-2065.0	LCD_SEG36	EBI_DCLK #0/1/2	TIM2_CC0 #0		
32	PA9	-1558.5	-2065.0	LCD_SEG37	EBI_DTEN #0/1/2	TIM2_CC1 #0		
33	PA10	-1421.5	-2065.0	LCD_SEG38	EBI_VSNC #0/1/2	TIM2_CC2 #0		
34	PA11	-1284.5	-2065.0	LCD_SEG39	EBI_HSNC #0/1/2			
35	IOVDD_2	-1147.5	-2065.0	Digital IO power supply 2.				
36	IOVSS_2	-1027.4	-2065.0	Digital IO ground 2.				
37	PA12	-907.2	-2065.0	LCD_BCAP_P	EBI_A00 #0/1/2	TIM2_CC0 #1		
38	PA13	-780.6	-2065.0	LCD_BCAP_N	EBI_A01 #0/1/2	TIM2_CC1 #1		
39	PA14	-654.0	-2065.0	LCD_BEXT	EBI_A02 #0/1/2	TIM2_CC2 #1		
40	RESETn	-527.4	-2065.0	Reset input, active low. To apply an external reset source to this pin, it is required to only drive this pin low during reset, and let the internal pull-up ensure that reset is released.				
41	PB9	-401.0	-2065.0		EBI_A03 #0/1/2		U1_TX #2	
42	PB10	-274.5	-2065.0		EBI_A04 #0/1/2		U1_RX #2	
43	PB11	260.7	-2065.0	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LETIM0_OUT0 #1	I2C1_SDA #1	
44	PB12	366.0	-2065.0	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
45	AVSS_2	464.8	-2065.0	Analog ground 2.				
46	AVDD_2	560.5	-2065.0	Analog power supply 2.				

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
DAC0_OUT0ALT / OPAMP_OUT0ALT					PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 / OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1ALT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
ETM_TCLK	PD7		PC6	PA6				Embedded Trace Module ETM clock .
ETM_TD0	PD6		PC7	PA2				Embedded Trace Module ETM data 0.
ETM_TD1	PD3		PD3	PA3				Embedded Trace Module ETM data 1.
ETM_TD2	PD4		PD4	PA4				Embedded Trace Module ETM data 2.
ETM_TD3	PD5		PD5	PA5				Embedded Trace Module ETM data 3.
GPIO_EM4WU0	PA0							Pin can be used to wake the system up from EM4
GPIO_EM4WU1	PA6							Pin can be used to wake the system up from EM4
GPIO_EM4WU3	PF1							Pin can be used to wake the system up from EM4
GPIO_EM4WU4	PF2							Pin can be used to wake the system up from EM4
GPIO_EM4WU5	PE13							Pin can be used to wake the system up from EM4
HFX TAL_N	PB14							High Frequency Crystal negative pin. Also used as external optional clock input pin.
HFX TAL_P	PB13							High Frequency Crystal positive pin.
I2C0_SCL	PA1	PD7	PC7			PF1	PE13	I2C0 Serial Clock Line input / output.
I2C0_SDA	PA0	PD6	PC6			PF0	PE12	I2C0 Serial Data input / output.
I2C1_SCL	PC5	PB12						I2C1 Serial Clock Line input / output.
I2C1_SDA	PC4	PB11						I2C1 Serial Data input / output.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15							LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6							LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LCD_SEG24	PF6							LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG25	PF7							LCD segment line 25. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG26	PF8							LCD segment line 26. Segments 24, 25, 26 and 27 are controlled by SEGEN6.
LCD_SEG27	PF9							LCD segment line 27. Segments 24, 25, 26 and 27 are controlled by SEGEN6.

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
L8	PB13	HFXTAL_P			US0_CLK #4/5 LEU0_TX #1	
L9	PB14	HFXTAL_N			US0_CS #4/5 LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_A08	PE1	PE1	PE1					External Bus Interface (EBI) address output pin 08.
EBI_A09	PE2	PC9	PC9					External Bus Interface (EBI) address output pin 09.
EBI_A10	PE3	PC10	PC10					External Bus Interface (EBI) address output pin 10.
EBI_A11	PE4	PE4	PE4					External Bus Interface (EBI) address output pin 11.
EBI_A12	PE5	PE5	PE5					External Bus Interface (EBI) address output pin 12.
EBI_A13	PE6	PE6	PE6					External Bus Interface (EBI) address output pin 13.
EBI_A14	PE7	PE7	PE7					External Bus Interface (EBI) address output pin 14.
EBI_A15	PC8	PC8	PC8					External Bus Interface (EBI) address output pin 15.
EBI_A16	PB0	PB0	PB0					External Bus Interface (EBI) address output pin 16.
EBI_A17	PB1	PB1	PB1					External Bus Interface (EBI) address output pin 17.
EBI_A18	PB2	PB2	PB2					External Bus Interface (EBI) address output pin 18.
EBI_A19	PB3	PB3	PB3					External Bus Interface (EBI) address output pin 19.
EBI_A20	PB4	PB4	PB4					External Bus Interface (EBI) address output pin 20.
EBI_A21	PB5	PB5	PB5					External Bus Interface (EBI) address output pin 21.
EBI_A22	PB6	PB6	PB6					External Bus Interface (EBI) address output pin 22.
EBI_A23	PC0	PC0	PC0					External Bus Interface (EBI) address output pin 23.
EBI_A24	PC1	PC1	PC1					External Bus Interface (EBI) address output pin 24.
EBI_A25	PC2	PC2	PC2					External Bus Interface (EBI) address output pin 25.
EBI_A26	PC4	PC4	PC4					External Bus Interface (EBI) address output pin 26.
EBI_A27	PD2	PD2	PD2					External Bus Interface (EBI) address output pin 27.
EBI_AD00	PE8	PE8	PE8					External Bus Interface (EBI) address and data input / output pin 00.
EBI_AD01	PE9	PE9	PE9					External Bus Interface (EBI) address and data input / output pin 01.
EBI_AD02	PE10	PE10	PE10					External Bus Interface (EBI) address and data input / output pin 02.
EBI_AD03	PE11	PE11	PE11					External Bus Interface (EBI) address and data input / output pin 03.
EBI_AD04	PE12	PE12	PE12					External Bus Interface (EBI) address and data input / output pin 04.
EBI_AD05	PE13	PE13	PE13					External Bus Interface (EBI) address and data input / output pin 05.
EBI_AD06	PE14	PE14	PE14					External Bus Interface (EBI) address and data input / output pin 06.
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.

6.2 BGA112 PCB Layout

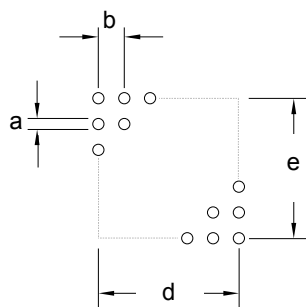


Figure 6.2. BGA112 PCB Land Pattern

Table 6.1. BGA112 PCB Land Pattern Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.35
b	0.80
d	8.00
e	8.00

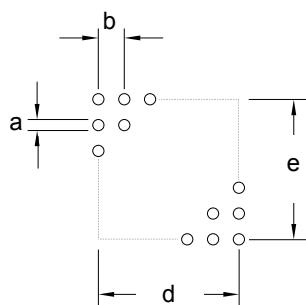


Figure 6.3. BGA112 PCB Solder Mask

Table 6.2. BGA112 PCB Solder Mask Dimensions (Dimensions in mm)

Symbol	Dim. (mm)
a	0.48
b	0.80
d	8.00
e	8.00

Symbol	Min	Nom	Max
A2	0.036	—	0.044
b	0.23	—	0.29
S	0.3075	0.31	0.3125
D	4.355 BSC.		
E	4.275 BSC.		
e	0.40 BSC.		
D1	3.20 BSC.		
E1	3.20 BSC.		
n	81		
aaa	0.05		
bbb	0.10		
ccc	0.075		
ddd	0.15		
eee	0.05		

All EFM32 packages are RoHS compliant and free of Bromine (Br) and Antimony (Sb).

For additional Quality and Environmental information, please see: <http://www.silabs.com/support/quality/pages/default.aspx>.