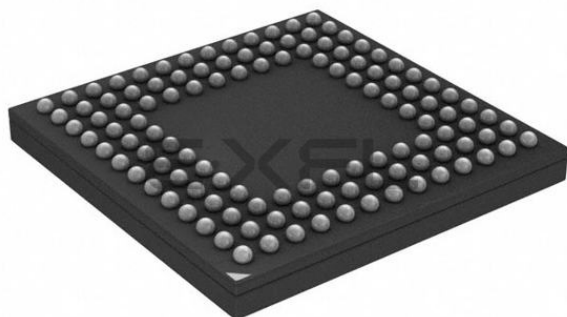




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Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M3
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	EBI/EMI, I ² C, IrDA, SmartCard, SPI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, POR, PWM, WDT
Number of I/O	93
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	120-VFBGA
Supplier Device Package	120-BGA (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32lg995f256g-e-bga120r

3.2.2 EFM32LG232

The features of the EFM32LG232 is a subset of the feature set described in the EFM32LG Reference Manual. The following table describes device specific implementation of the features.

Table 3.2. EFM32LG232 Configuration Summary

Module	Configuration	Pin Connections
Cortex-M3	Full configuration	NA
DBG	Full configuration	DBG_SWCLK, DBG_SWDIO, DBG_SWO
MSC	Full configuration	NA
DMA	Full configuration	NA
RMU	Full configuration	NA
EMU	Full configuration	NA
CMU	Full configuration	CMU_OUT0, CMU_OUT1
WDOG	Full configuration	NA
PRS	Full configuration	NA
I2C0	Full configuration	I2C0_SDA, I2C0_SCL
I2C1	Full configuration	I2C1_SDA, I2C1_SCL
USART0	Full configuration with IrDA	US0_TX, US0_RX, US0_CLK, US0_CS
USART1	Full configuration with I2S	US1_TX, US1_RX, US1_CLK, US1_CS
USART2	Full configuration with I2S	US2_TX, US2_RX, US2_CLK, US2_CS
LEUART0	Full configuration	LEU0_TX, LEU0_RX
LEUART1	Full configuration	LEU1_TX, LEU1_RX
TIMER0	Full configuration with DTI	TIM0_CC[2:0], TIM0_CDTI[2:0]
TIMER1	Full configuration	TIM1_CC[2:0]
TIMER2	Full configuration	TIM2_CC[2:0]
TIMER3	Full configuration	TIM3_CC[2:0]
RTC	Full configuration	NA
BURTC	Full configuration	NA
LETIMER0	Full configuration	LET0_O[1:0]
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx

Module	Configuration	Pin Connections
OPAMP	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	50 pins	Available pins are shown in 5.7.3 GPIO Pinout Overview

Table 4.27. I2C Fast-mode Plus (Fm+)

Parameter	Symbol	Min	Typ	Max	Unit
SCL clock frequency	f_{SCL}	0		1000 ¹	kHz
SCL clock low time	t_{LOW}	0.5			μs
SCL clock high time	t_{HIGH}	0.26			μs
SDA set-up time	$t_{SU,DAT}$	50			ns
SDA hold time	$t_{HD,DAT}$	8			ns
Repeated START condition set-up time	$t_{SU,STA}$	0.26			μs
(Repeated) START condition hold time	$t_{HD,STA}$	0.26			μs
STOP condition set-up time	$t_{SU,STO}$	0.26			μs
Bus free time between a STOP and a START condition	t_{BUF}	0.5			μs
Note: 1. For the minimum HPERCLK frequency required in Fast-mode Plus, see the I2C chapter in the EFM32LG Reference Manual.					

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
75	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT		TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3 U0_RX #3	LES_CH15 #0 DBG_SWO #1
76	PF0			TIM0_CC0 #5 LE- TIM0_OUT0 #2	US1_CLK #2 LEU0_TX #3 I2C0_SDA #5	DBG_SWCLK #0/1/2/3
77	PF1			TIM0_CC1 #5 LE- TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
78	PF2		EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
79	PF3		EBI_ALE #0	TIM0_CDTI0 #2/5		PRS_CH0 #1 ETM_TD3 #1
80	PF4		EBI_WEn #0/2	TIM0_CDTI1 #2/5		PRS_CH1 #1
81	PF5		EBI_REn #0/2	TIM0_CDTI2 #2/5		PRS_CH2 #1
82	IOVDD_5	Digital IO power supply 5.				
83	VSS	Ground.				
84	PF6		EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
85	PF7		EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
86	PF8		EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
87	PF9		EBI_REn #1			ETM_TD0 #1
88	PD9		EBI_CS0 #0/1/2			
89	PD10		EBI_CS1 #0/1/2			
90	PD11		EBI_CS2 #0/1/2			
91	PD12		EBI_CS3 #0/1/2			
92	PE8		EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
93	PE9		EBI_AD01 #0/1/2	PCNT2_S1IN #1		
94	PE10		EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
95	PE11		EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
96	PE12		EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
97	PE13		EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
98	PE14		EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
99	PE15		EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
100	PA15		EBI_AD08 #0/1/2	TIM3_CC2 #0		

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
L4	IOVDD_1	Digital IO power supply 1.				
L5	PB11	DAC0_OUT0 / OPAMP_OUT0		TIM1_CC2 #3 LE- TIM0_OUT0 #1	I2C1_SDA #1	
L6	PB12	DAC0_OUT1 / OPAMP_OUT1		LETIM0_OUT1 #1	I2C1_SCL #1	
L7	AVSS_2	Analog ground 2.				
L8	PB13	HFX TAL_P			US0_CLK #4/5 LEU0_TX #1	
L9	PB14	HFX TAL_N			US0_CS #4/5 LEU0_RX #1	
L10	AVDD_0	Analog power supply 0.				
L11	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1		PCNT2_S0IN #0	US1_TX #1	

5.7 EFM32LG332 (TQFP64)

5.7.1 Pinout

The EFM32LG332 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

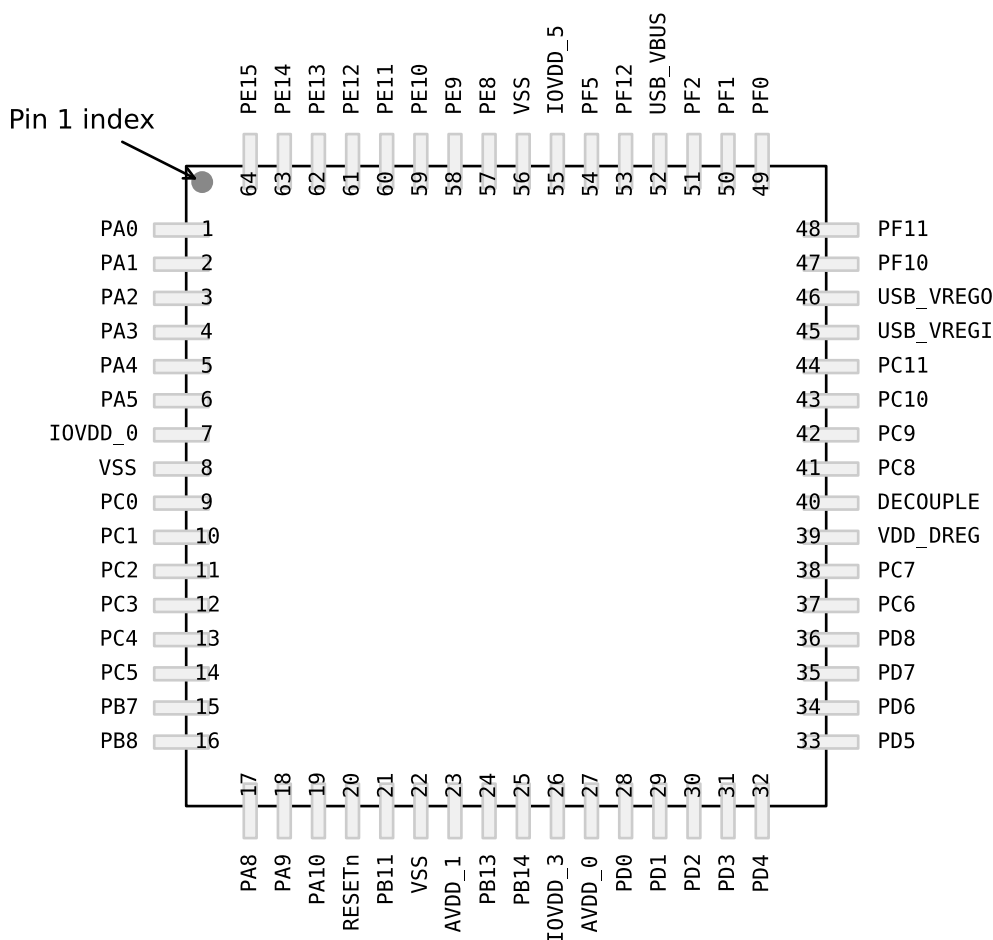


Figure 5.13. EFM32LG332 Pinout (top view, not to scale)

Table 5.19. Device Pinout

QFP64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
1	PA0		TIM0_CC0 #0/1/4	LEU0_RX #4 I2C0_SDA #0	PRS_CH0 #0 GPIO_EM4WU0
2	PA1		TIM0_CC1 #0/1	I2C0_SCL #0	CMU_CLK1 #0 PRS_CH1 #0

5.10 EFM32LG390 (BGA112)

5.10.1 Pinout

The EFM32LG390 pinout is shown in the following figure and table. Alternate locations are denoted by "#" followed by the location number (Multiple locations on the same pin are split with "/"). Alternate locations can be configured in the LOCATION bitfield in the *_ROUTE register in the module in question.

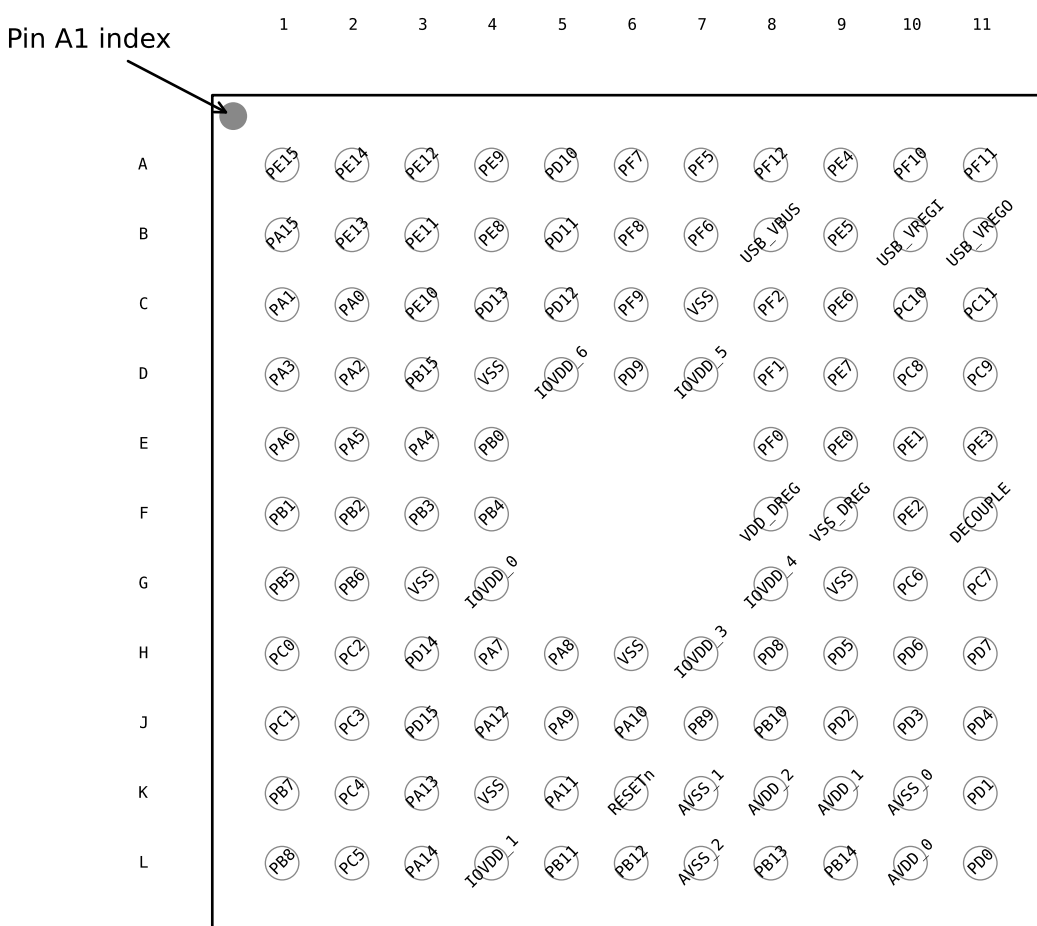


Figure 5.19. EFM32LG390 Pinout (top view, not to scale)

Table 5.28. Device Pinout

BGA112 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
A1	PE15		EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
A2	PE14		EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	

QFN64 Pin# and Name		Pin Alternate Functionality / Description			
Pin #	Pin Name	Analog	Timers	Communication	Other
27	AVDD_0	Analog power supply 0.			
28	PD0	ADC0_CH0 DAC0_OUT0ALT #4/ OPAMP_OUT0ALT OPAMP_OUT2 #1	PCNT2_S0IN #0	US1_TX #1	
29	PD1	ADC0_CH1 DAC0_OUT1ALT #4/ OPAMP_OUT1ALT	TIM0_CC0 #3 PCNT2_S1IN #0	US1_RX #1	DBG_SWO #2
30	PD2	ADC0_CH2	TIM0_CC1 #3	US1_CLK #1	DBG_SWO #3
31	PD3	ADC0_CH3 OPAMP_N2	TIM0_CC2 #3	US1_CS #1	ETM_TD1 #0/2
32	PD4	ADC0_CH4 OPAMP_P2		LEU0_TX #0	ETM_TD2 #0/2
33	PD5	ADC0_CH5 OPAMP_OUT2 #0		LEU0_RX #0	ETM_TD3 #0/2
34	PD6	ADC0_CH6 OPAMP_P1	TIM1_CC0 #4 LE- TIM0_OUT0 #0 PCNT0_S0IN #3	US1_RX #2 I2C0_SDA #1	LES_ALTEX0 #0 ACMP0_O #2 ETM_TD0 #0
35	PD7	ADC0_CH7 OPAMP_N1	TIM1_CC1 #4 LE- TIM0_OUT1 #0 PCNT0_S1IN #3	US1_TX #2 I2C0_SCL #1	CMU_CLK0 #2 LES_ALTEX1 #0 ACMP1_O #2 ETM_TCLK #0
36	PD8	BU_VIN			CMU_CLK1 #1
37	PC6	ACMP0_CH6		LEU1_TX #0 I2C0_SDA #2	LES_CH6 #0 ETM_TCLK #2
38	PC7	ACMP0_CH7		LEU1_RX #0 I2C0_SCL #2	LES_CH7 #0 ETM_TD0 #2
39	VDD_DREG	Power supply for on-chip voltage regulator.			
40	DECOUPLE	Decouple output for on-chip voltage regulator. An external capacitance of size C _{DECOUPLE} is required at this pin.			
41	PE4	LCD_COM0		US0_CS #1	
42	PE5	LCD_COM1		US0_CLK #1	
43	PE6	LCD_COM2		US0_RX #1	
44	PE7	LCD_COM3		US0_TX #1	
45	PC12	ACMP1_CH4 DAC0_OUT1ALT #0/ OPAMP_OUT1ALT			CMU_CLK0 #1 LES_CH12 #0
46	PC13	ACMP1_CH5 DAC0_OUT1ALT #1/ OPAMP_OUT1ALT	TIM0_CDTI0 #1/3 TIM1_CC0 #0 TIM1_CC2 #4 PCNT0_S0IN #0		LES_CH13 #0
47	PC14	ACMP1_CH6 DAC0_OUT1ALT #2/ OPAMP_OUT1ALT	TIM0_CDTI1 #1/3 TIM1_CC1 #0 PCNT0_S1IN #0	US0_CS #3	LES_CH14 #0
48	PC15	ACMP1_CH7 DAC0_OUT1ALT #3/ OPAMP_OUT1ALT	TIM0_CDTI2 #1/3 TIM1_CC2 #0	US0_CLK #3	LES_CH15 #0 DBG_SWO #1

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
EBI_AD07	PE15	PE15	PE15					External Bus Interface (EBI) address and data input / output pin 07.
EBI_AD08	PA15	PA15	PA15					External Bus Interface (EBI) address and data input / output pin 08.
EBI_AD09	PA0	PA0	PA0					External Bus Interface (EBI) address and data input / output pin 09.
EBI_AD10	PA1	PA1	PA1					External Bus Interface (EBI) address and data input / output pin 10.
EBI_AD11	PA2	PA2	PA2					External Bus Interface (EBI) address and data input / output pin 11.
EBI_AD12	PA3	PA3	PA3					External Bus Interface (EBI) address and data input / output pin 12.
EBI_AD13	PA4	PA4	PA4					External Bus Interface (EBI) address and data input / output pin 13.
EBI_AD14	PA5	PA5	PA5					External Bus Interface (EBI) address and data input / output pin 14.
EBI_AD15	PA6	PA6	PA6					External Bus Interface (EBI) address and data input / output pin 15.
EBI_ALE		PC11	PC11					External Bus Interface (EBI) Address Latch Enable output.
EBI_ARDY	PF2	PF2	PF2					External Bus Interface (EBI) Hardware Ready Control input.
EBI_BL0	PF6	PF6	PF6					External Bus Interface (EBI) Byte Lane/Enable pin 0.
EBI_BL1	PF7	PF7	PF7					External Bus Interface (EBI) Byte Lane/Enable pin 1.
EBI_CS0	PD9	PD9	PD9					External Bus Interface (EBI) Chip Select output 0.
EBI_CS1	PD10	PD10	PD10					External Bus Interface (EBI) Chip Select output 1.
EBI_CS2	PD11	PD11	PD11					External Bus Interface (EBI) Chip Select output 2.
EBI_CS3	PD12	PD12	PD12					External Bus Interface (EBI) Chip Select output 3.
EBI_CSTFT	PA7	PA7	PA7					External Bus Interface (EBI) Chip Select output TFT.
EBI_DCLK	PA8	PA8	PA8					External Bus Interface (EBI) TFT Dot Clock pin.
EBI_DTEN	PA9	PA9	PA9					External Bus Interface (EBI) TFT Data Enable pin.
EBI_HSNC	PA11	PA11	PA11					External Bus Interface (EBI) TFT Horizontal Synchronization pin.
EBI_NANDREn	PC3	PC3	PC3					External Bus Interface (EBI) NAND Read Enable output.
EBI_NANDWEn	PC5	PC5	PC5					External Bus Interface (EBI) NAND Write Enable output.
EBI_REn	PF5	PF9	PF5					External Bus Interface (EBI) Read Enable output.
EBI_VSNC	PA10	PA10	PA10					External Bus Interface (EBI) TFT Vertical Synchronization pin.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0	PF6	PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1	PF7	PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2	PF8	PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15				UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14				UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX	PC13		PB10	PE3				UART1 Receive input.
U1_TX	PC12		PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15							LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG15	PA2							LCD segment line 15. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG16	PA3							LCD segment line 16. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG17	PA4							LCD segment line 17. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG18	PA5							LCD segment line 18. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG19	PA6							LCD segment line 19. Segments 16, 17, 18 and 19 are controlled by SEGEN4.
LCD_SEG20/ LCD_COM4	PB3							LCD segment line 20. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 4
LCD_SEG21/ LCD_COM5	PB4							LCD segment line 21. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 5
LCD_SEG22/ LCD_COM6	PB5							LCD segment line 22. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 6
LCD_SEG23/ LCD_COM7	PB6							LCD segment line 23. Segments 20, 21, 22 and 23 are controlled by SEGEN5. This pin may also be used as LCD COM line 7
LCD_SEG24	PF6							LCD segment line 24. Segments 24, 25, 26 and 27 are controlled by SEGEN6.

5.18.2 Alternate Functionality Pinout

A wide selection of alternate functionality is available for multiplexing to various pins. This is shown in the following table. The table shows the name of the alternate functionality in the first column, followed by columns showing the possible LOCATION bitfield settings.

Note: Some functionality, such as analog interfaces, do not have alternate settings or a LOCATION bitfield. In these cases, the pinout is shown in the column corresponding to LOCATION 0.

Table 5.53. Alternate functionality overview

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
ACMP0_CH4	PC4							Analog comparator ACMP0, channel 4.
ACMP0_CH5	PC5							Analog comparator ACMP0, channel 5.
ACMP0_CH6	PC6							Analog comparator ACMP0, channel 6.
ACMP0_CH7	PC7							Analog comparator ACMP0, channel 7.
ACMP0_O	PE13		PD6					Analog comparator ACMP0, digital output.
ACMP1_O	PF2		PD7					Analog comparator ACMP1, digital output.
ADC0_CH0	PD0							Analog to digital converter ADC0, input channel number 0.
ADC0_CH1	PD1							Analog to digital converter ADC0, input channel number 1.
ADC0_CH2	PD2							Analog to digital converter ADC0, input channel number 2.
ADC0_CH3	PD3							Analog to digital converter ADC0, input channel number 3.
ADC0_CH4	PD4							Analog to digital converter ADC0, input channel number 4.
ADC0_CH5	PD5							Analog to digital converter ADC0, input channel number 5.
ADC0_CH6	PD6							Analog to digital converter ADC0, input channel number 6.
ADC0_CH7	PD7							Analog to digital converter ADC0, input channel number 7.
BOOT_RX	PE11							Bootloader RX.
BOOT_TX	PE10							Bootloader TX.
BU_VIN	PD8							Battery input for Backup Power Domain
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_BCAP_N	PA13							LCD voltage booster (optional), boost capacitor, negative pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BCAP_P	PA12							LCD voltage booster (optional), boost capacitor, positive pin. If using the LCD voltage booster, connect a 22 nF capacitor between LCD_BCAP_N and LCD_BCAP_P.
LCD_BEXT	PA14							LCD voltage booster (optional), boost output. If using the LCD voltage booster, connect a 1 uF capacitor between this pin and VSS. An external LCD voltage may also be applied to this pin if the booster is not enabled. If AVDD is used directly as the LCD supply voltage, this pin may be left unconnected or used as a GPIO.
LCD_COM0	PE4							LCD driver common line number 0.
LCD_COM1	PE5							LCD driver common line number 1.
LCD_COM2	PE6							LCD driver common line number 2.
LCD_COM3	PE7							LCD driver common line number 3.
LCD_SEG0	PF2							LCD segment line 0. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG3	PF5							LCD segment line 3. Segments 0, 1, 2 and 3 are controlled by SEGEN0.
LCD_SEG4	PE8							LCD segment line 4. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG5	PE9							LCD segment line 5. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG6	PE10							LCD segment line 6. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG7	PE11							LCD segment line 7. Segments 4, 5, 6 and 7 are controlled by SEGEN1.
LCD_SEG8	PE12							LCD segment line 8. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG9	PE13							LCD segment line 9. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG10	PE14							LCD segment line 10. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG11	PE15							LCD segment line 11. Segments 8, 9, 10 and 11 are controlled by SEGEN2.
LCD_SEG12	PA15							LCD segment line 12. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG13	PA0							LCD segment line 13. Segments 12, 13, 14 and 15 are controlled by SEGEN3.
LCD_SEG14	PA1							LCD segment line 14. Segments 12, 13, 14 and 15 are controlled by SEGEN3.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN				PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN				PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4	PB3						Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5	PB4						Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0							Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1							Peripheral Reflex System PRS, channel 1.
PRS_CH2		PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3		PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2		PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3		PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3							Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4							Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5		PF5		PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0		PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1		PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2		PE12		PB11				Timer 1 Capture Compare input / output channel 2.
TIM2_CC0		PA12						Timer 2 Capture Compare input / output channel 0.
TIM2_CC1		PA13						Timer 2 Capture Compare input / output channel 1.
TIM2_CC2		PA14						Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
US0_CLK	PE12	PE5			PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4			PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6		PE12	PB8			USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
US1_TX		PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.
US2_CS	PC5	PB6						USART2 chip select input / output.
US2_RX		PB4						USART2 Asynchronous Receive. USART2 Synchronous mode Master Input / Slave Output (MISO).
US2_TX		PB3						USART2 Asynchronous Transmit. Also used as receive input in half duplex communication. USART2 Synchronous mode Master Output / Slave Input (MOSI).
USB_DM	PF10							USB D- pin.
USB_DMPU	PD2							USB D- Pullup control.
USB_DP	PF11							USB D+ pin.
USB_ID	PF12							USB ID pin. Used in OTG mode.
USB_VBUS	USB_VBUS							USB 5 V VBUS input.
USB_VBUSEN	PF5							USB 5 V VBUS enable.
USB_VREGI	USB_VREGI							USB Input to internal 3.3 V regulator
USB_VREGO	USB_VREGO							USB Decoupling for internal 3.3 V USB regulator and regulator output

5.19.3 GPIO Pinout Overview

The specific GPIO pins available in EFM32LG942 is shown in the following table. Each GPIO port is organized as 16-bit ports indicated by letters A through F, and the individual pin on this port is indicated by a number from 15 down to 0.

Table 5.57. GPIO Pinout

Port	Pin 15	Pin 14	Pin 13	Pin 12	Pin 11	Pin 10	Pin 9	Pin 8	Pin 7	Pin 6	Pin 5	Pin 4	Pin 3	Pin 2	Pin 1	Pin 0
Port A	—	PA14	PA13	PA12	—	—	—	—	—	—	PA5	PA4	PA3	PA2	PA1	PA0
Port B	—	PB14	PB13	—	PB11	—	—	PB8	PB7	PB6	PB5	PB4	PB3	—	—	—
Port C	—	—	—	—	—	—	—	—	PC7	PC6	PC5	PC4	—	—	—	—
Port D	—	—	—	—	—	—	—	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
Port E	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8	PE7	PE6	PE5	PE4	—	—	—	—
Port F	—	—	—	PF12	PF11	PF10	—	—	—	—	PF5	—	—	PF2	PF1	PF0

LQFP100 Pin# and Name		Pin Alternate Functionality / Description				
Pin #	Pin Name	Analog	EBI	Timers	Communication	Other
77	PF1			TIM0_CC1 #5 LE- TIM0_OUT1 #2	US1_CS #2 LEU0_RX #3 I2C0_SCL #5	DBG_SWDIO #0/1/2/3 GPIO_EM4WU3
78	PF2	LCD_SEG0	EBI_ARDY #0/1/2	TIM0_CC2 #5	LEU0_TX #4	ACMP1_O #0 DBG_SWO #0 GPIO_EM4WU4
79	USB_VBUS	USB 5.0 V VBUS input.				
80	PF12				USB_ID	
81	PF5	LCD_SEG3	EBI_REn #0/2	TIM0_CDTI2 #2/5	USB_VBUSEN #0	PRS_CH2 #1
82	IOVDD_5	Digital IO power supply 5.				
83	VSS	Ground.				
84	PF6	LCD_SEG24	EBI_BL0 #0/1/2	TIM0_CC0 #2	U0_TX #0	
85	PF7	LCD_SEG25	EBI_BL1 #0/1/2	TIM0_CC1 #2	U0_RX #0	
86	PF8	LCD_SEG26	EBI_WEn #1	TIM0_CC2 #2		ETM_TCLK #1
87	PF9	LCD_SEG27	EBI_REn #1			ETM_TD0 #1
88	PD9	LCD_SEG28	EBI_CS0 #0/1/2			
89	PD10	LCD_SEG29	EBI_CS1 #0/1/2			
90	PD11	LCD_SEG30	EBI_CS2 #0/1/2			
91	PD12	LCD_SEG31	EBI_CS3 #0/1/2			
92	PE8	LCD_SEG4	EBI_AD00 #0/1/2	PCNT2_S0IN #1		PRS_CH3 #1
93	PE9	LCD_SEG5	EBI_AD01 #0/1/2	PCNT2_S1IN #1		
94	PE10	LCD_SEG6	EBI_AD02 #0/1/2	TIM1_CC0 #1	US0_TX #0	BOOT_TX
95	PE11	LCD_SEG7	EBI_AD03 #0/1/2	TIM1_CC1 #1	US0_RX #0	LES_ALTEX5 #0 BOOT_RX
96	PE12	LCD_SEG8	EBI_AD04 #0/1/2	TIM1_CC2 #1	US0_RX #3 US0_CLK #0 I2C0_SDA #6	CMU_CLK1 #2 LES_ALTEX6 #0
97	PE13	LCD_SEG9	EBI_AD05 #0/1/2		US0_TX #3 US0_CS #0 I2C0_SCL #6	LES_ALTEX7 #0 ACMP0_O #0 GPIO_EM4WU5
98	PE14	LCD_SEG10	EBI_AD06 #0/1/2	TIM3_CC0 #0	LEU0_TX #2	
99	PE15	LCD_SEG11	EBI_AD07 #0/1/2	TIM3_CC1 #0	LEU0_RX #2	
100	PA15	LCD_SEG12	EBI_AD08 #0/1/2	TIM3_CC2 #0		

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
BU_STAT	PE3							Backup Power Domain status, whether or not the system is in backup mode
BU_VIN	PD8							Battery input for Backup Power Domain
BU_VOUT	PE2							Power output for Backup Power Domain
CMU_CLK0	PA2		PD7					Clock Management Unit, clock output number 0.
CMU_CLK1	PA1	PD8	PE12					Clock Management Unit, clock output number 1.
OPAMP_N0	PC5							Operational Amplifier 0 external negative input.
OPAMP_N1	PD7							Operational Amplifier 1 external negative input.
OPAMP_N2	PD3							Operational Amplifier 2 external negative input.
DAC0_OUT0 / OPAMP_OUT0	PB11							Digital to Analog Converter DAC0_OUT0 /OPAMP output channel number 0.
DAC0_OUT0ALT / OPAMP_OUT0A LT	PC0	PC1	PC2	PC3	PD0			Digital to Analog Converter DAC0_OUT0ALT / OPAMP alternative output for channel 0.
DAC0_OUT1 / OPAMP_OUT1	PB12							Digital to Analog Converter DAC0_OUT1 /OPAMP output channel number 1.
DAC0_OUT1ALT / OPAMP_OUT1A LT					PD1			Digital to Analog Converter DAC0_OUT1ALT / OPAMP alternative output for channel 1.
OPAMP_OUT2	PD5	PD0						Operational Amplifier 2 output.
OPAMP_P0	PC4							Operational Amplifier 0 external positive input.
OPAMP_P1	PD6							Operational Amplifier 1 external positive input.
OPAMP_P2	PD4							Operational Amplifier 2 external positive input.
DBG_SWCLK	PF0	PF0	PF0	PF0				Debug-interface Serial Wire clock input. Note that this function is enabled to pin out of reset, and has a built-in pull down.
DBG_SWDIO	PF1	PF1	PF1	PF1				Debug-interface Serial Wire data input / output. Note that this function is enabled to pin out of reset, and has a built-in pull up.
DBG_SWO	PF2		PD1	PD2				Debug-interface Serial Wire viewer Output. Note that this function is not enabled after reset, and must be enabled by software to be used.
EBI_A00	PA12	PA12	PA12					External Bus Interface (EBI) address output pin 00.
EBI_A01	PA13	PA13	PA13					External Bus Interface (EBI) address output pin 01.
EBI_A02	PA14	PA14	PA14					External Bus Interface (EBI) address output pin 02.
EBI_A03	PB9	PB9	PB9					External Bus Interface (EBI) address output pin 03.
EBI_A04	PB10	PB10	PB10					External Bus Interface (EBI) address output pin 04.
EBI_A05	PC6	PC6	PC6					External Bus Interface (EBI) address output pin 05.
EBI_A06	PC7	PC7	PC7					External Bus Interface (EBI) address output pin 06.
EBI_A07	PE0	PE0	PE0					External Bus Interface (EBI) address output pin 07.

Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LCD_SEG28	PD9							LCD segment line 28. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG29	PD10							LCD segment line 29. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG30	PD11							LCD segment line 30. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG31	PD12							LCD segment line 31. Segments 28, 29, 30 and 31 are controlled by SEGEN7.
LCD_SEG32	PB0							LCD segment line 32. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG33	PB1							LCD segment line 33. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG34	PB2							LCD segment line 34. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG35	PA7							LCD segment line 35. Segments 32, 33, 34 and 35 are controlled by SEGEN8.
LCD_SEG36	PA8							LCD segment line 36. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG37	PA9							LCD segment line 37. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG38	PA10							LCD segment line 38. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LCD_SEG39	PA11							LCD segment line 39. Segments 36, 37, 38 and 39 are controlled by SEGEN9.
LES_ALTEX0	PD6							LESENSE alternate exite output 0.
LES_ALTEX1	PD7							LESENSE alternate exite output 1.
LES_ALTEX2	PA3							LESENSE alternate exite output 2.
LES_ALTEX3	PA4							LESENSE alternate exite output 3.
LES_ALTEX4	PA5							LESENSE alternate exite output 4.
LES_ALTEX5	PE11							LESENSE alternate exite output 5.
LES_ALTEX6	PE12							LESENSE alternate exite output 6.
LES_ALTEX7	PE13							LESENSE alternate exite output 7.
LES_CH0	PC0							LESENSE channel 0.
LES_CH1	PC1							LESENSE channel 1.
LES_CH2	PC2							LESENSE channel 2.
LES_CH3	PC3							LESENSE channel 3.
LES_CH4	PC4							LESENSE channel 4.
LES_CH5	PC5							LESENSE channel 5.
LES_CH6	PC6							LESENSE channel 6.
LES_CH7	PC7							LESENSE channel 7.
LES_CH8	PC8							LESENSE channel 8.

Alternate	LOCATION							Description
Functionality	0	1	2	3	4	5	6	
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10	PB0	PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11	PB1	PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12	PB2	PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8	PA12	PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9	PA13	PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10	PA14	PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14	PE0						Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15	PE1						Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15	PE2						Timer 3 Capture Compare input / output channel 2.
U0_RX	PF7	PE1	PA4	PC15				UART0 Receive input.
U0_TX	PF6	PE0	PA3	PC14				UART0 Transmit output. Also used as receive input in half duplex communication.
U1_RX	PC13	PF11	PB10	PE3				UART1 Receive input.
U1_TX	PC12	PF10	PB9	PE2				UART1 Transmit output. Also used as receive input in half duplex communication.
US0_CLK	PE12	PE5	PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13	PE4	PC8	PC14	PB14	PB14		USART0 chip select input / output.
US0_RX	PE11	PE6	PC10	PE12	PB8	PC1		USART0 Asynchronous Receive. USART0 Synchronous mode Master Input / Slave Output (MISO).
US0_TX	PE10	PE7	PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit. Also used as receive input in half duplex communication. USART0 Synchronous mode Master Output / Slave Input (MOSI).
US1_CLK	PB7	PD2	PF0					USART1 clock input / output.
US1_CS	PB8	PD3	PF1					USART1 chip select input / output.
US1_RX	PC1	PD1	PD6					USART1 Asynchronous Receive. USART1 Synchronous mode Master Input / Slave Output (MISO).
US1_TX	PC0	PD0	PD7					USART1 Asynchronous Transmit. Also used as receive input in half duplex communication. USART1 Synchronous mode Master Output / Slave Input (MOSI).
US2_CLK	PC4	PB5						USART2 clock input / output.

5.22.4 Opamp Pinout Overview

The specific opamp terminals available in EFM32LG995 is shown in the following figure.

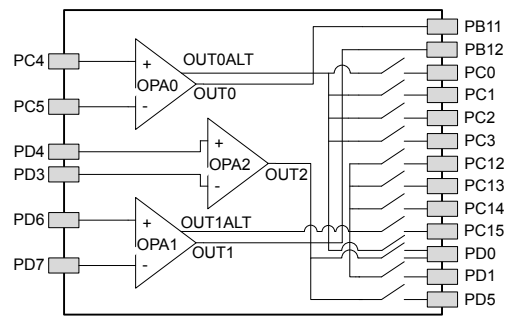


Figure 5.44. Opamp Pinout