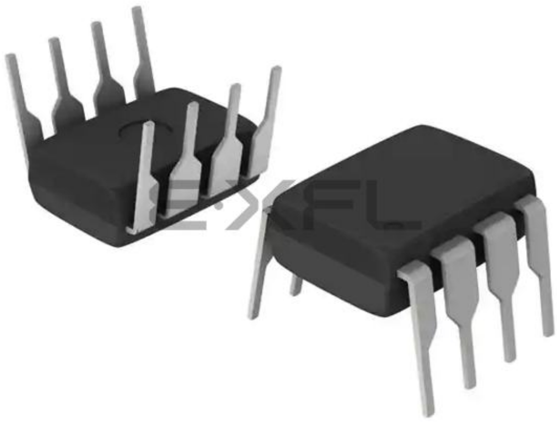

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Applications of "Embedded - Microcontrollers"

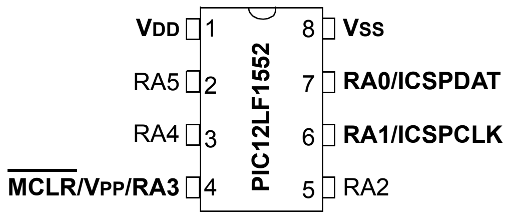
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	8-DIP (0.300", 7.62mm)
Supplier Device Package	8-PDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1552-e-p

2.0 DEVICE PINOUTS

The pin diagram is shown in Figure 2-1. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagram.

FIGURE 2-1: 8-PIN PDIP, SOIC, MSOP, DFN DIAGRAM FOR PIC12LF1552

PDIP, SOIC, MSOP, DFN (2x3)



 Preliminary

3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 8000h-8003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note:	MPLAB® IDE only displays the seven Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the seven LSbs be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word is located at 8006h. This location is read-only and cannot be erased or modified.

REGISTER 3-1: DEVICE ID: DEVICE ID REGISTER(1)

R	R	R	R	R	R
DEV8	DEV7	DEV6	DEV5	DEV4	DEV3
bit 13					bit 8

R	R	R	R	R	R	R	R
DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0
bit 7							bit 0

Legend:		
R = Readable bit	‘1’ = Bit is set	‘0’ = Bit is cleared

bit 13-5 **DEV<8:0>:** Device ID bits
These bits are used to identify the part number.

bit 4-0 **REV<4:0>:** Revision ID bits
These bits are used to identify the revision.

Note 1: This location cannot be written.

TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC12LF1552	0010 1011 110	x xxxx

3.3 Configuration Words

There are two Configuration Words, Configuration Word 1 (8007h) and Configuration Word 2 (8008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

The internal calibration values are factory calibrated and stored in Calibration Words 1 and 2 (8009h, 800Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-2: CONFIGURATION WORD 1

U-1	U-1	R/P-1	R/P-1	R/P-1	U-1(3)
—	—	$\overline{\text{CLKOUTEN}}$	BOREN<1:0>		—
bit 13					bit 8

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	U-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE<1:0>		—	FOSC<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 13-12 **Unimplemented:** Read as '1'

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits[(1)]
When enabled, Brown-out Reset Voltage (V_{BOR}) is set by the BORV bit of the Configuration Word 2 register.
11 = Brown-out Reset enabled. SPBOREN bit is ignored.
10 = Brown-out Reset enabled while running and disabled in Sleep. SBOREN bit is ignored.
01 = Brown-out Reset controlled by the SBOREN bit in the BORCON register
00 = Brown-out Reset disabled. SBOREN bit is ignored

bit 8[(3)] **Unimplemented:** Read as '1'

bit 7 **$\overline{\text{CP}}$:** Code Protection bit[(2)]
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/VPP Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = $\overline{\text{MCLR}}$/VPP pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUA register.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit[(1)]
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled. SWDTEN is ignored.
10 = WDT enabled while running and disabled in Sleep. SWDTEN is ignored.
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled. SWDTEN is ignored.

bit 2 **Unimplemented:** Read as '1'

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
11 = ECH: External Clock, High-Power mode: on CLKIN pin
10 = ECM: External Clock, Medium-Power mode: on CLKIN pin
01 = ECL: External Clock, Low-Power mode: on CLKIN pin
00 = INTOSC oscillator: I/O function on OSC1 pin

Note 1: Enabling Brown-out Reset does not automatically enable Power-up Timer.
2: The entire program memory will be erased when the code protection is turned off.
3: This bit should be maintained as '1' when programmed.

REGISTER 3-3: CONFIGURATION WORD 2

R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1
LVP	—	$\overline{\text{LPBOR}}$	BORV	STVREN	—
bit 13					bit 8

U-1	U-1	U-1	U-1	U-1	U-1	R/P-1	R/P-1
—	—	—	—	—	—	WRT<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as ‘1’
‘0’ = Bit is cleared	‘1’ = Bit is set	-n = Value when blank or after Bulk Erase

bit 13 **LVP:** Low-Voltage Programming Enable bit(1)
1 = Low-voltage programming enabled. $\overline{\text{MCLR}}$/VPP pin function is $\overline{\text{MCLR}}$. MCLRE Configuration bit is ignored.
0 = HV on $\overline{\text{MCLR}}$/VPP must be used for programming.

bit 12 **Unimplemented:** Read as ‘1’

bit 11 **$\overline{\text{LPBOR}}$:** Low-Power BOR bit
1 = Low-Power BOR is disabled
0 = Low-Power BOR is enabled

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
1 = Brown-out Reset Voltage (VBOR) set to 1.9V
0 = Brown-out Reset Voltage (VBOR) set to 2.7V

bit 9 **STVREN:** Stack Overflow/Underflow Reset Enable bit
1 = Stack Overflow or Underflow will cause a Reset
0 = Stack Overflow or Underflow will not cause a Reset

bit 8-2 Unimplemented: Read as ‘1’

bit 1-0 WRT<1:0>: Flash Memory Self-Write Protection bits
11 = Write protection off
10 = 000h to 1FFh write-protected, 200h to 7FFh may be modified by PMCON control
01 = 000h to 3FFh write-protected, 400h to 7FFh may be modified by PMCON control
00 = 000h to 7FFh write-protected, no addresses may be modified by PMCON control

Note 1: The LVP bit cannot be programmed to ‘0’ when Programming mode is entered via LVP.

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/ Verify mode via high voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{MCLR}$ from 0V to VIHH.
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, the device will execute code when Configuration Word 1 has $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer is disabled ($\overline{PWRTE}$ = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{MCLR}$ to VDD or lower (VIL). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the device to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{MCLR}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{MCLR}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{MCLR}$ to VIL. See Figure 8-8 and Figure 8-9.

Note:	To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3 Program/Verify Commands

The device implements ten programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

4.3.1 LOAD CONFIGURATION

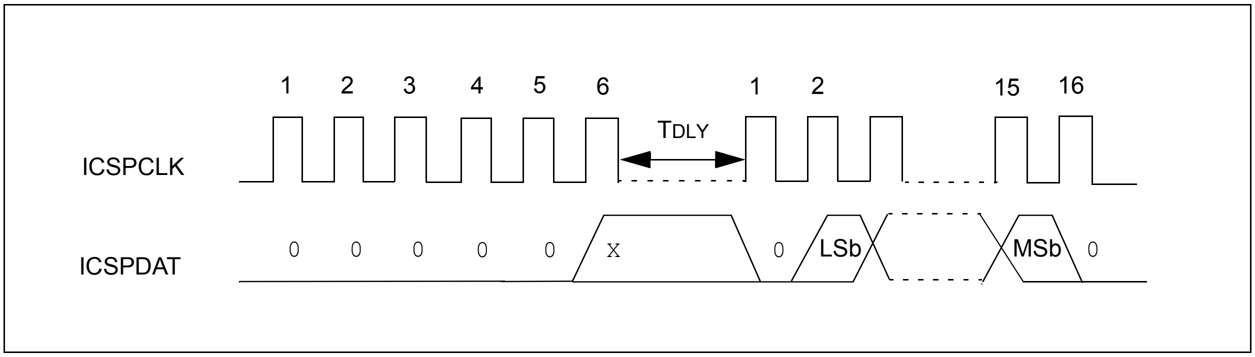
The Load Configuration command is used to access the configuration memory (user ID locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

Note:	Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

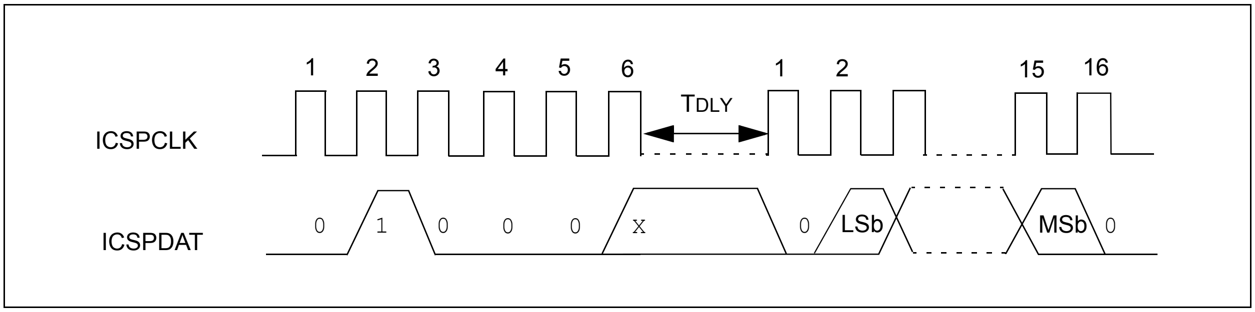
FIGURE 4-1: LOAD CONFIGURATION



4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

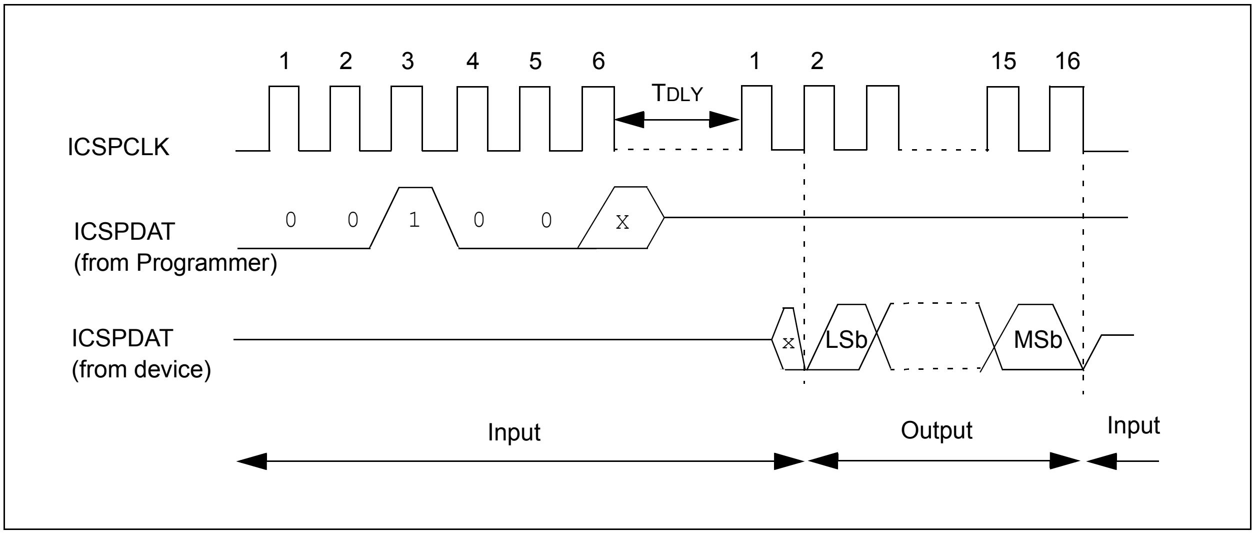
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

FIGURE 4-3: READ DATA FROM PROGRAM MEMORY

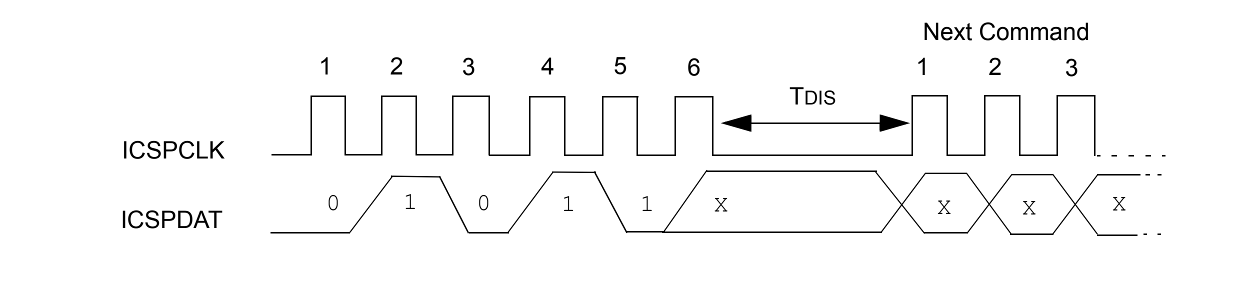


4.3.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by TPEXT, after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (TDIS) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands (see Figure 4-8).

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING



4.3.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions dependent on the current state of the address.

Address 0000h-7FFFh:

Program Memory is erased

Configuration Words are erased

Address 8000h-8008h:

Program Memory is erased

Configuration Words are erased

User ID Locations are erased

A Bulk Erase Program Memory command should not be issued when the address is greater than 8008h.

After receiving the Bulk Erase Program Memory command, the erase will not complete until the time interval, TERAB, has expired.

Note:	The code protection Configuration bit ($\overline{CP}$) has no effect on the Bulk Erase Program Memory command.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY

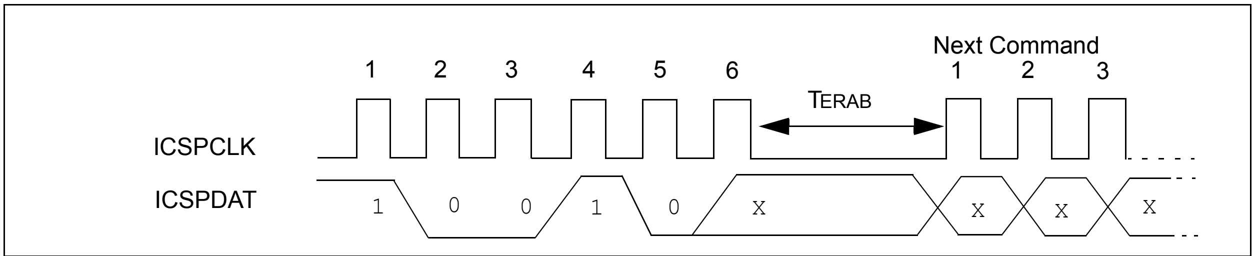
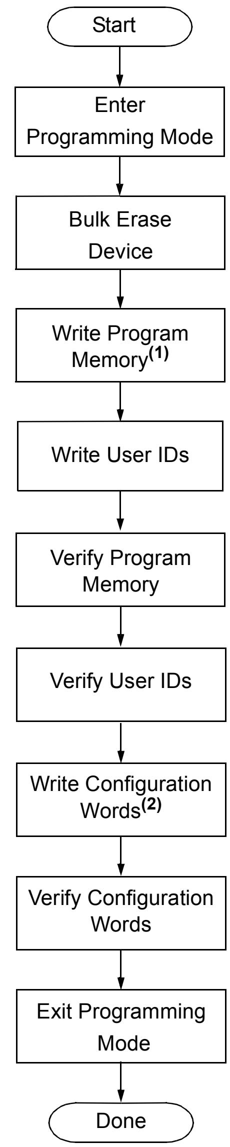
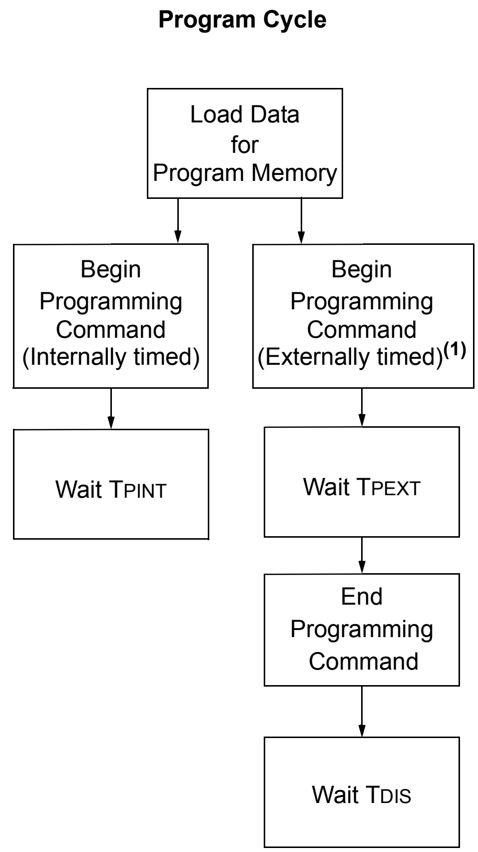


FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See Figure 5-2.
2: See Figure 5-5.

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

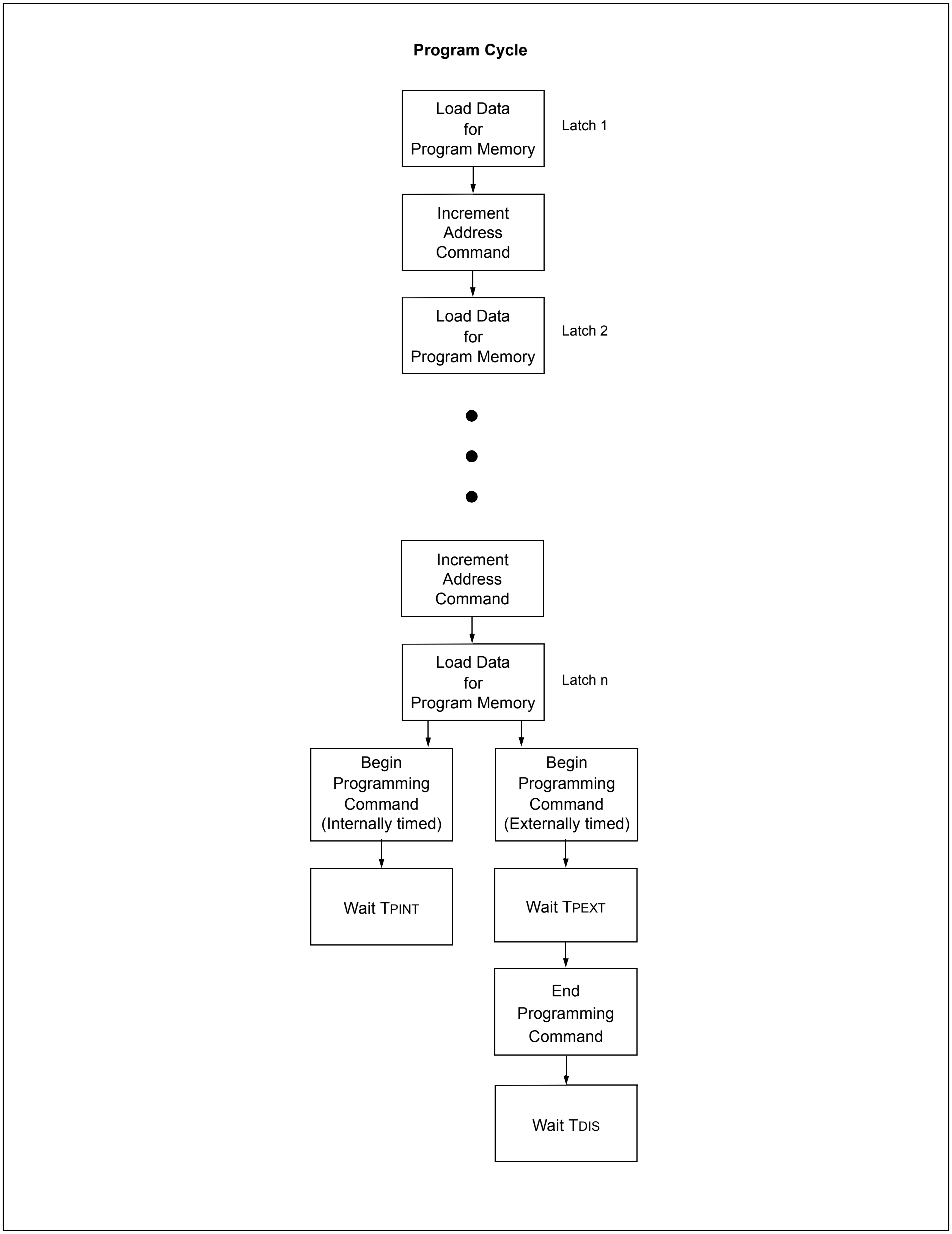
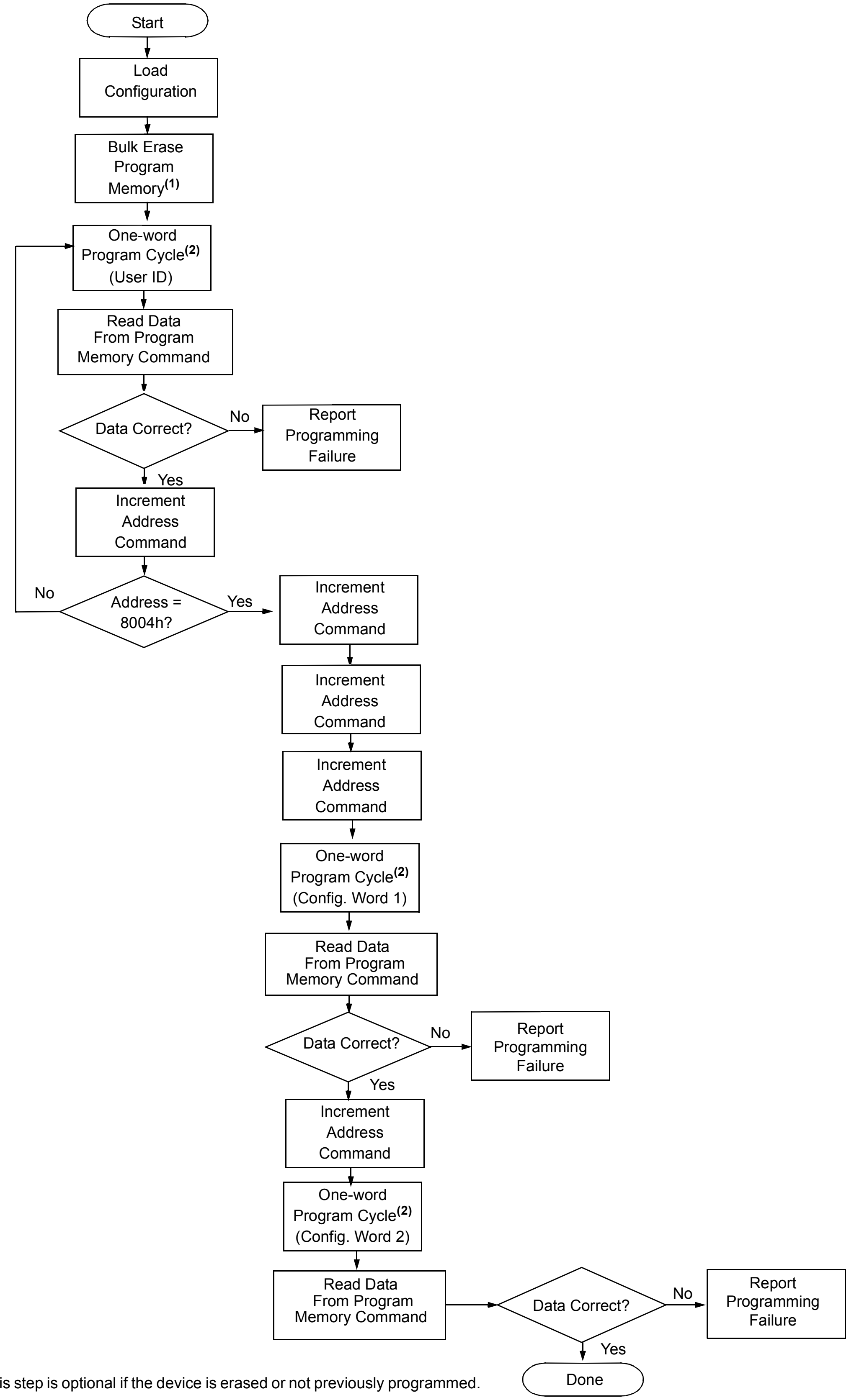


FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if the device is erased or not previously programmed.
2: See Figure 5-3.

6.0 CODE PROTECTION

Code protection is controlled using the $\overline{CP}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-7FFFh) read as '0'. Further programming is disabled for the program memory (0000h-7FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Program Memory

Code protection is enabled by programming the $\overline{CP}$ bit in Configuration Word 1 register to '0'.

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INHX32 hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: Configuration Word 1 is stored at 8007h. In the hex file this will be referenced as 1000Eh-1000Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 1000Ch-1000Dh (8006h on the part), the programmer should verify the device ID (excluding the revision) against the value read from the part. On a mismatch condition the programmer should generate a warning message.

7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{CP}$ Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC12LF1552	0EFBh	2E03h

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

EXAMPLE 7-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED ($\overline{CP}$ = 1), PIC12LF1552, 00AAh AT FIRST AND LAST ADDRESS

PIC12LF1552	Sum of Memory addresses 0000h-07FFh	7956h(1)
	Configuration Word 1	3FFFh(2)
	Configuration Word 1 mask	0EFBh(3)
	Configuration Word 2	3FFFh(4)
	Configuration Word 2 mask	2E03h(5)

Checksum = 7956h + (3FFFh and 0EFBh) + (3FFFh and 2E03h)(6)
= 7956h + 0EFBh + 2E03h
= B654h

Note 1: This value is obtained by taking the total number of program memory locations (0x000 to 0x7FFh which is 800h) subtracting 2h which yields 7FEh, then multiplying it by the blank memory value of 0x3FFF to get the sum of 1FF 7802h. Then, truncate to 16 bits the value of 7802h. Now add 00AAh (00AAh + 00AAh) to 7802h to get the final value of B654h.

2: This value is obtained by making all bits of the Configuration Word 1 a '1', then converting it to hex, thus having a value of 3FFFh.

3: This value is obtained by making all used bits of the Configuration Word 1 a '1', then converting it to hex, thus having a value of 0EFBh.

4: This value is obtained by making all bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 3FFFh.

5: This value is obtained by making all used bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 2E03h.

6: This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of memory addresses: (3FFFh and 0EFBh) + (3FFFh and 2E03h) + 7956h = B654h. Then, truncate to 16 bits, thus having a final value of B654h.

7.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED ($\overline{CP}$ = 0), PIC12LF1552, 00AAh AT FIRST AND LAST ADDRESS

PIC12LF1552	Configuration Word 1	3F7Fh(1)
	Configuration Word 1 mask	0E7Bh(2)
	Configuration Word 2	3FFFh(3)
	Configuration Word 2 mask	2E03h(4)
	User ID (8000h)	000Eh(5)
	User ID (8001h)	0008h(5)
	User ID (8002h)	0005h(5)
	User ID (8003h)	0008h(5)

Sum of User IDs = (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 + (0005h and 000Fh) << 4 + (0008h and 000Fh)(6)
= E000h + 0800h + 0050h + 0008h
= E858h

Checksum = (3F7Fh and 0E7Bh) + (3FFFh and 2E03h) + Sum of User IDs(7)
= 0E7Bh +2E03h + E858h
= 24D6h

Note 1: This value is obtained by making all bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 3F7Fh.

2: This value is obtained by making all used bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 0E7Bh.

3: This value is obtained by making all bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 3FFFh.

4: This value is obtained by making all used bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 2E03h.

5: These values are picked at random for this example; they could be any 16-bit value.

6: In order to calculate the sum of user IDs, take the 16-bit value of the first user ID location (000Eh), AND the address to (000Fh), thus masking the MSB. This gives you the value 000Eh, then shift left 12 bits, giving you E000h. Do the same procedure for the 16-bit value of the second user ID location (0008h), except shift left 8 bits. Also, do the same for the third user ID location (0005h), except shift left 4 bits. For the fourth user ID location do not shift. Finally, add up all four user ID values to get the final sum of user IDs of E858h.

7: This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of user IDs: (3F7Fh AND 0E7Bh) + (3FFFh AND 2E03h) + E858h = 24D6h.

8.0 ELECTRICAL SPECIFICATIONS

Refer to the device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
Supply Voltages and Currents						
VDD	**VDD**					
	Read/Write and Row Erase operations	VDDMIN	—	VDDMAX	V	
	Bulk Erase operations	2.7	—	VDDMAX	V	
IDDI	Current on VDD, Idle	—	—	1.0	mA	
IDDP	Current on VDD, Programming	—	—	3.0	mA	
	VPP					
IPP	Current on $\overline{\text{MCLR}}$/VPP	—	—	600	μA	
VIHH	High voltage on $\overline{\text{MCLR}}$/VPP for Program/Verify mode entry	8.0	—	9.0	V	
TVHHR	$\overline{\text{MCLR}}$ rise time (VIL to VIHH) for Program/Verify mode entry	—	—	1.0	μs	
	I/O pins					
VIH	(ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}$/VPP) input high level	0.8 VDD	—	—	V	
VIL	(ICSPCLK, ICSPDAT, $\overline{\text{MCLR}}$/VPP) input low level	—	—	0.2 VDD	V	
VOH	ICSPDAT output high level	VDD-0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 2 mA, VDD = 1.8V
VOL	ICSPDAT output low level	—	—	0.6	V	IOH = 8 mA, VDD = 5V IOH = 6 mA, VDD = 3.3V IOH = 3 mA, VDD = 1.8V
Programming Mode Entry and Exit						
TENTS	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or $\overline{\text{MCLR}}$↑	100	—	—	ns	
TENTH	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or $\overline{\text{MCLR}}$↑	250	—	—	μs	
Serial Program/Verify						
TCKL	Clock Low Pulse Width	100	—	—	ns	
TCKH	Clock High Pulse Width	100	—	—	ns	
TDS	Data in setup time before clock↓	100	—	—	ns	
TDH	Data in hold time after clock↓	100	—	—	ns	
TCO	Clock↑ to data out valid (during a Read Data command)	0	—	80	ns	
TLZD	Clock↓ to data low-impedance (during a Read Data command)	0	—	80	ns	
THZD	Clock↓ to data high-impedance (during a Read Data command)	0	—	80	ns	
TDLY	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	μs	
TERAB	Bulk Erase cycle time	—	—	5	ms	
TERAR	Row Erase cycle time	—	—	2.5	ms	
TPINT	Internally timed programming operation time	— —	— —	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	**Note 1**
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	μs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	μs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

8.1 AC Timing Diagrams

FIGURE 8-1: PROGRAMMING MODE ENTRY – VDD FIRST

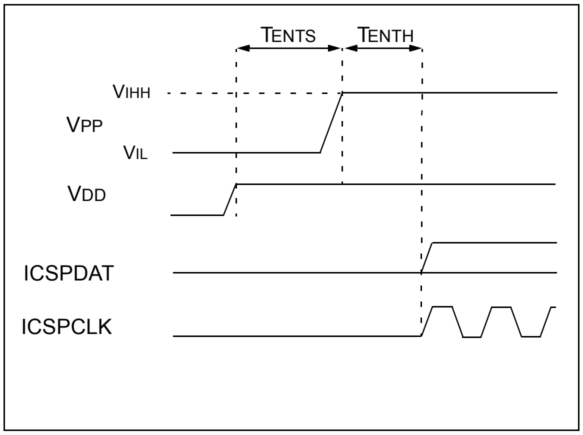


FIGURE 8-2: PROGRAMMING MODE ENTRY – VPP FIRST

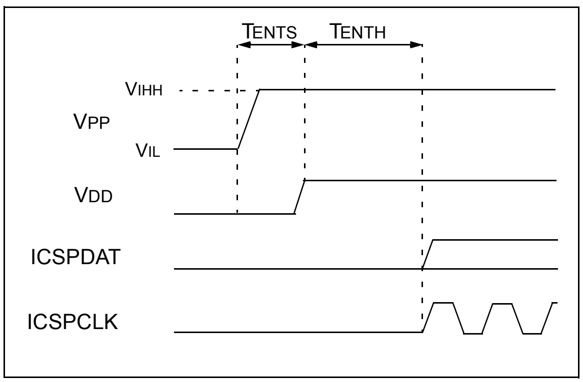


FIGURE 8-3: PROGRAMMING MODE EXIT – VPP LAST

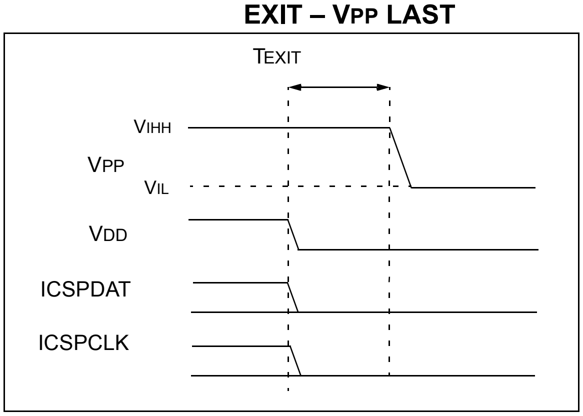


FIGURE 8-4: PROGRAMMING MODE EXIT – VDD LAST

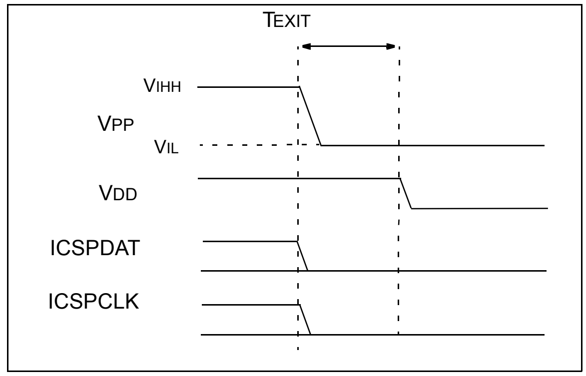


FIGURE 8-5: CLOCK AND DATA TIMING

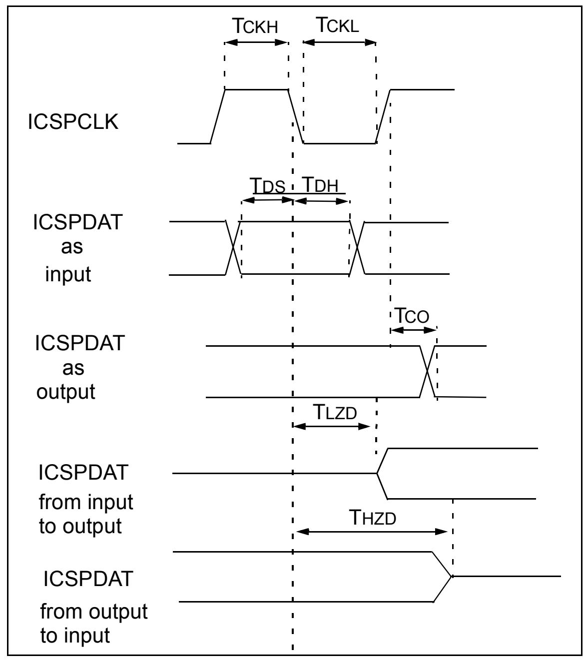
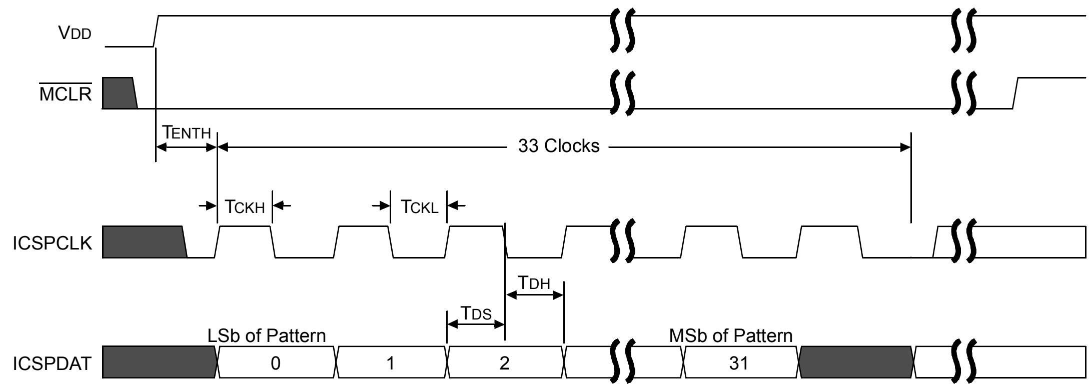


FIGURE 8-9: LVP ENTRY (POWERING UP)



Note 1: Sequence matching can start with no edge on $\overline{\text{MCLR}}$ first.

APPENDIX A: REVISION HISTORY

Revision A (06/2012)

Initial release of this document.

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