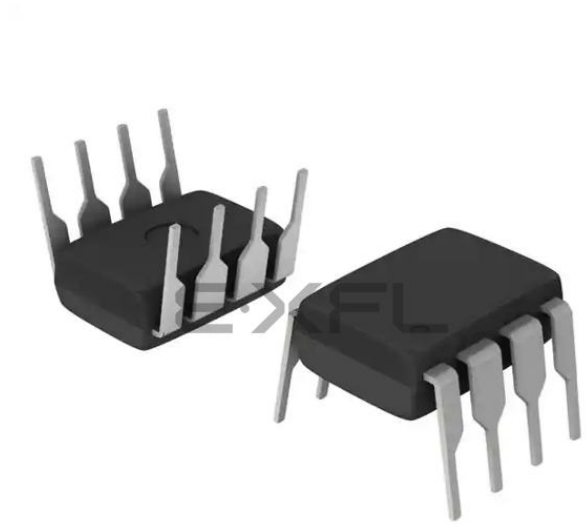

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

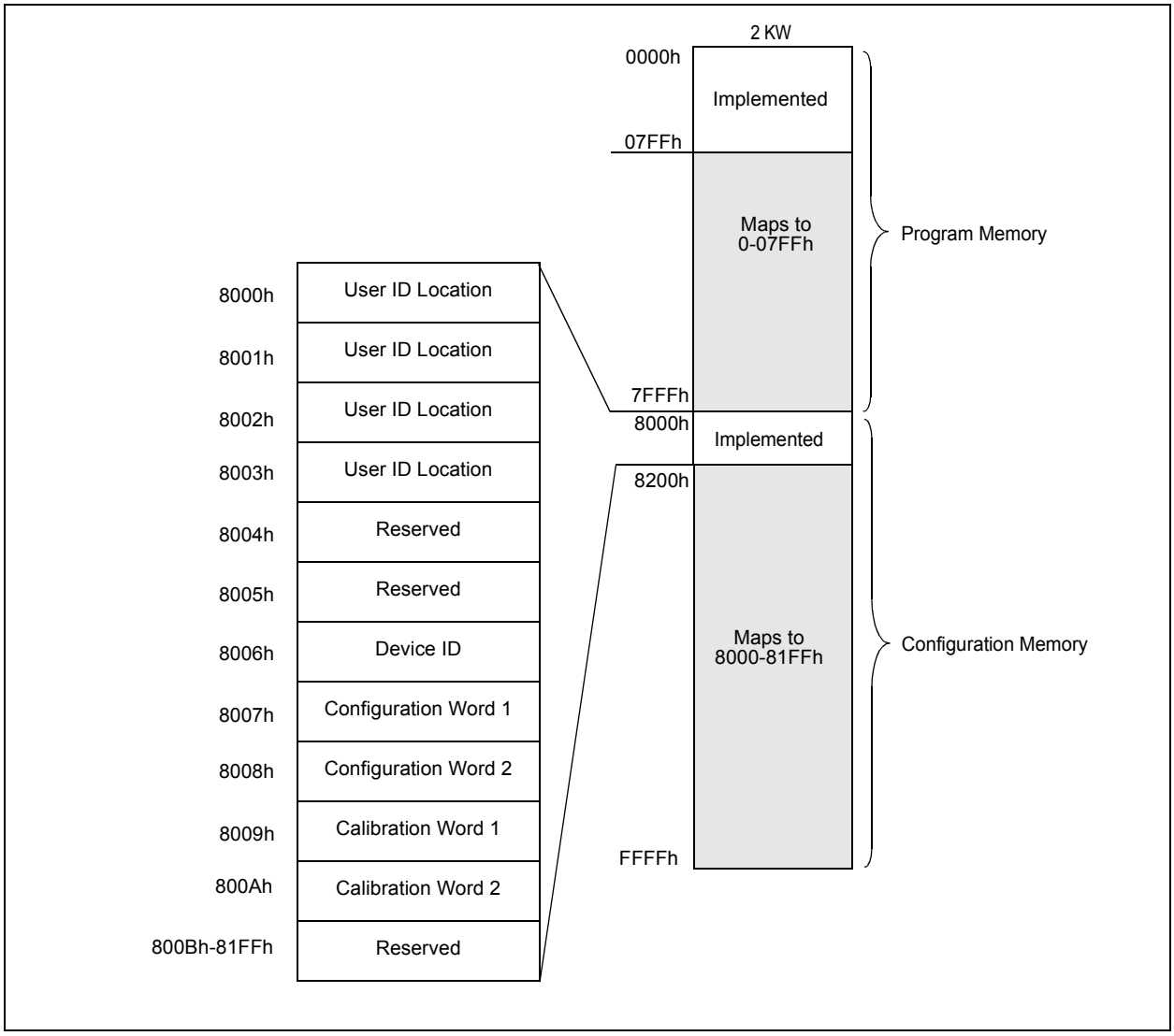
## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 32MHz |
| Connectivity | I²C, SPI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 5 |
| Program Memory Size | 3.5KB (2K x 14) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 256 x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.8V ~ 3.6V |
| Data Converters | A/D 4x10b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 8-DIP (0.300", 7.62mm) |
| Supplier Device Package | 8-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1552-i-p |

## 3.0 MEMORY MAP

The memory is broken into two sections: program memory and configuration memory.

**FIGURE 3-1: PIC12LF1552 PROGRAM MEMORY MAPPING**



**REGISTER 3-2: CONFIGURATION WORD 1**

| U-1 | U-1 | R/P-1 | R/P-1 | R/P-1 | U-1(3) |
|---|---|---|---|---|---|
| — | — | $\overline{\text{CLKOUTEN}}$ | BOREN<1:0> | | — |
| bit 13 | | | | | bit 8 |

| R/P-1 | R/P-1 | R/P-1 | R/P-1 | R/P-1 | U-1 | R/P-1 | R/P-1 |
|---|---|---|---|---|---|---|---|
| $\overline{\text{CP}}$ | MCLRE | $\overline{\text{PWRTE}}$ | WDTE<1:0> | | — | FOSC<1:0> | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | |
|---|---|---|
| R = Readable bit | P = Programmable bit | U = Unimplemented bit, read as '1' |
| '0' = Bit is cleared | '1' = Bit is set | -n = Value when blank or after Bulk Erase |

bit 13-12 **Unimplemented:** Read as '1'

bit 11 **$\overline{\text{CLKOUTEN}}$:** Clock Out Enable bit
1 = CLKOUT function is disabled. I/O or oscillator function on CLKOUT pin.
0 = CLKOUT function is enabled on CLKOUT pin

bit 10-9 **BOREN<1:0>:** Brown-out Reset Enable bits(1)
When enabled, Brown-out Reset Voltage ($V_{BOR}$) is set by the BORV bit of the Configuration Word 2 register.
11 = Brown-out Reset enabled. SPBOREN bit is ignored.
10 = Brown-out Reset enabled while running and disabled in Sleep. SBOREN bit is ignored.
01 = Brown-out Reset controlled by the SBOREN bit in the BORCON register
00 = Brown-out Reset disabled. SBOREN bit is ignored

bit 8(3) **Unimplemented:** Read as '1'

bit 7 **$\overline{\text{CP}}$:** Code Protection bit(2)
1 = Program memory code protection is disabled
0 = Program memory code protection is enabled

bit 6 **MCLRE:** $\overline{\text{MCLR}}$/$V_{PP}$ Pin Function Select bit
If LVP bit = 1:
This bit is ignored.
If LVP bit = 0:
1 = $\overline{\text{MCLR}}$/$V_{PP}$ pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
0 = $\overline{\text{MCLR}}$/$V_{PP}$ pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up under control of WPUA register.

bit 5 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 4-3 **WDTE<1:0>:** Watchdog Timer Enable bit
11 = WDT enabled. SWDTEN is ignored.
10 = WDT enabled while running and disabled in Sleep. SWDTEN is ignored.
01 = WDT controlled by the SWDTEN bit in the WDTCON register
00 = WDT disabled. SWDTEN is ignored.

bit 2 **Unimplemented:** Read as '1'

bit 1-0 **FOSC<1:0>:** Oscillator Selection bits
11 = ECH: External Clock, High-Power mode: on CLKIN pin
10 = ECM: External Clock, Medium-Power mode: on CLKIN pin
01 = ECL: External Clock, Low-Power mode: on CLKIN pin
00 = INTOSC oscillator: I/O function on OSC1 pin

**Note 1:** Enabling Brown-out Reset does not automatically enable Power-up Timer.
**2:** The entire program memory will be erased when the code protection is turned off.
**3:** This bit should be maintained as '1' when programmed.

## 4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

### 4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high voltage:

- VPP – First entry mode
- VDD – First entry mode

#### 4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{MCLR}$ from 0V to VIHH.
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, the device will execute code when Configuration Word 1 has $\overline{MCLR}$ disabled (MCLRE = 0), the Power-up Timer is disabled ($\overline{PWRTE}$ = 0), the internal oscillator is selected (FOSC = 100), and ICSPCLK and ICSPDAT pins are driven by the user application. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

#### 4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{MCLR}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

#### 4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{MCLR}$ to VDD or lower (VIL). See Figures 8-3 and 8-4.

### 4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the device to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to '1', the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to '0'. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{MCLR}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{MCLR}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{MCLR}$ to VIL. See Figure 8-8 and Figure 8-9.

| **Note:** | To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts. |
|---|---|

## 4.3 Program/Verify Commands

The device implements ten programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

**TABLE 4-1: COMMAND MAPPING**

| Command | Mapping | | | | | | | Data/Note |
|---|---|---|---|---|---|---|---|---|
| | Binary (MSb … LSb) | | | | | | Hex | |
| Load Configuration | x | 0 | 0 | 0 | 0 | 0 | 00h | 0, data (14), 0 |
| Load Data For Program Memory | x | 0 | 0 | 0 | 1 | 0 | 02h | 0, data (14), 0 |
| Read Data From Program Memory | x | 0 | 0 | 1 | 0 | 0 | 04h | 0, data (14), 0 |
| Increment Address | x | 0 | 0 | 1 | 1 | 0 | 06h | — |
| Reset Address | x | 1 | 0 | 1 | 1 | 0 | 16h | — |
| Begin Internally Timed Programming | x | 0 | 1 | 0 | 0 | 0 | 08h | — |
| Begin Externally Timed Programming | x | 1 | 1 | 0 | 0 | 0 | 18h | — |
| End Externally Timed Programming | x | 0 | 1 | 0 | 1 | 0 | 0Ah | — |
| Bulk Erase Program Memory | x | 0 | 1 | 0 | 0 | 1 | 09h | Internally Timed |
| Row Erase Program Memory | x | 1 | 0 | 0 | 0 | 1 | 11h | Internally Timed |

### 4.3.1 LOAD CONFIGURATION

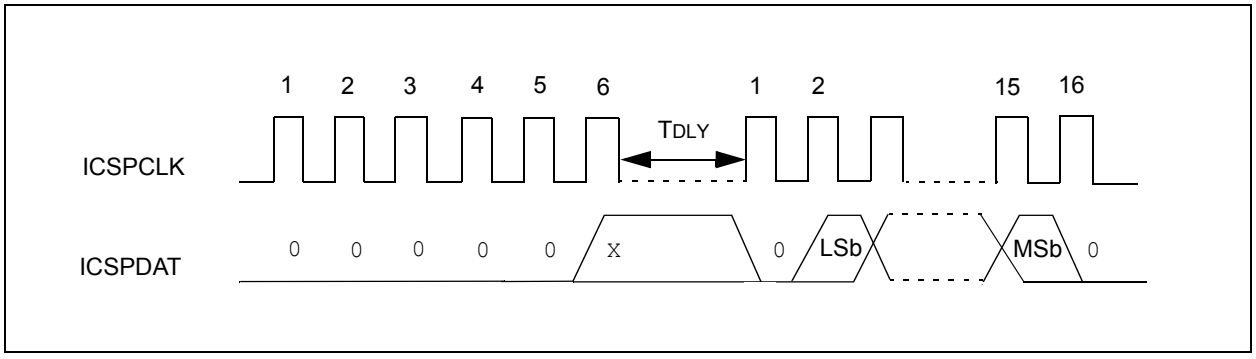
The Load Configuration command is used to access the configuration memory (user ID locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

**Note:** Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

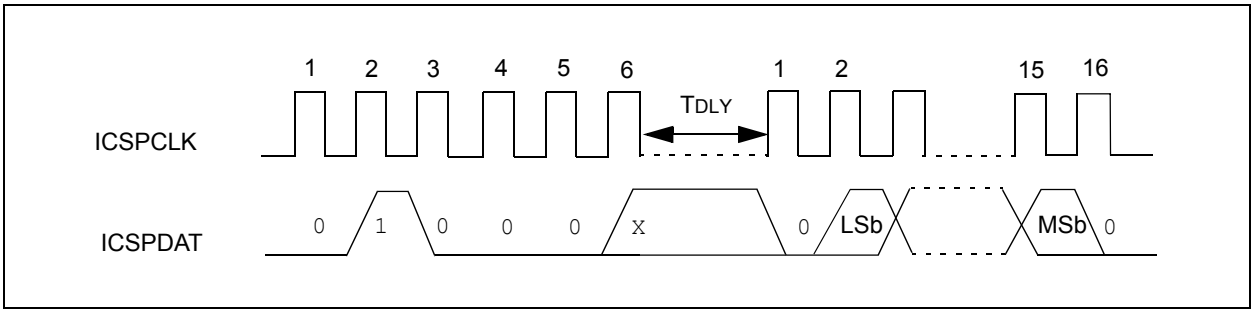
**FIGURE 4-1: LOAD CONFIGURATION**



### 4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

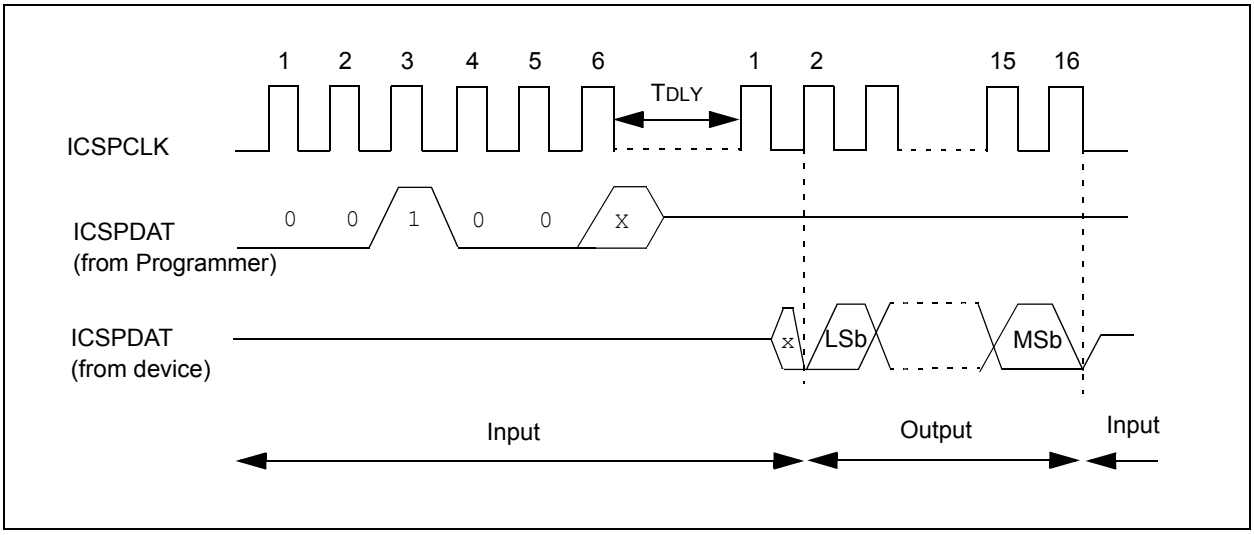
**FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY**




### 4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

**FIGURE 4-3: READ DATA FROM PROGRAM MEMORY**



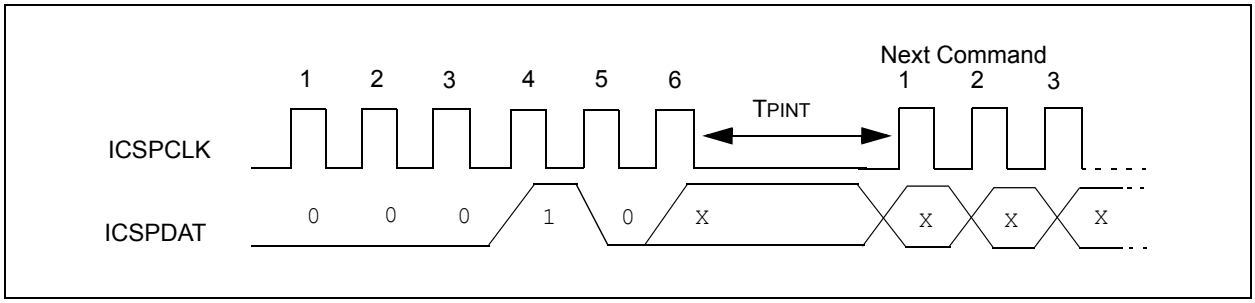
### 4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

**FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING**

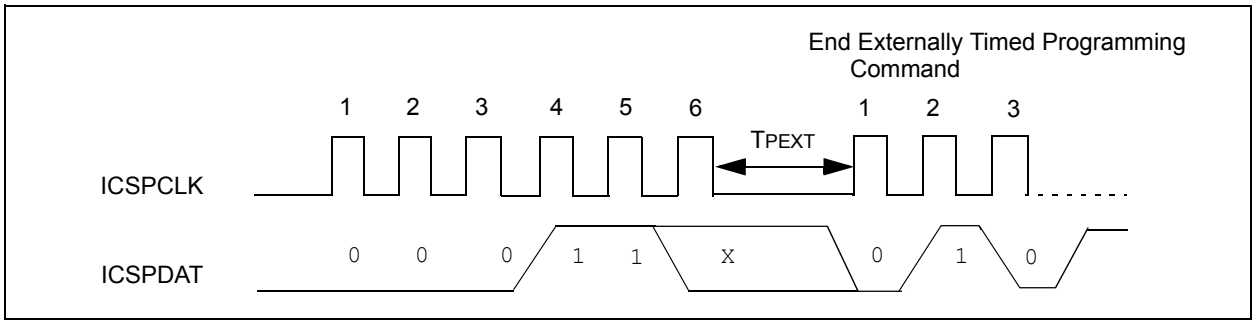



### 4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

**FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING**



### 4.3.10 ROW ERASE PROGRAM MEMORY

The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of the device and the PC bits used to address them. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h, the Row Erase Program Memory command will only erase the user ID locations, regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command, the erase will not complete until the time interval, TERAR, has expired.

**TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES**

| Device | PC | Row Size | Number of Latches |
|---|---|---|---|
| PIC12LF1552 | <15:4> | 16 | 16 |

**FIGURE 4-10: ROW ERASE PROGRAM MEMORY**

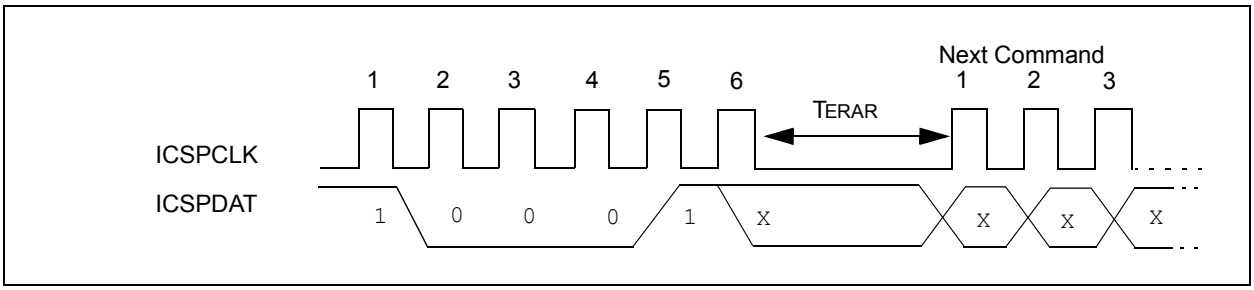
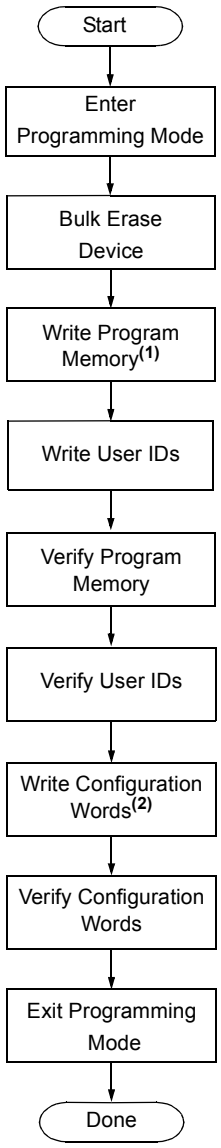
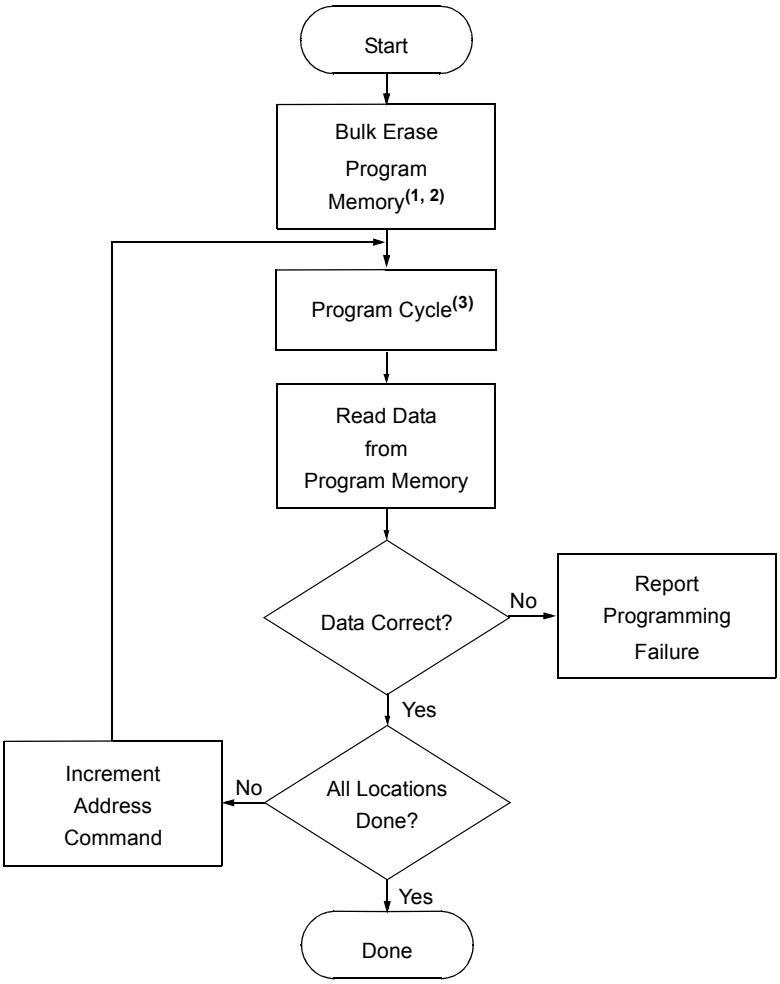


**FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART**




**Note 1:** See Figure 5-2.
**2:** See Figure 5-5.

**FIGURE 5-2: PROGRAM MEMORY FLOWCHART**



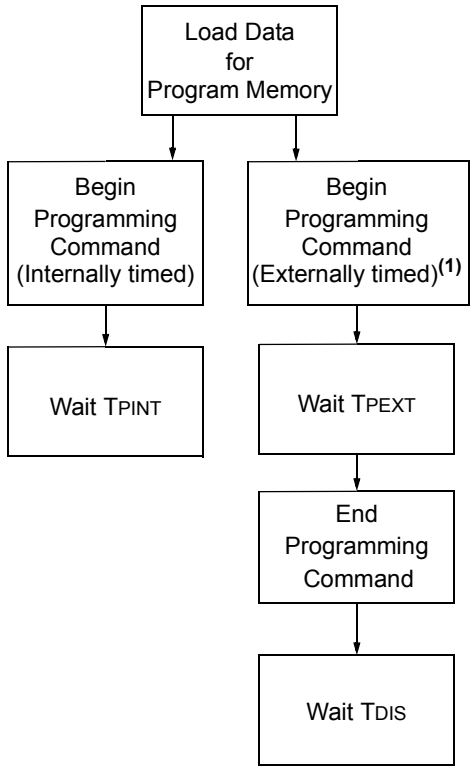

**Note 1:** This step is optional if the device has already been erased or has not been previously programmed.

**2:** If the device is code-protected or must be completely erased, then Bulk Erase the device per Figure 5-6.

**3:** See Figure 5-3 or Figure 5-4.

**FIGURE 5-3: ONE-WORD PROGRAM CYCLE**




**Note 1:** Externally timed writes are not supported for Configuration and Calibration bits.

**FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE**

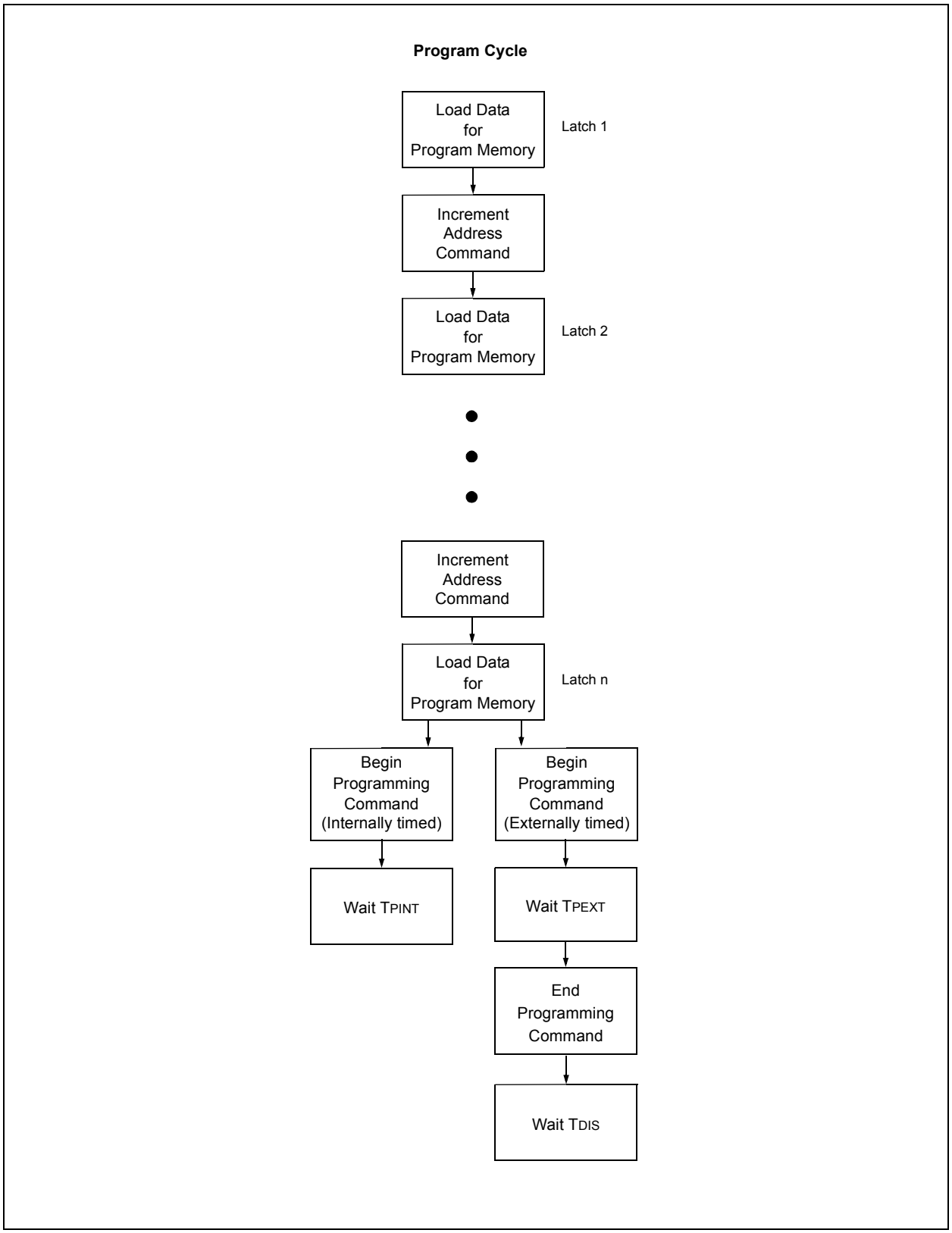
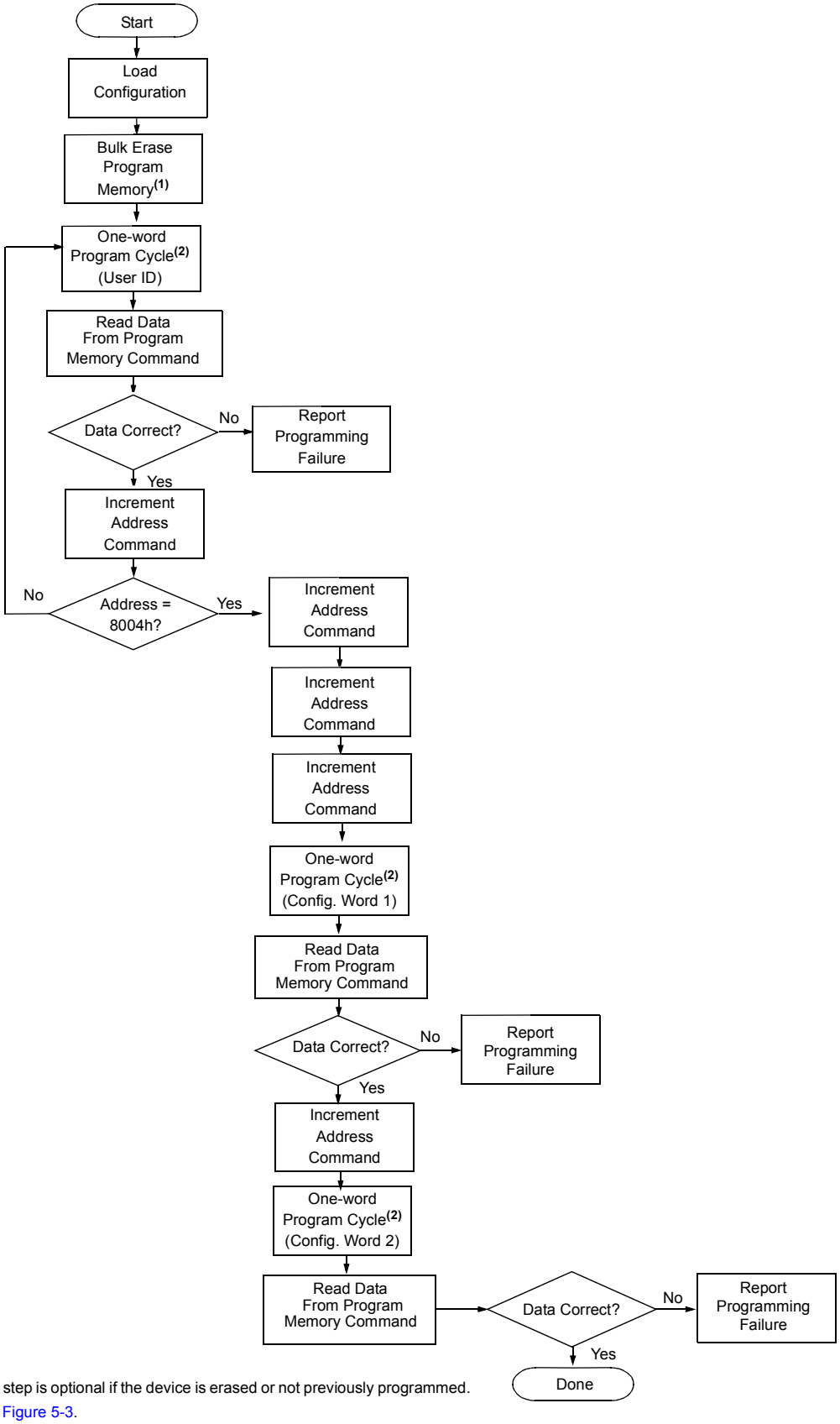


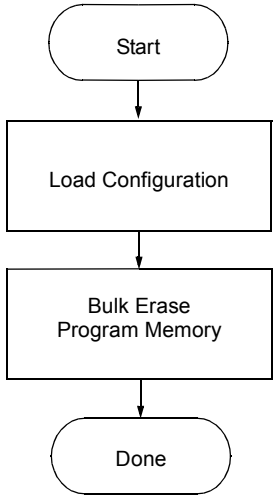
**FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART**




**Note 1:** This step is optional if the device is erased or not previously programmed.

**2:** See Figure 5-3.

**FIGURE 5-6: ERASE FLOWCHART**




**Note:** This sequence does not erase the Calibration Words.

### 7.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

**EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED (CP = 0), PIC12LF1552, 00AAh AT FIRST AND LAST ADDRESS**

| | | |
|---|---|---|
| PIC12LF1552 | Configuration Word 1 | 3F7Fh(1) |
| | Configuration Word 1 mask | 0E7Bh(2) |
| | Configuration Word 2 | 3FFFh(3) |
| | Configuration Word 2 mask | 2E03h(4) |
| | User ID (8000h) | 000Eh(5) |
| | User ID (8001h) | 0008h(5) |
| | User ID (8002h) | 0005h(5) |
| | User ID (8003h) | 0008h(5) |
| | Sum of User IDs | = (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 + (0005h and 000Fh) << 4 + (0008h and 000Fh)(6) |
| | | = E000h + 0800h + 0050h + 0008h |
| | | = E858h |
| | Checksum | = (3F7Fh and 0E7Bh) + (3FFFh and 2E03h) + Sum of User IDs(7) |
| | | = 0E7Bh +2E03h + E858h |
| | | = 24D6h |

**Note 1:** This value is obtained by making all bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 3F7Fh.

**2:** This value is obtained by making all used bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 0E7Bh.

**3:** This value is obtained by making all bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 3FFFh.

**4:** This value is obtained by making all used bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 2E03h.

**5:** These values are picked at random for this example; they could be any 16-bit value.

**6:** In order to calculate the sum of user IDs, take the 16-bit value of the first user ID location (000Eh), AND the address to (000Fh), thus masking the MSB. This gives you the value 000Eh, then shift left 12 bits, giving you E000h. Do the same procedure for the 16-bit value of the second user ID location (0008h), except shift left 8 bits. Also, do the same for the third user ID location (0005h), except shift left 4 bits. For the fourth user ID location do not shift. Finally, add up all four user ID values to get the final sum of user IDs of E858h.

**7:** This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of user IDs: (3F7Fh AND 0E7Bh) + (3FFFh AND 2E03h) + E858h = 24D6h.

## 8.0 ELECTRICAL SPECIFICATIONS

Refer to the device specific data sheet for absolute maximum ratings.

**TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE**

| AC/DC CHARACTERISTICS | | Standard Operating Conditions<br>Production tested at 25°C | | | | |
|---|---|---|---|---|---|---|
| **Sym.** | **Characteristics** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions/Comments** |
| **Supply Voltages and Currents** | | | | | | |
| VDD | **VDD** | | | | | |
| | Read/Write and Row Erase operations | VDDMIN | — | VDDMAX | V | |
| | Bulk Erase operations | 2.7 | — | VDDMAX | V | |
| IDDI | Current on VDD, Idle | — | — | 1.0 | mA | |
| IDDP | Current on VDD, Programming | — | — | 3.0 | mA | |
| | **VPP** | | | | | |
| IPP | Current on $\overline{MCLR}$/VPP | — | — | 600 | μA | |
| VIHH | High voltage on $\overline{MCLR}$/VPP for Program/Verify mode entry | 8.0 | — | 9.0 | V | |
| TVHHR | $\overline{MCLR}$ rise time (VIL to VIHH) for Program/Verify mode entry | — | — | 1.0 | μs | |
| | **I/O pins** | | | | | |
| VIH | (ICSPCLK, ICSPDAT, $\overline{MCLR}$/VPP) input high level | 0.8 VDD | — | — | V | |
| VIL | (ICSPCLK, ICSPDAT, $\overline{MCLR}$/VPP) input low level | — | — | 0.2 VDD | V | |
| VOH | ICSPDAT output high level | VDD-0.7 | — | — | V | IOH = 3.5 mA, VDD = 5V<br>IOH = 3 mA, VDD = 3.3V<br>IOH = 2 mA, VDD = 1.8V |
| VOL | ICSPDAT output low level | — | — | 0.6 | V | IOH = 8 mA, VDD = 5V<br>IOH = 6 mA, VDD = 3.3V<br>IOH = 3 mA, VDD = 1.8V |
| **Programming Mode Entry and Exit** | | | | | | |
| TENTS | Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or $\overline{MCLR}$↑ | 100 | — | — | ns | |
| TENTH | Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or $\overline{MCLR}$↑ | 250 | — | — | μs | |
| **Serial Program/Verify** | | | | | | |
| TCKL | Clock Low Pulse Width | 100 | — | — | ns | |
| TCKH | Clock High Pulse Width | 100 | — | — | ns | |
| TDS | Data in setup time before clock↓ | 100 | — | — | ns | |
| TDH | Data in hold time after clock↓ | 100 | — | — | ns | |
| TCO | Clock↑ to data out valid (during a Read Data command) | 0 | — | 80 | ns | |
| TLZD | Clock↓ to data low-impedance (during a Read Data command) | 0 | — | 80 | ns | |
| THZD | Clock↓ to data high-impedance (during a Read Data command) | 0 | — | 80 | ns | |
| TDLY | Data input not driven to next clock input (delay required between command/data or command/command) | 1.0 | — | — | μs | |
| TERAB | Bulk Erase cycle time | — | — | 5 | ms | |
| TERAR | Row Erase cycle time | — | — | 2.5 | ms | |
| TPINT | Internally timed programming operation time | —<br>— | —<br>— | 2.5<br>5 | ms<br>ms | Program memory<br>Configuration Words |
| TPEXT | Externally timed programming pulse | 1.0 | — | 2.1 | ms | **Note 1** |
| TDIS | Time delay from program to compare (HV discharge time) | 300 | — | — | μs | |
| TEXIT | Time delay when exiting Program/Verify mode | 1 | — | — | μs | |

**Note 1:** Externally timed writes are not supported for Configuration and Calibration bits.

**FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING**

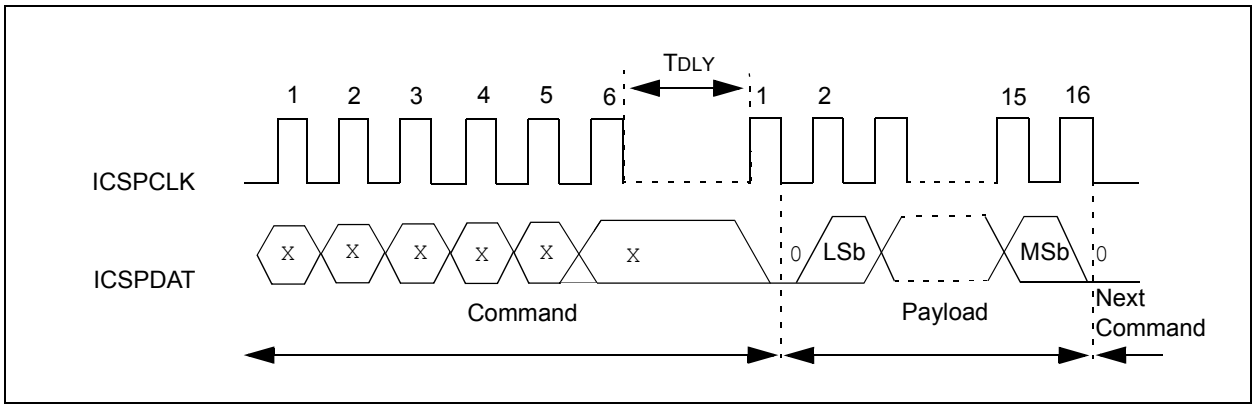



**FIGURE 8-7: READ COMMAND-PAYLOAD TIMING**

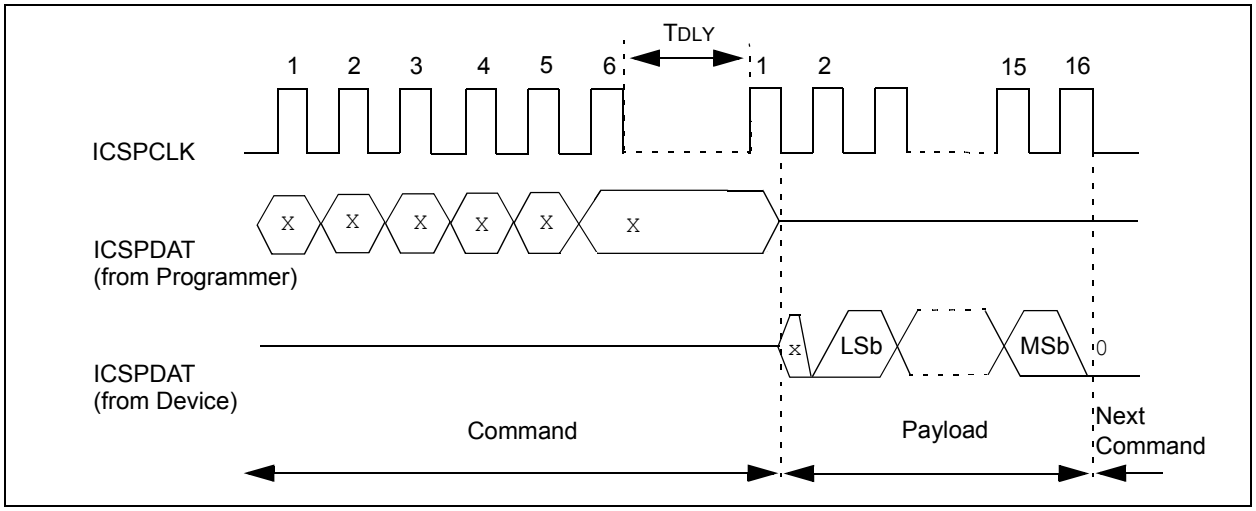



**FIGURE 8-8: LVP ENTRY (POWERED)**

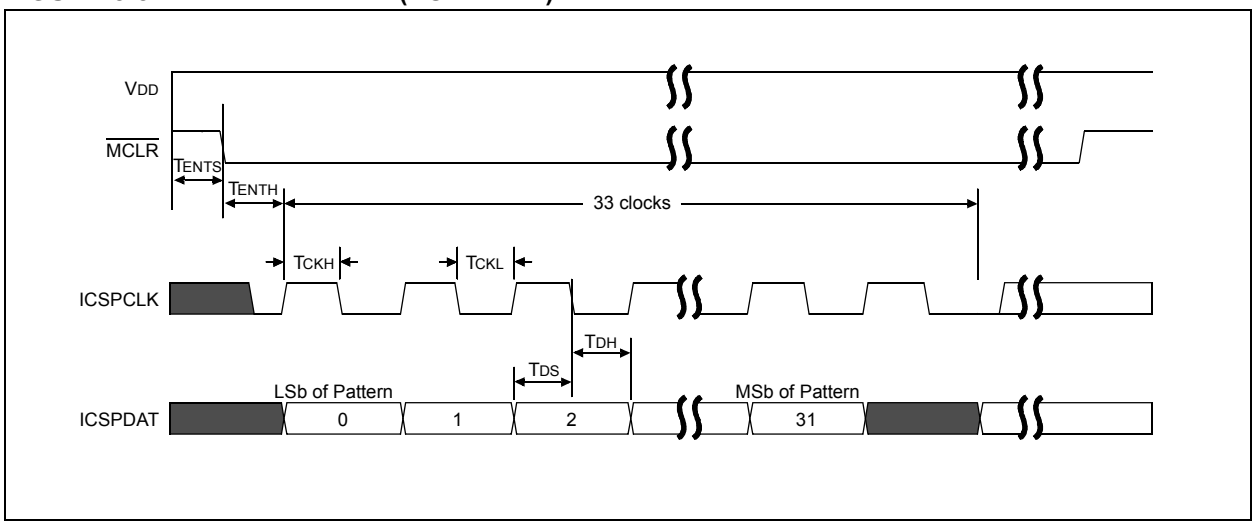
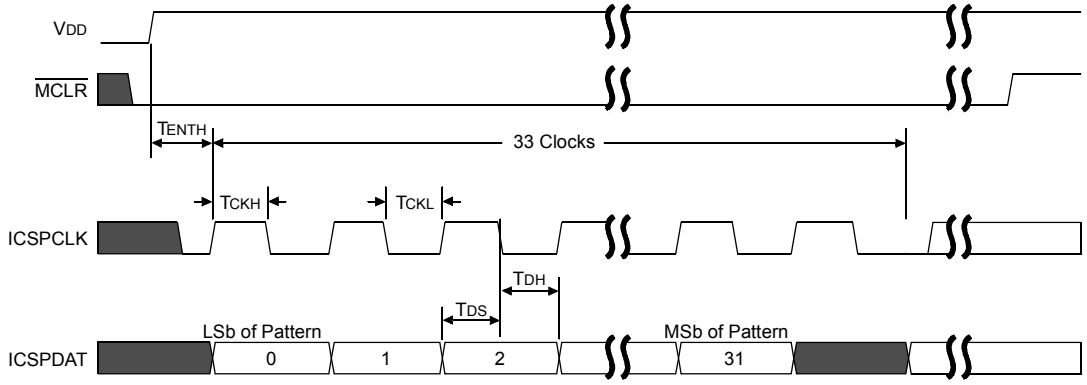


**FIGURE 8-9: LVP ENTRY (POWERING UP)**




**Note 1:** Sequence matching can start with no edge on $\overline{MCLR}$ first.

## APPENDIX A: REVISION HISTORY

### Revision A (06/2012)

Initial release of this document.

**Note the following details of the code protection feature on Microchip devices:**

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
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