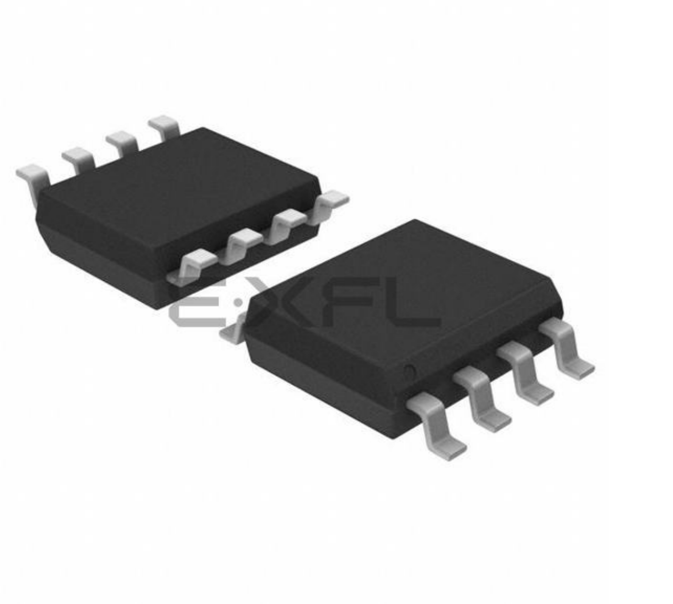

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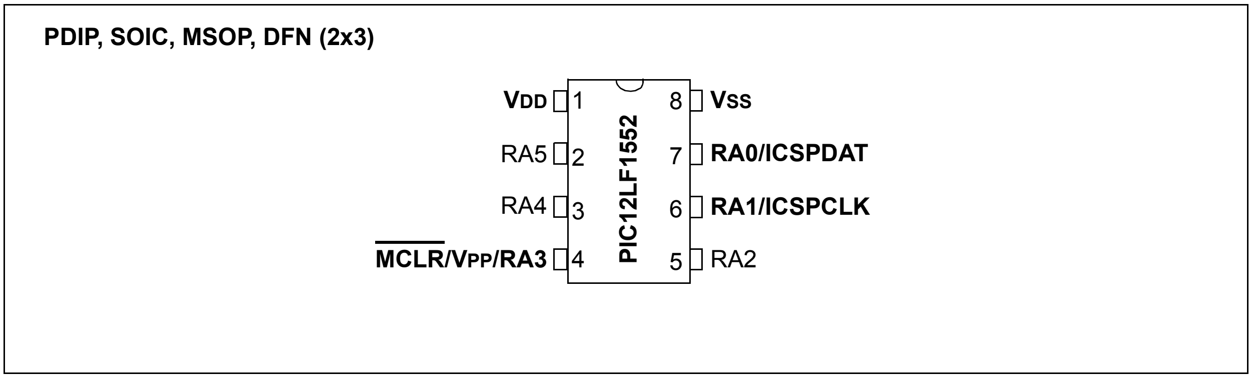
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, SPI
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	5
Program Memory Size	3.5KB (2K x 14)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	8-SOIC (0.154", 3.90mm Width)
Supplier Device Package	8-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic12lf1552t-i-sn

2.0 DEVICE PINOUTS

The pin diagram is shown in Figure 2-1. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagram.

FIGURE 2-1: 8-PIN PDIP, SOIC, MSOP, DFN DIAGRAM FOR PIC12LF1552

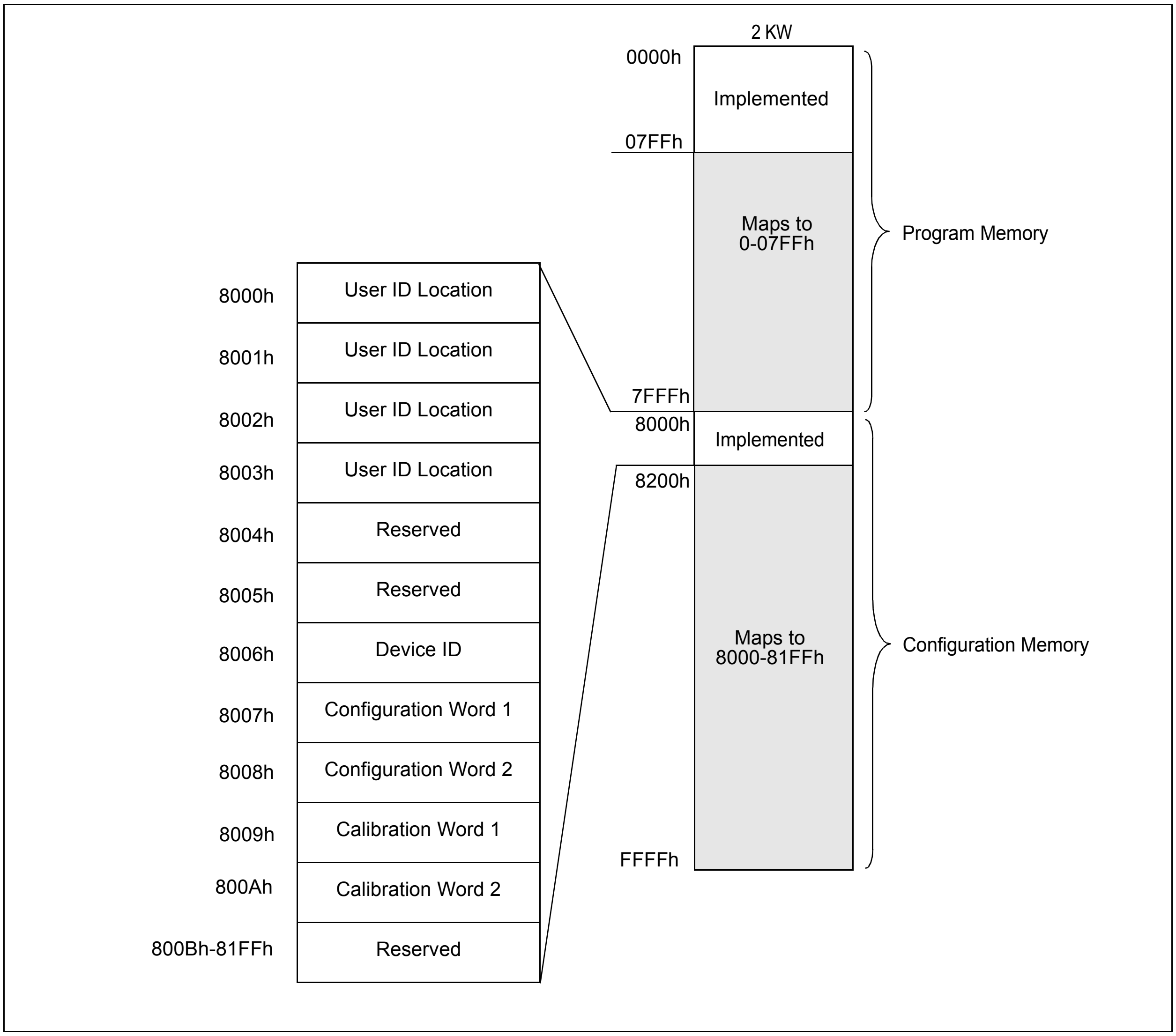


 Preliminary

3.0 MEMORY MAP

The memory is broken into two sections: program memory and configuration memory.

FIGURE 3-1: PIC12LF1552 PROGRAM MEMORY MAPPING



4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode, both the ICSPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/Os are automatically configured as high-impedance inputs and the address is cleared.

4.1 High-Voltage Program/Verify Mode Entry and Exit

There are two different methods of entering Program/Verify mode via high voltage:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to VIHH.
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode. For example, the device will execute code when Configuration Word 1 has $\overline{\text{MCLR}}$ disabled (MCLRE = `0`), the Power-up Timer is disabled ($\overline{\text{PWRTE}}$ = `0`), the internal oscillator is selected (FOSC = `100`), and ICSPCLK and ICSPDAT pins are driven by the user application. Since this may prevent entry, VPP-first entry mode is strongly recommended. See the timing diagram in Figure 8-2.

4.1.2 VDD – FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from VDD or below to VIHH.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-1.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower (VIL). See Figures 8-3 and 8-4.

4.2 Low-Voltage Programming (LVP) Mode

The Low-Voltage Programming mode allows the device to be programmed using VDD only, without high voltage. When the LVP bit of Configuration Word 2 register is set to ‘`1`’, the low-voltage ICSP programming entry is enabled. To disable the Low-Voltage ICSP mode, the LVP bit must be programmed to ‘`0`’. This can only be done while in the High-Voltage Entry mode.

Entry into the Low-Voltage ICSP Program/Verify modes requires the following steps:

1. $\overline{\text{MCLR}}$ is brought to VIL.
2. A 32-bit key sequence is presented on ICSPDAT, while clocking ICSPCLK.

The key sequence is a specific 32-bit pattern, `'0100 1101 0100 0011 0100 1000 0101 0000'` (more easily remembered as MCHP in ASCII). The device will enter Program/Verify mode only if the sequence is valid. The Least Significant bit of the Least Significant nibble must be shifted in first.

Once the key sequence is complete, $\overline{\text{MCLR}}$ must be held at VIL for as long as Program/Verify mode is to be maintained.

For low-voltage programming timing, see Figure 8-8 and Figure 8-9.

Exiting Program/Verify mode is done by no longer driving $\overline{\text{MCLR}}$ to VIL. See Figure 8-8 and Figure 8-9.

Note:	To enter LVP mode, the LSB of the Least Significant nibble must be shifted in first. This differs from entering the key sequence on other parts.

4.3 Program/Verify Commands

The device implements ten programming commands; each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of TDLY between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	—
Reset Address	x	1	0	1	1	0	16h	—
Begin Internally Timed Programming	x	0	1	0	0	0	08h	—
Begin Externally Timed Programming	x	1	1	0	0	0	18h	—
End Externally Timed Programming	x	0	1	0	1	0	0Ah	—
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

4.3.1 LOAD CONFIGURATION

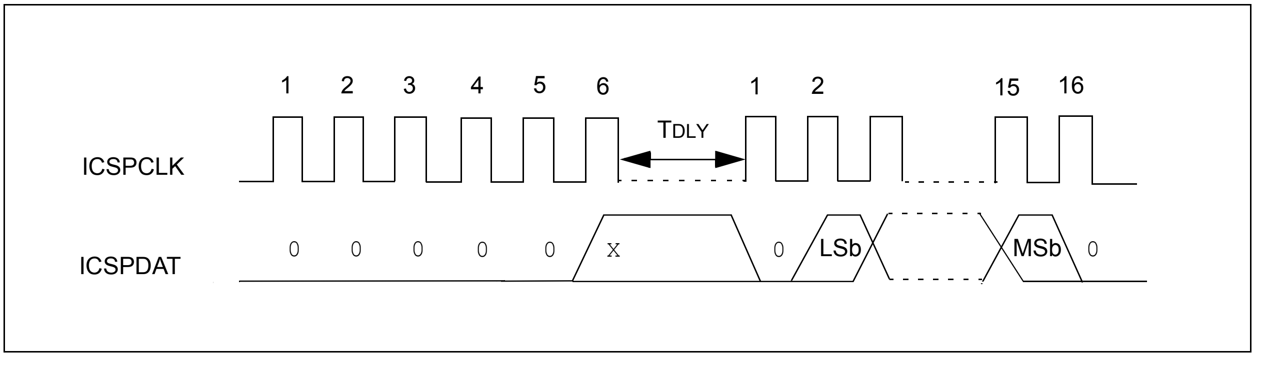
The Load Configuration command is used to access the configuration memory (user ID locations, Configuration Words, Calibration Words). The Load Configuration command sets the address to 8000h and loads the data latches with one word of data (see Figure 4-1).

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

> **Note:** Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

The only way to get back to the program memory (address 0) is to exit Program/Verify mode or issue the Reset Address command after the configuration memory has been accessed by the Load Configuration command.

FIGURE 4-1: LOAD CONFIGURATION

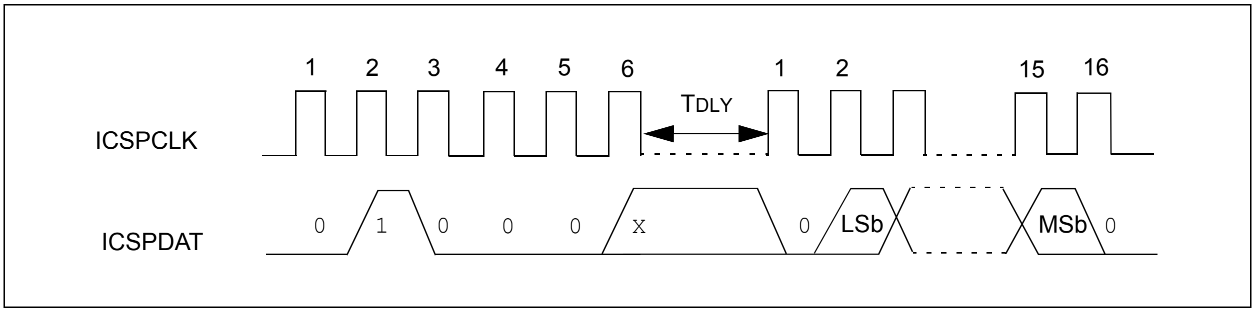


 Preliminary

4.3.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word programs into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is issued (see Figure 4-2).

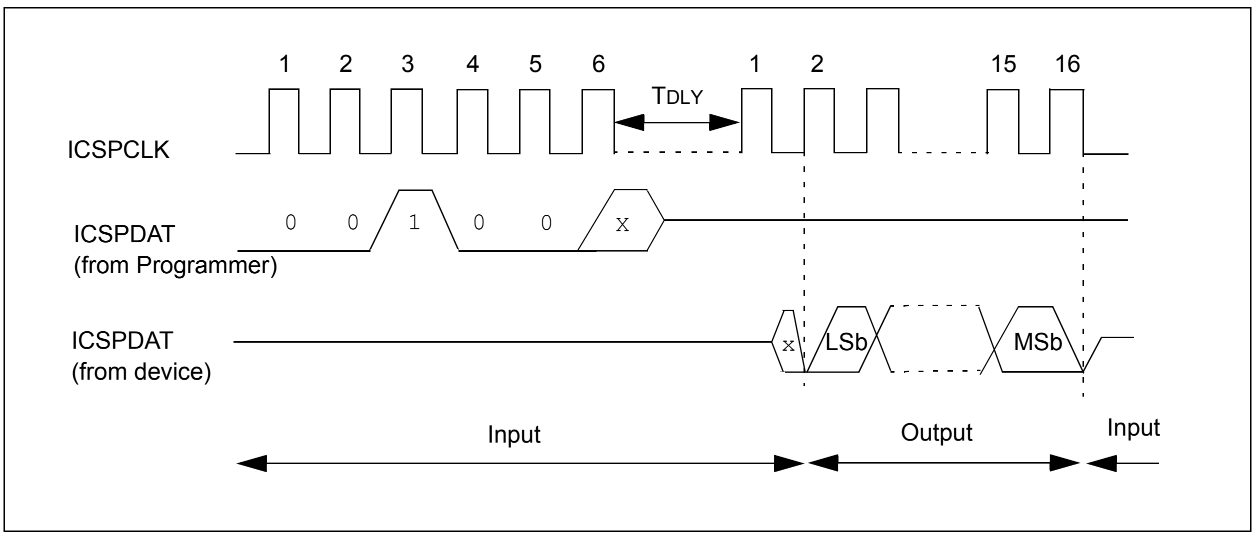
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.3.3 READ DATA FROM PROGRAM MEMORY

The Read Data from Program Memory command will transmit data bits out of the program memory map currently accessed, starting with the second rising edge of the clock input. The ICSPDAT pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros (see Figure 4-3).

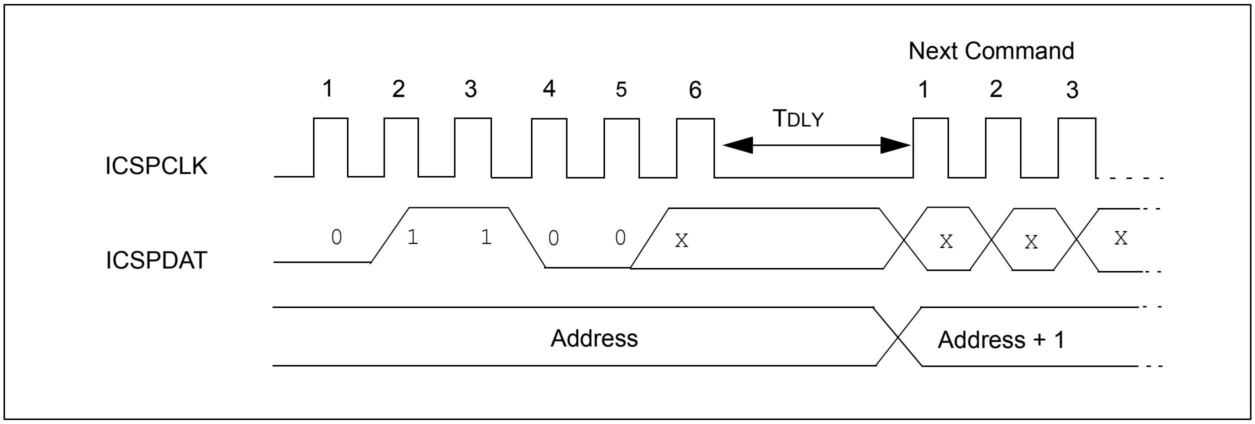
FIGURE 4-3: READ DATA FROM PROGRAM MEMORY



4.3.4 INCREMENT ADDRESS

The address is incremented when this command is received. It is not possible to decrement the address. To reset this counter, the user must use the Reset Address command or exit Program/Verify mode and re-enter it. If the address is incremented from address 7FFFh, it will wrap-around to location 0000h. If the address is incremented from FFFFh, it will wrap-around to location 8000h.

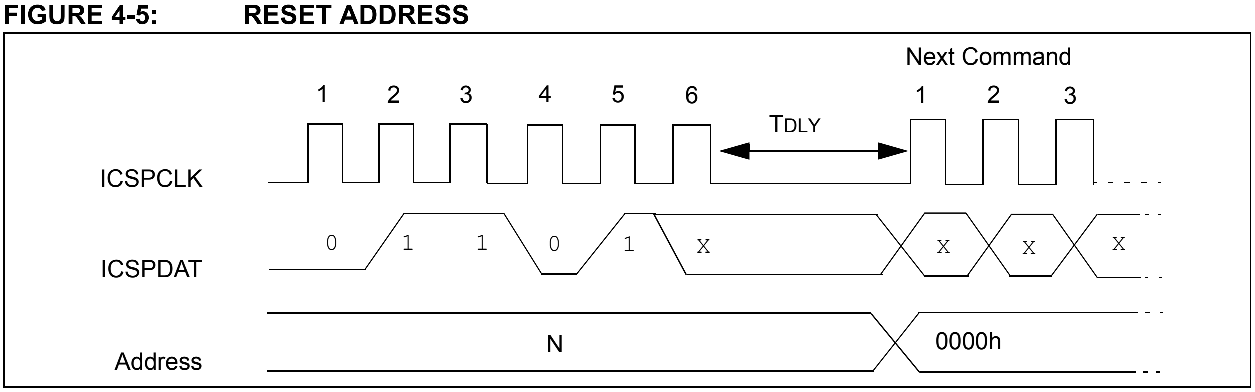
FIGURE 4-4: INCREMENT ADDRESS



4.3.5 RESET ADDRESS

The Reset Address command will reset the address to 0000h, regardless of the current value. The address is used in program memory or the configuration memory.

FIGURE 4-5: RESET ADDRESS



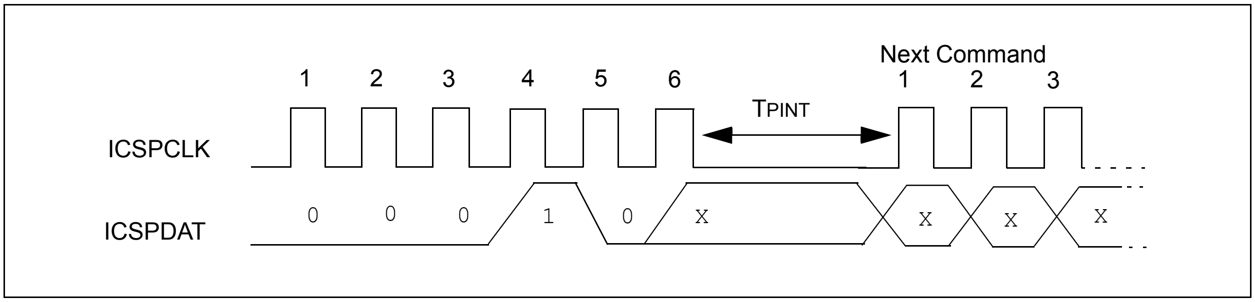
4.3.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time, TPINT, for the programming to complete.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

The program memory address that is being programmed is not erased prior to being programmed.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

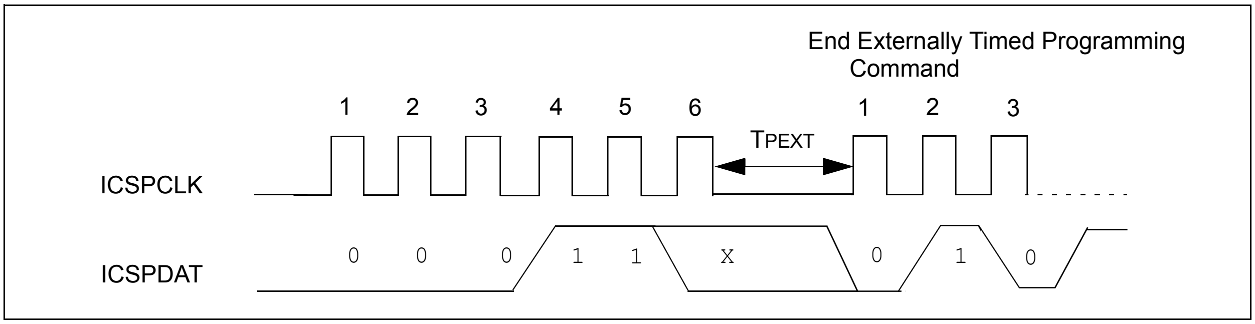


4.3.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming, the End Externally Timed Programming command must be sent in the specified time window defined by TPEXT (see Figure 4-7).

Externally timed writes are not supported for Configuration and Calibration bits. Any externally timed write to the Configuration or Calibration Word will have no effect on the targeted word.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING



4.3.10 ROW ERASE PROGRAM MEMORY

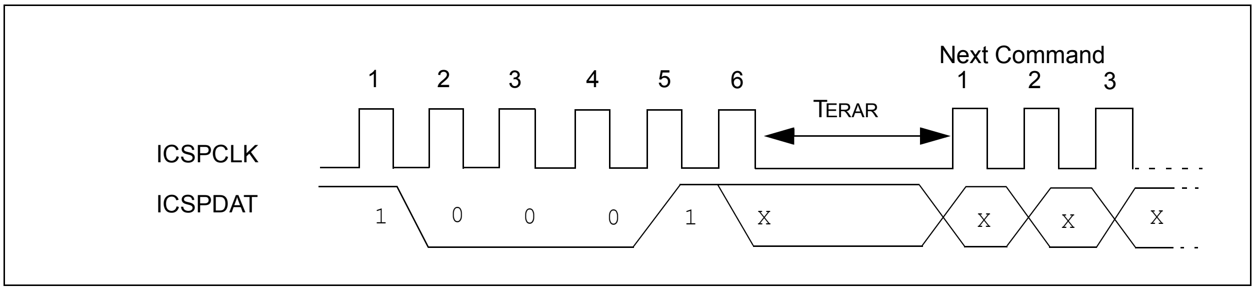
The Row Erase Program Memory command will erase an individual row. Refer to Table 4-2 for row sizes of the device and the PC bits used to address them. If the program memory is code-protected, the Row Erase Program Memory command will be ignored. When the address is 8000h-8008h, the Row Erase Program Memory command will only erase the user ID locations, regardless of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command, the erase will not complete until the time interval, TERAR, has expired.

TABLE 4-2: PROGRAMMING ROW SIZE AND LATCHES

Device	PC	Row Size	Number of Latches
PIC12LF1552	<15:4>	16	16

FIGURE 4-10: ROW ERASE PROGRAM MEMORY



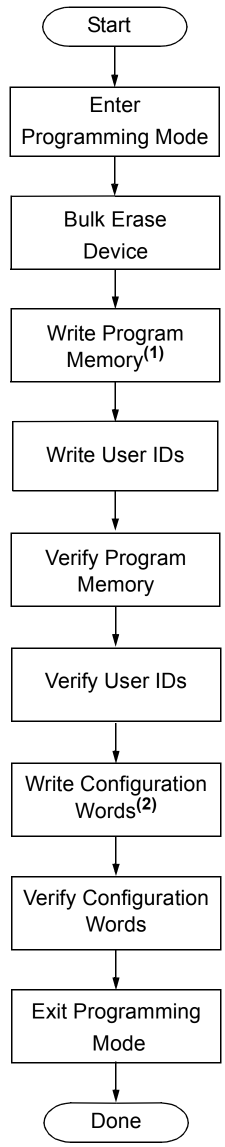
5.0 PROGRAMMING ALGORITHMS

The device uses internal latches to temporarily store the 14-bit words used for programming. Refer to Table 4-2 for specific latch information. The data latches allow the user to write the program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration command is used to load a single data latch. The data latch will hold the data until the Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the LSbs of the address. The PC's address at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given will determine which location(s) in memory are written. Writes cannot cross the physical boundary. For example, attempting to write from address 0002h-0009h will result in data being written to 0008h-000Fh.

If more than the maximum number of data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command, the data in the data latches will be overwritten. The following figures show the recommended flowcharts for programming.

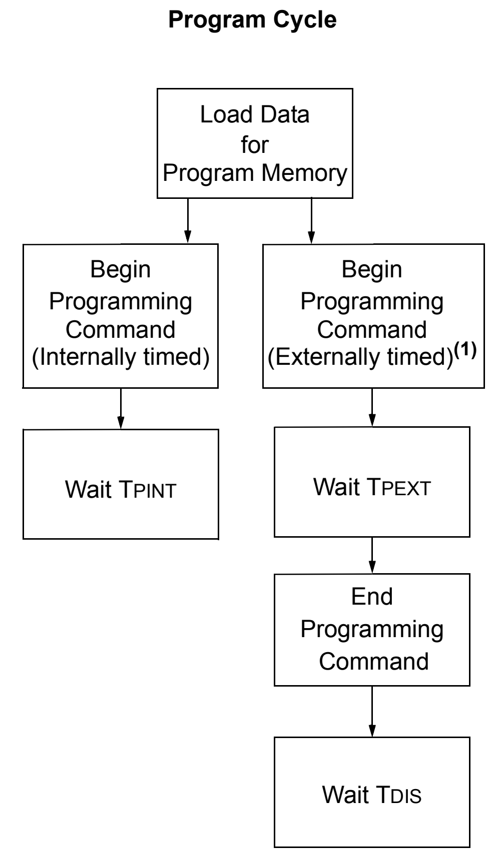
FIGURE 5-1: DEVICE PROGRAM/VERIFY FLOWCHART



Note 1: See Figure 5-2.

2: See Figure 5-5.

FIGURE 5-3: ONE-WORD PROGRAM CYCLE



Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 5-4: MULTIPLE-WORD PROGRAM CYCLE

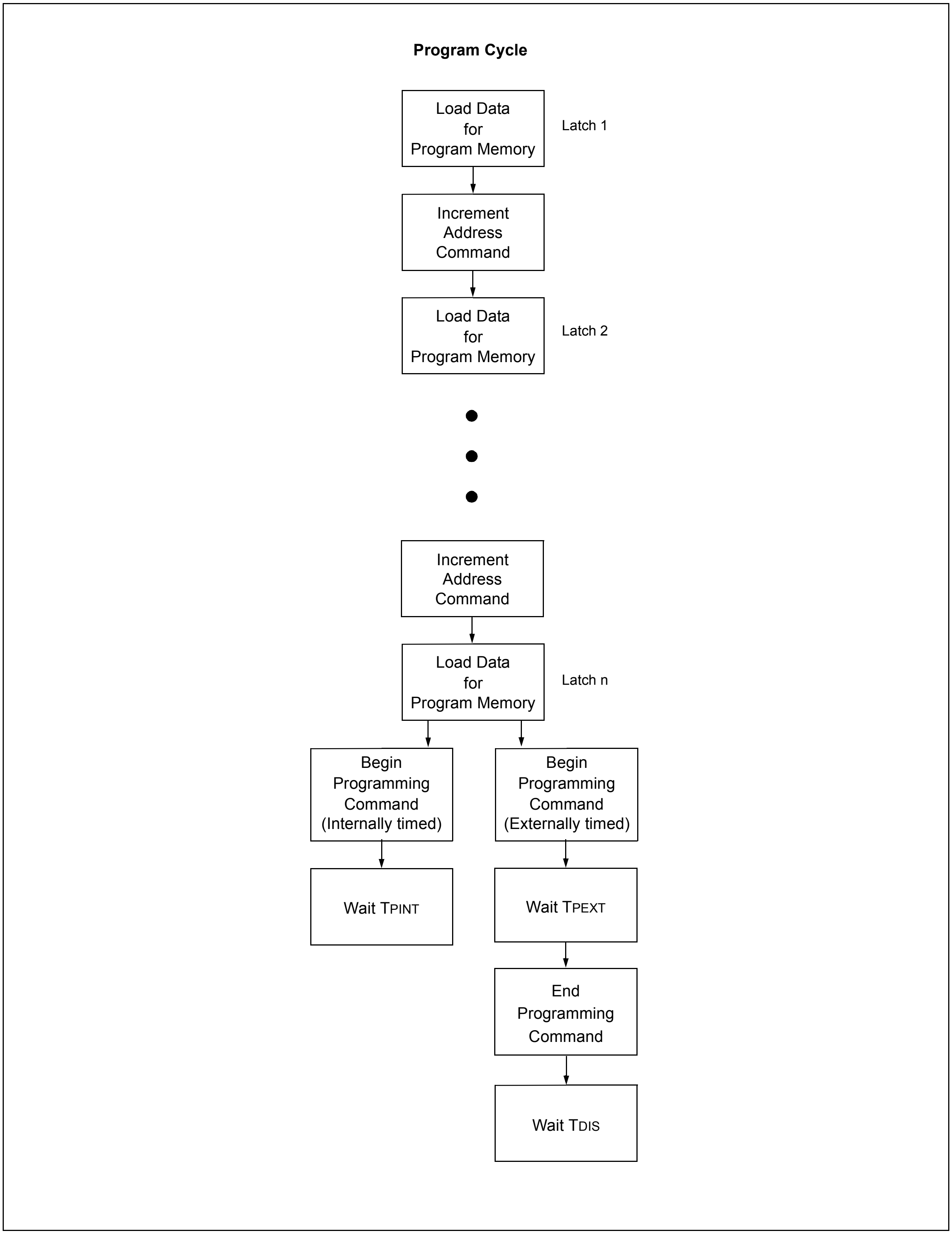
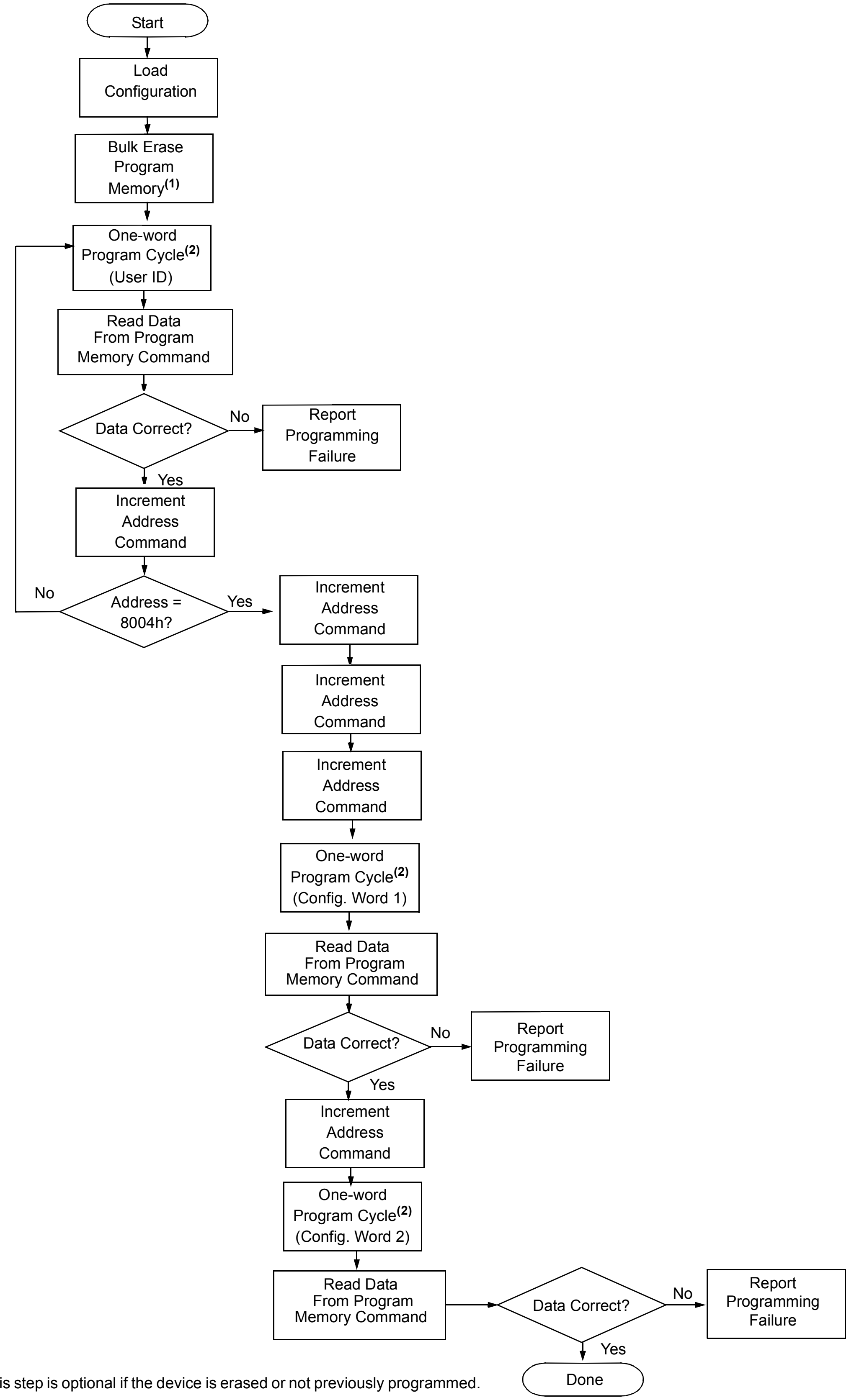


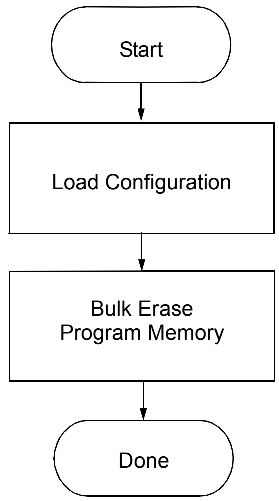
FIGURE 5-5: CONFIGURATION MEMORY PROGRAM FLOWCHART



Note 1: This step is optional if the device is erased or not previously programmed.

2: See Figure 5-3.

FIGURE 5-6: ERASE FLOWCHART



Note: This sequence does not erase the Calibration Words.

7.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{CP}$ Configuration bit.

TABLE 7-1: CONFIGURATION WORD MASK VALUES

Device	Config. Word 1 Mask	Config. Word 2 Mask
PIC12LF1552	0EFBh	2E03h

7.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data starting at address 0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits are ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

EXAMPLE 7-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED ($\overline{CP}$ = 1), PIC12LF1552, 00AAh AT FIRST AND LAST ADDRESS

PIC12LF1552	Sum of Memory addresses 0000h-07FFh	7956h(1)
	Configuration Word 1	3FFFh(2)
	Configuration Word 1 mask	0EFBh(3)
	Configuration Word 2	3FFFh(4)
	Configuration Word 2 mask	2E03h(5)

Checksum = 7956h + (3FFFh and 0EFBh) + (3FFFh and 2E03h)(6)
= 7956h + 0EFBh + 2E03h
= B654h

Note 1: This value is obtained by taking the total number of program memory locations (0x000 to 0x7FFh which is 800h) subtracting 2h which yields 7FEh, then multiplying it by the blank memory value of 0x3FFF to get the sum of 1FF 7802h. Then, truncate to 16 bits the value of 7802h. Now add 00AAh (00AAh + 00AAh) to 7802h to get the final value of B654h.

2: This value is obtained by making all bits of the Configuration Word 1 a '1', then converting it to hex, thus having a value of 3FFFh.

3: This value is obtained by making all used bits of the Configuration Word 1 a '1', then converting it to hex, thus having a value of 0EFBh.

4: This value is obtained by making all bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 3FFFh.

5: This value is obtained by making all used bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 2E03h.

6: This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of memory addresses: (3FFFh and 0EFBh) + (3FFFh and 2E03h) + 7956h = B654h. Then, truncate to 16 bits, thus having a final value of B654h.

7.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner: The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 8000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Words (all unimplemented Configuration bits are masked to '0').

EXAMPLE 7-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED ($\overline{CP}$ = 0), PIC12LF1552, 00AAh AT FIRST AND LAST ADDRESS

PIC12LF1552	Configuration Word 1	3F7Fh[(1)]
	Configuration Word 1 mask	0E7Bh[(2)]
	Configuration Word 2	3FFFh[(3)]
	Configuration Word 2 mask	2E03h[(4)]
	User ID (8000h)	000Eh[(5)]
	User ID (8001h)	0008h[(5)]
	User ID (8002h)	0005h[(5)]
	User ID (8003h)	0008h[(5)]

Sum of User IDs = (000Eh and 000Fh) << 12 + (0008h and 000Fh) << 8 +
(0005h and 000Fh) << 4 + (0008h and 000Fh)[(6)]
= E000h + 0800h + 0050h + 0008h
= E858h

Checksum = (3F7Fh and 0E7Bh) + (3FFFh and 2E03h) + Sum of User IDs[(7)]
= 0E7Bh +2E03h + E858h
= 24D6h

Note 1: This value is obtained by making all bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 3F7Fh.

2: This value is obtained by making all used bits of the Configuration Word 1 a '1', but the code-protect bit is '0' (thus, enabled), then converting it to hex, thus having a value of 0E7Bh.

3: This value is obtained by making all bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 3FFFh.

4: This value is obtained by making all used bits of the Configuration Word 2 a '1', then converting it to hex, thus having a value of 2E03h.

5: These values are picked at random for this example; they could be any 16-bit value.

6: In order to calculate the sum of user IDs, take the 16-bit value of the first user ID location (000Eh), AND the address to (000Fh), thus masking the MSB. This gives you the value 000Eh, then shift left 12 bits, giving you E000h. Do the same procedure for the 16-bit value of the second user ID location (0008h), except shift left 8 bits. Also, do the same for the third user ID location (0005h), except shift left 4 bits. For the fourth user ID location do not shift. Finally, add up all four user ID values to get the final sum of user IDs of E858h.

7: This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask Value and adding it to the sum of user IDs: (3F7Fh AND 0E7Bh) + (3FFFh AND 2E03h) + E858h = 24D6h.

8.0 ELECTRICAL SPECIFICATIONS

Refer to the device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions Production tested at 25°C				
Sym.	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
	Supply Voltages and Currents					
VDD	**VDD**					
	Read/Write and Row Erase operations	VDDMIN	—	VDDMAX	V	
	Bulk Erase operations	2.7	—	VDDMAX	V	
IDDI	Current on VDD, Idle	—	—	1.0	mA	
IDDP	Current on VDD, Programming	—	—	3.0	mA	
	VPP					
IPP	Current on MCLR/VPP	—	—	600	µA	
VIHH	High voltage on MCLR/VPP for Program/Verify mode entry	8.0	—	9.0	V	
TVHHR	MCLR rise time (VIL to VIHH) for Program/Verify mode entry	—	—	1.0	µs	
	I/O pins					
VIH	(ICSPCLK, ICSPDAT, MCLR/VPP) input high level	0.8 VDD	—	—	V	
VIL	(ICSPCLK, ICSPDAT, MCLR/VPP) input low level	—	—	0.2 VDD	V	
VOH	ICSPDAT output high level	VDD-0.7	—	—	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 2 mA, VDD = 1.8V
VOL	ICSPDAT output low level	—	—	0.6	V	IOH = 8 mA, VDD = 5V IOH = 6 mA, VDD = 3.3V IOH = 3 mA, VDD = 1.8V
	Programming Mode Entry and Exit					
TENTS	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or MCLR↑	100	—	—	ns	
TENTH	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or MCLR↑	250	—	—	µs	
	Serial Program/Verify					
TCKL	Clock Low Pulse Width	100	—	—	ns	
TCKH	Clock High Pulse Width	100	—	—	ns	
TDS	Data in setup time before clock↓	100	—	—	ns	
TDH	Data in hold time after clock↓	100	—	—	ns	
TCO	Clock↑ to data out valid (during a Read Data command)	0	—	80	ns	
TLZD	Clock↓ to data low-impedance (during a Read Data command)	0	—	80	ns	
THZD	Clock↓ to data high-impedance (during a Read Data command)	0	—	80	ns	
TDLY	Data input not driven to next clock input (delay required between command/data or command/command)	1.0	—	—	µs	
TERAB	Bulk Erase cycle time	—	—	5	ms	
TERAR	Row Erase cycle time	—	—	2.5	ms	
TPINT	Internally timed programming operation time	— —	— —	2.5 5	ms ms	Program memory Configuration Words
TPEXT	Externally timed programming pulse	1.0	—	2.1	ms	**Note 1**
TDIS	Time delay from program to compare (HV discharge time)	300	—	—	µs	
TEXIT	Time delay when exiting Program/Verify mode	1	—	—	µs	

Note 1: Externally timed writes are not supported for Configuration and Calibration bits.

FIGURE 8-6: WRITE COMMAND-PAYLOAD TIMING

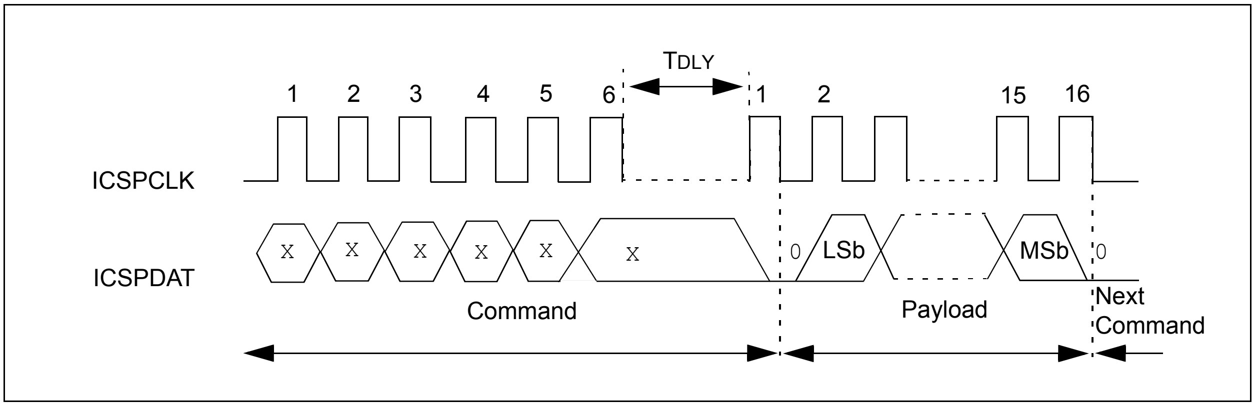


FIGURE 8-7: READ COMMAND-PAYLOAD TIMING

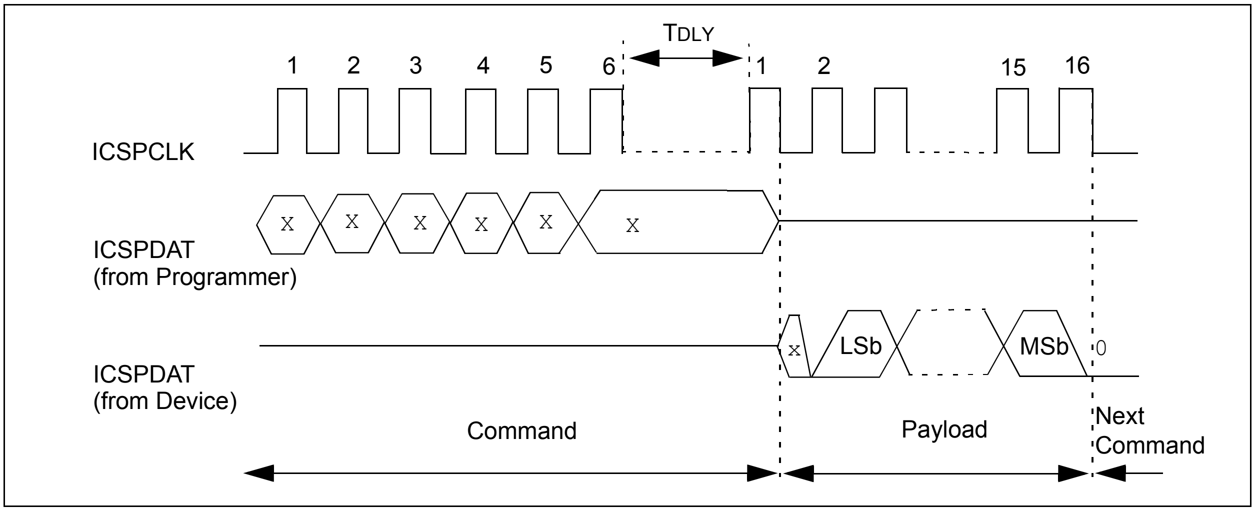


FIGURE 8-8: LVP ENTRY (POWERED)

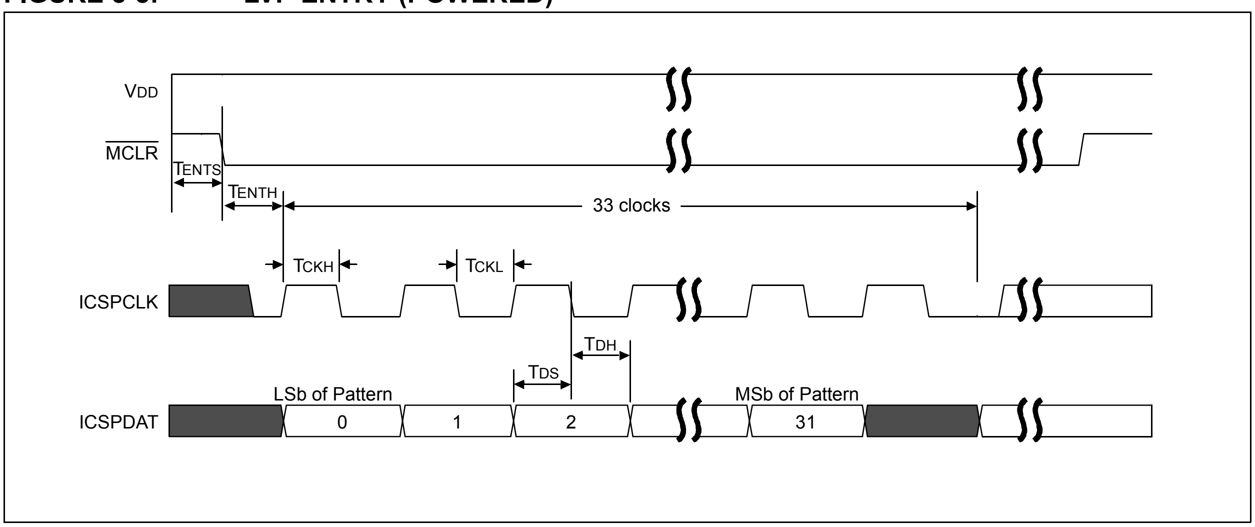
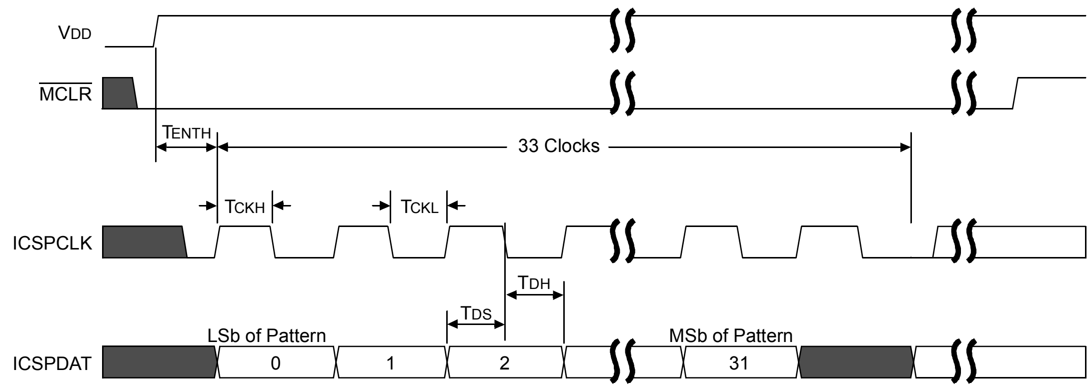


FIGURE 8-9: LVP ENTRY (POWERING UP)



Note 1: Sequence matching can start with no edge on $\overline{\text{MCLR}}$ first.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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