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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	573440
Number of I/O	404
Number of Gates	129600
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv405e-6bg560c

Dedicated Routing

Some signal classes require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two signal classes.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB. Global Clock Distribution Network.
- DLL Location

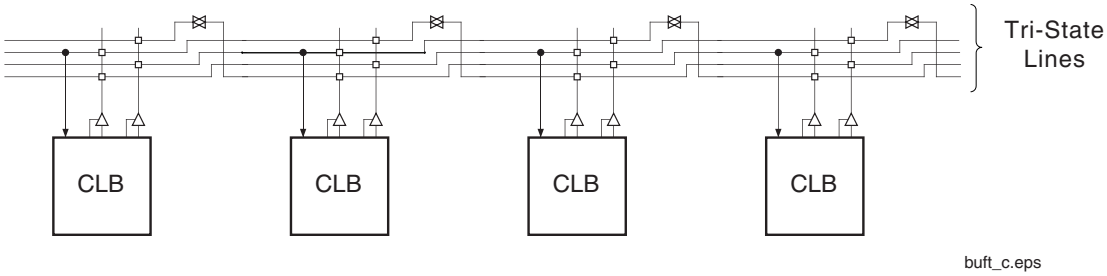

Figure 8: **BUFT Connections to Dedicated Horizontal Bus LInes**

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets can be driven only by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

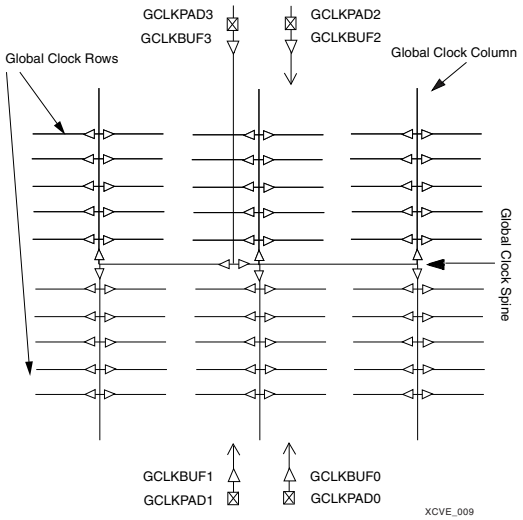

Figure 9: **Global Clock Distribution Network**

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loops

There are eight DLLs (Delay-Locked Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1

where

v = the die version number

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code (see Table 7) is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 7: **IDCODEs Assigned to Virtex-E FPGAs**

FPGA	IDCODE
XCV405EM	v0C28093h
XCV812EM	v0C38093h

Note:
Attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Including Boundary Scan in a Design

Since the boundary scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the boundary scan symbol and connect the necessary pins as appropriate.

Development System

Virtex-E FPGAs are supported by the Xilinx Foundation and Alliance Series CAE tools. The basic methodology for Virtex-E design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex-E design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and Alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex-E FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnec-

Port Signals

Each block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 15 describes the depth and width aspect ratios for the block SelectRAM+ memory.

Table 15: **Block SelectRAM+ Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A/B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A/B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A/B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A/B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A/B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 15.

Data In Bus—DI[A/B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 15.

Data Output Bus—DO[A/B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 15.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$Start = ((ADDR_{port} + 1) * Width_{port}) - 1$$

$$End = ADDR_{port} * Width_{port}$$

Table 16 shows low order address mapping for each port width.

Table 16: **Port Address Mapping**

Port Width	Port Addresses																
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

Creating Larger RAM Structures

The block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

Conflict Resolution

The block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 33 shows a timing diagram for a single port of a block SelectRAM+ memory. The block SelectRAM+ AC switching characteristics are specified in the data sheet. The block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 34 shows a timing diagram for a true dual-port read/write block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location are invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory are correct, but the read port has invalid data. At the first rising edge of CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.

Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

Using SelectI/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards.

SelectI/O, the revolutionary input/output resource of Virtex-E devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each input/output block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 18, each buffer type can support a variety of voltage requirements.

Table 18: **Virtex-E Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

http://www.jedec.org

LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3 V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3 V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5 V applications. This standard requires a 2.5 V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

LVCMOS18 — 1.8 V Low Voltage CMOS

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required.

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3 V output source voltage (V_{CCO}).

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5 V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 40.

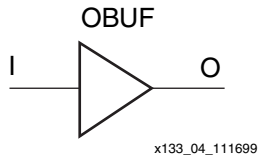

Figure 40: **Virtex-E Output Buffer (OBUF) Symbol**

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows.

```
OBUF_<slew_rate>_<drive_strength>
```

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank.

Table 20 summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 20: **Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards that share compatible V_{CCO} can be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 41, typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

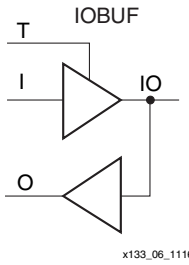

Figure 42: **Input/Output Buffer Symbol (IOBUF)**

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 on page 34 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 46. A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 47.

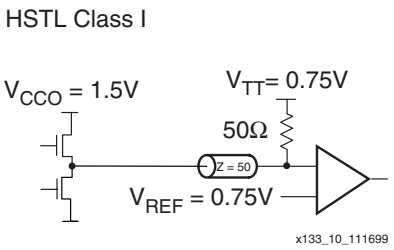

Figure 46: **Terminated HSTL Class I**

Table 25: **HSTL Class I Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

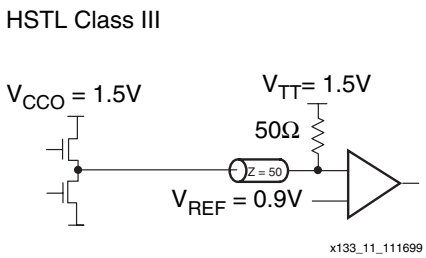

Figure 47: **Terminated HSTL Class III**

Table 26: **HSTL Class III Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	24	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 48.

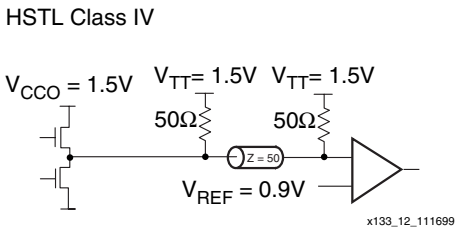

Figure 48: **Terminated HSTL Class IV**

Table 27: **HSTL Class IV Voltage Specification**

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	48	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

VHDL Instantiation

```
data0_p:   IOBUF_LVDS port map
(I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));

data0_inv: INV        port map
(I=>data_out(0),   O=>data_n_out(0));

data0_n  : IOBUF_LVDS port map
(I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

Verilog Instantiation

```
IOBUF_LVDS data0_p(.I(data_out[0]),
.T(data_tri), .IO(data_p[0]),
.O(data_int[0]);

INV        data0_inv (.I(data_out[0],
.O(data_n_out[0]);

IOBUF_LVDS
data0_n(.I(data_n_out[0]),.T(data_tri),.
IO(data_n[0]).O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the UCF or NCF file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB), then any IO_L#PIN pair can be used. If the output side of the bidirectional buffers are asynchronous (no output register), then they must use one of the pairs that is a part of the asynchronous LVDS IOB group. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that can be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product's lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE), and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the "map -pr [i|o|b]", where "i" is inputs only, "o" is outputs only, and "b" is both inputs and outputs. To improve design coding times, VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 44.

The 3-state is configured to be 3-stated at GSR and when the PRE, CLR, S, or R is asserted and shares its clock enable with the output and input register. If this is not desirable, then the library can be updated with the desired functionality by the user. The I/O and IOB inputs to the macros are the external net connections.

Table 44: **Bidirectional I/O Library Macros**

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q

Table 44: **Bidirectional I/O Library Macros *(Continued)***

Name	Inputs	Bidirectional	Outputs
IOBUFDS_LD_LVDS	D, T, G	IO, IOB	Q
IOBUFDS_LDE_LVDS	D, T, GE, G	IO, IOB	Q
IOBUFDS_LDC_LVDS	D, T, G, CLR	IO, IOB	Q
IOBUFDS_LDCE_LVDS	D, T, GE, G, CLR	IO, IOB	Q
IOBUFDS_LDP_LVDS	D, T, G, PRE	IO, IOB	Q
IOBUFDS_LDPE_LVDS	D, T, GE, G, PRE	IO, IOB	Q

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/23/00	1.0	Initial Xilinx release.
08/01/00	1.1	Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table.
09/19/00	1.2	• In Table 3 (Module 4), **FG676 Fine-Pitch BGA — XCV405E**, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1. • Min values added to **Virtex-E Electrical Characteristics** tables.
11/20/00	1.3	• Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3). • Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2). • Added to note 2 of **Absolute Maximum Ratings** (Module 3). • Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3). • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters** (Module 3).
04/02/01	1.4	• In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF. • Updated values in Virtex-E Switching Characteristics tables. • Converted data sheet to modularized format.
04/19/01	1.5	• Modified Figure 30, which shows “DLL Generation of 4x Clock in Virtex-E Devices.”
07/23/01	1.6	• Made minor edits to text under Configuration.
11/16/01	2.0	• Added warning under Configuration section that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.
07/17/02	2.1	• Data sheet designation upgraded from Preliminary to Production.
09/10/02	2.2	• Added clarifications in the Input/Output Block, Configuration, Boundary-Scan Mode, and Block SelectRAM+ Memory sections. Revised Figure 18, Table 11, and Table 36.
11/19/02	2.3	• Added clarification in the Boundary Scan section. • Removed last sentence regarding deactivation of duty-cycle correction in Duty Cycle Correction Property section.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.8 – 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.8 – 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Description(1)		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data might be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data might be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current[1]		XCV405E		400	mA
			XCV812E		500	mA
I_{CCOQ}	Quiescent V_{CCO} supply current[1]		XCV405E		2	mA
			XCV812E		2	mA
I_L	Input or output leakage current		All	–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2	0.25	mA

Notes:
1. With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0 V. The fastest ramp rate is 0 V to nominal voltage in 2 ms and the slowest allowed ramp rate is 0 V to nominal voltage in 50 ms. For more details on power supply requirements, see XAPP158 on www.xilinx.com.

Product (Commercial Grade)	Description(2)	Current Requirement(3)
XCV50E - XCV600E	Minimum required current supply	500 mA
XCV812E - XCV2000E	Minimum required current supply	1 A
XCV2600E - XCV3200E	Minimum required current supply	1.2 A
Virtex-E Family, Industrial Grade	Minimum required current supply	2 A

Notes:
1. Ramp rate used for this specification is from 0 - 1.8 V DC. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents might result if ramp rates are forced to be faster.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL(1)	– 0.5	0.8	2.0	3.6	0.4	2.4	24	– 24
LVCMOS2	– 0.5	0.7	1.7	2.7	0.4	1.9	12	– 12
LVCMOS18	– 0.5	20% V_{CCO}	70% V_{CCO}	1.95	0.4	V_{CCO} – 0.4	8	– 8
PCI, 3.3 V	– 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	– 0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I(3)	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	– 0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.61	V_{REF} + 0.61	7.6	–7.6
SSTL2 II	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.80	V_{REF} + 0.80	15.2	–15.2
CTT	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	– 0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Notes:
1. V_{OL} and V_{OH} for lower drive currents are sample tested.
2. Tested according to the relevant specifications.
3. DC input and output levels for HSTL18 (HSTL I/O standard with V_{CCO} of 1.8 V) are provided in an HSTL white paper on www.xilinx.com.

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
4	IO_L92N_YY	AJ6
4	IO_L93P	AK5
4	IO_L93N	AN3
4	IO_L94P_YY	AL5
4	IO_L94N_YY	AJ7
4	IO_VREF_L95P_YY	AM4
4	IO_L95N_YY	AM5
4	IO_L96P_Y	AK7
4	IO_L96N_Y	AL6
4	IO_L97P_YY	AM6
4	IO_L97N_YY	AN6
4	IO_VREF_L98P_YY	AL7
4	IO_L98N_YY	AJ9
4	IO_L99P	AN7
4	IO_L99N	AL8
4	IO_L100P_YY	AM8
4	IO_L100N_YY	AJ10
4	IO_VREF_L101P_YY	AL9[1]
4	IO_L101N_YY	AM9
4	IO_L102P_Y	AK10
4	IO_L102N_Y	AN9
4	IO_VREF_L103P_YY	AL10
4	IO_L103N_YY	AM10
4	IO_L104P_YY	AL11
4	IO_L104N_YY	AJ12
4	IO_L105P	AN11
4	IO_L105N	AK12
4	IO_L106P_YY	AL12
4	IO_L106N_YY	AM12
4	IO_VREF_L107P_YY	AK13[1]
4	IO_L107N_YY	AL13
4	IO_L108P_Y	AM13
4	IO_L108N_Y	AN13
4	IO_L109P_YY	AJ14
4	IO_L109N_YY	AK14
4	IO_VREF_L110P_YY	AM14
4	IO_L110N_YY	AN15
4	IO_L111P	AJ15
4	IO_L111N	AK15
4	IO_L112P_YY	AL15
4	IO_L112N_YY	AM16
4	IO_VREF_L113P_YY	AL16
4	IO_L113N_YY	AJ16
4	IO_L114P_Y	AK16
4	IO_L114N_Y	AN17
4	IO_LVDS_DLL_L115P	AM17
5	GCK1	AJ17
5	IO	AL18
5	IO	AL25
5	IO	AL28
5	IO	AL30
5	IO	AN28
5	IO_LVDS_DLL_L115N	AM18
5	IO_L116P_YY	AK18
5	IO_VREF_L116N_YY	AJ18
5	IO_L117P_YY	AN19
5	IO_L117N_YY	AL19
5	IO_L118P	AK19
5	IO_L118N	AM20
5	IO_L119P_YY	AJ19
5	IO_VREF_L119N_YY	AL20
5	IO_L120P_YY	AN21
5	IO_L120N_YY	AL21
5	IO_L121P_Y	AJ20
5	IO_L121N_Y	AM22
5	IO_L122P_YY	AK21
5	IO_VREF_L122N_YY	AN23[1]
5	IO_L123P_YY	AJ21
5	IO_L123N_YY	AM23
5	IO_L124P	AK22
5	IO_L124N	AM24
5	IO_L125P_YY	AL23
5	IO_L125N_YY	AJ22

BG560 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
Global Differential Clock					
3	0	A17	C18	NA	IO LVDS 21
2	1	D17	E17	NA	IO LVDS 21
1	5	AJ17	AM18	NA	IO LVDS 115
0	4	AL17	AM17	NA	IO LVDS 115
IO LVDS Total Outputs: 183, Asyncronous Outputs: 79					
0	0	D29	E28	NA	-
1	0	A31	D28	√	-
2	0	C29	E27	√	VREF_0
3	0	D27	B30	1	-
4	0	B29	E26	√	-
5	0	C27	D26	√	VREF_0
6	0	A28	E25	NA	-
7	0	C26	D25	1	-
8	0	B26	E24	1	VREF_0
9	0	D24	C25	1	-
10	0	A25	E23	√	VREF_0
11	0	B24	D23	√	-
12	0	C23	E22	NA	-
13	0	D22	A23	√	-
14	0	B22	E21	√	VREF_0
15	0	C21	D21	1	-
16	0	E20	B21	√	-
17	0	C20	D20	√	VREF_0
18	0	E19	B20	NA	-
19	0	C19	D19	1	-
20	0	D18	A19	1	VREF_0
21	1	E17	C18	NA	GCLK LVDS 3/2
22	1	B17	C17	1	-
23	1	D16	B16	1	VREF_1
24	1	C16	E16	1	-
25	1	C15	A15	NA	-
26	1	E15	D15	√	VREF_1
27	1	D14	C14	√	-
28	1	E14	A13	1	-
29	1	D13	C13	√	VREF_1
30	1	E13	C12	√	-
31	1	D12	A11	NA	-
32	1	C11	B11	√	-
33	1	D11	B10	√	VREF_1
34	1	A9	C10	2	-
35	1	D10	C9	1	VREF_1
36	1	B8	A8	1	-
37	1	C8	E10	NA	-
38	1	A6	B7	√	VREF_1
39	1	D8	C7	√	-
40	1	B5	A5	2	-
41	1	D7	C6	√	VREF_1
42	1	B4	A4	√	-
43	1	E7	C5	NA	-
44	1	A2	D6	√	CS
45	2	D4	E4	√	DIN_D0
46	2	F5	B3	2	-
47	2	F4	C1	NA	-
48	2	G5	E3	1	VREF_2
49	2	D2	G4	1	-

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
1	VCCO	H15
2	VCCO	N18
2	VCCO	M19
2	VCCO	M18
2	VCCO	L19
2	VCCO	K19
2	VCCO	J19
3	VCCO	V19
3	VCCO	U19
3	VCCO	T19
3	VCCO	R19
3	VCCO	R18
3	VCCO	P18
4	VCCO	W18
4	VCCO	W17
4	VCCO	W16
4	VCCO	W15
4	VCCO	V15
4	VCCO	V14
5	VCCO	W9
5	VCCO	W12
5	VCCO	W11
5	VCCO	W10
5	VCCO	V13
5	VCCO	V12
6	VCCO	V8
6	VCCO	U8
6	VCCO	T8
6	VCCO	R9
6	VCCO	R8
6	VCCO	P9
7	VCCO	N9
7	VCCO	M9
7	VCCO	M8
7	VCCO	L8

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
7	VCCO	K8
7	VCCO	J8
NA	GND	V25
NA	GND	V2
NA	GND	U17
NA	GND	U16
NA	GND	U15
NA	GND	U14
NA	GND	U13
NA	GND	U12
NA	GND	U11
NA	GND	U10
NA	GND	T17
NA	GND	T16
NA	GND	T15
NA	GND	T14
NA	GND	T13
NA	GND	T12
NA	GND	T11
NA	GND	T10
NA	GND	R17
NA	GND	R16
NA	GND	R15
NA	GND	R14
NA	GND	R13
NA	GND	R12
NA	GND	R11
NA	GND	R10
NA	GND	P25
NA	GND	P17
NA	GND	P16
NA	GND	P15
NA	GND	P14
NA	GND	P13

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF
120	5	AD11	Y12	√	-
121	5	AB11	AD10	NA	-
122	5	AC11	AE10	√	-
123	5	AC10	AA11	√	-
124	5	Y11	AD9	NA	-
125	5	AB10	AF9	√	-
126	5	AD8	AA10	√	VREF
127	5	AE8	Y10	√	-
128	5	AC9	AF8	NA	-
129	5	AF7	AB9	NA	-
130	5	AA9	AF6	√	-
131	5	AC8	AC7	√	VREF
132	5	AD6	Y9	√	-
133	5	AE5	AA8	√	-
134	5	AC6	AB8	√	VREF
135	5	AD5	AA7	√	-
136	5	AF4	AC5	NA	-
137	6	AC3	AA5	√	-
138	6	AB4	AC2	√	-
139	6	AA4	W6	NA	-
140	6	Y5	AB3	NA	VREF
141	6	V7	AB2	NA	-
142	6	Y4	AB1	√	-
143	6	W5	V5	√	VREF
144	6	V6	AA1	√	-
145	6	Y3	W4	NA	-
146	6	U7	Y1	NA	-
147	6	V4	W1	√	-
148	6	U6	W2	√	VREF
149	6	T5	V3	√	-
150	6	U4	U5	√	-
151	6	U3	T7	NA	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
152	6	T6	U2	NA	-
153	6	T4	U1	NA	-
154	6	T3	R7	NA	-
155	6	R6	R4	√	VREF
156	6	R5	R3	√	-
157	6	P7	P8	NA	-
158	6	P6	R1	NA	VREF
159	6	P4	P5	√	-
160	7	N8	N5	√	-
161	7	N3	N6	√	-
162	7	M2	N4	NA	VREF
163	7	M7	N7	NA	-
164	7	M3	M6	√	-
165	7	M5	M4	√	VREF
166	7	L7	L3	NA	-
167	7	K2	L6	NA	-
168	7	K1	L4	NA	-
169	7	L5	K3	NA	-
170	7	J3	K5	√	-
171	7	J4	K4	√	-
172	7	K6	H3	√	VREF
173	7	G3	K7	√	-
174	7	H1	J5	NA	-
175	7	J6	G2	NA	-
176	7	F1	J7	√	-
177	7	G4	H4	√	VREF
178	7	H5	F3	NA	-
179	7	H6	E2	NA	-
180	7	F4	G5	NA	VREF
181	7	G6	H7	NA	-
182	7	E4	E3	√	-

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
0	IO_L29N	D14
0	IO_L29P	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_LVDS_DLL_L34N	A15
1	GCk2	E15
1	IO	B18
1	IO	B21
1	IO	B28
1	IO	C23
1	IO	C26
1	IO	D20
1	IO	D23
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N	B16
1	IO_L35P	F16
1	IO_L36N	A16
1	IO_L36P	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N	A17
1	IO_L39P	E17
1	IO_L40N	F17
1	IO_L40P	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N	B19

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
1	IO_L43P	G18
1	IO_L44N	D19
1	IO_L44P	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N	H19
1	IO_L53P	B22
1	IO_L54N	E21
1	IO_L54P	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N	G21
1	IO_L57P	A23
1	IO_L58N	A24
1	IO_L58P	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N	E23
1	IO_L61P	C25
1	IO_L62N	D24

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
3	IO_L131P_YY	Y22
3	IO_VREF_L131N_YY	AC27
3	IO_L132P	AD28
3	IO_L132N	AB25
3	IO_L133P	AC26
3	IO_L133N	AE30
3	IO_L134P_YY	AD27
3	IO_L134N_YY	AF30
3	IO_L135P_Y	AF29
3	IO_VREF_L135N_Y	AB24
3	IO_L136P	AB23
3	IO_L136N	AE28
3	IO_L138P	AE26
3	IO_L138N	AG29
3	IO_L139P_Y	AH30
3	IO_L139N_Y	AC24
3	IO_D7_L141P_YY	AH29
3	IO_INIT_L141N_YY	AA22
4	GCK0	AJ16
4	IO	AB19
4	IO	AC16
4	IO	AC19
4	IO	AD19
4	IO	AD20
4	IO	AE21
4	IO	AF19
4	IO	AH17
4	IO	AH23
4	IO	AH26
4	IO	AH27
4	IO	AK18
4	IO_VREF_4	AA18
4	IO_L142P_YY	AF27

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
4	IO_L142N_YY	AK28
4	IO_L144P_Y	AD23
4	IO_L144N_Y	AJ27
4	IO_L145P_Y	AB21
4	IO_L145N_Y	AF25
4	IO_L147P_YY	AA21
4	IO_L147N_YY	AG25
4	IO_VREF_4_L148P_YY	AJ26
4	IO_L148N_YY	AD22
4	IO_L149P	AA20
4	IO_L149N	AH25
4	IO_L150P	AC21
4	IO_L150N	AF24
4	IO_L151P_YY	AG24
4	IO_L151N_YY	AK26
4	IO_VREF_4_L152P_YY	AJ24
4	IO_L152N_YY	AF23
4	IO_L153P	AE23
4	IO_L153N	AB20
4	IO_L154P	AC20
4	IO_L154N	AG23
4	IO_L155P_YY	AF22
4	IO_L155N_YY	AE22
4	IO_VREF_4_L156P_YY	AJ22
4	IO_L156N_YY	AG22
4	IO_L158P	AA19
4	IO_L158N	AF21
4	IO_L160P	AG21
4	IO_L160N	AK23
4	IO_L162P_Y	AE20
4	IO_L162N_Y	AJ21
4	IO_L163P_Y	AG20
4	IO_L163N_Y	AF20
4	IO_L165P_YY	AJ20