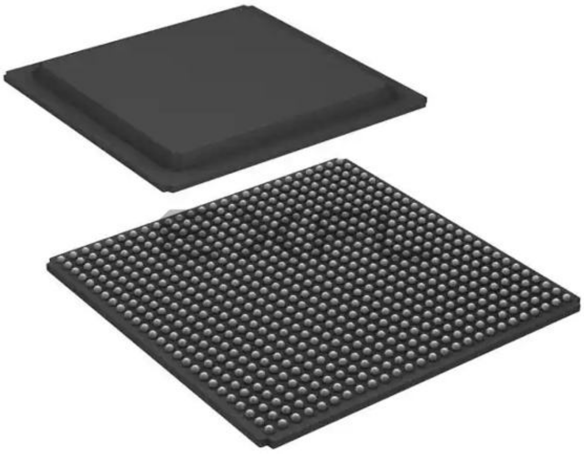

Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2400 |
| Number of Logic Elements/Cells | 10800 |
| Total RAM Bits | 573440 |
| Number of I/O | 404 |
| Number of Gates | 129600 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcv405e-6fg676c |

*Table 1:* **Virtex-E Extended Memory Field-Programmable Gate Array Family Members**

| Device | Logic Gates | CLB Array | Logic Cells | Differential I/O Pairs | User I/O | BlockRAM Bits | Distributed RAM Bits |
|---|---|---|---|---|---|---|---|
| XCV405E | 129,600 | 40 x 60 | 10,800 | 183 | 404 | 573,440 | 153,600 |
| XCV812E | 254,016 | 56 x 84 | 21,168 | 201 | 556 | 1,146,880 | 301,056 |

## Virtex-E Compared to Virtex Devices

The Virtex-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectI/O technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250MHz) block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

$V_{CCINT}$, the supply voltage for the internal logic and memory, is 1.8 V, instead of 2.5 V for Virtex devices. Advanced processing and 0.18 µm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3 V tolerant, and can be 5 V tolerant with an external 100 Ω resistor. PCI 5 V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by $V_{CCINT}$. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage $V_{CCO}$.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

## General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 µm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

## Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex-E family to accommodate even the largest and most complex designs.

Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Configuration data can be read from an external SPROM (master serial mode), or can be written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation Series™ and Alliance Series™ Development systems deliver complete design support for Virtex-E, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation and downloading of a configuration bit stream.

### Higher Performance

Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architectures. Virtex-E I/Os comply fully with 3.3 V PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz.

While performance is design-dependent, many designs operate internally at speeds in excess of 133 MHz and can achieve over 311 MHz. Table 2, page 3, shows performance data for representative circuits, using worst-case timing parameters.

# Virtex™-E 1.8 V Extended Memory Field Programmable Gate Arrays

DS025-2 (v2.3) November 19, 2002

**Production Product Specification**

## Architectural Description

### Virtex-E Array

The Virtex-E user-programmable gate array (see Figure 1) comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic.
- IOBs provide the interface between the package pins and the CLBs.

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex-E architecture also includes the following circuits that connect to the GRM:

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

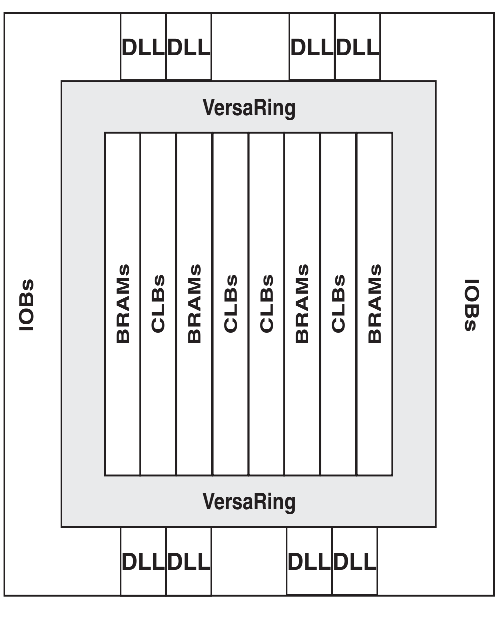


*Figure 1:* **Virtex-E Architecture Overview**

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

### Input/Output Block

The Virtex-E IOB, Figure 2, features SelectIO+™ inputs and outputs that support a wide variety of I/O signalling standards (see Table 1).

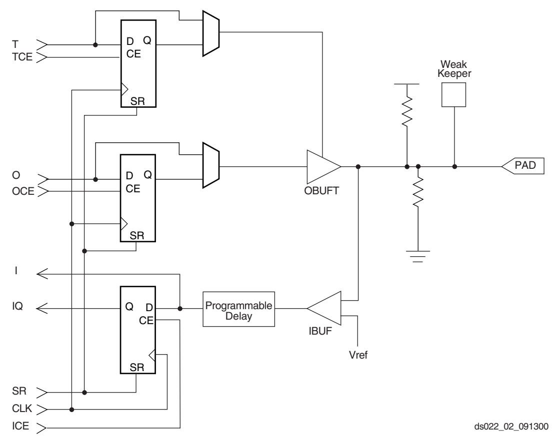


*Figure 2:* **Virtex-E Input/Output Block (IOB)**

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

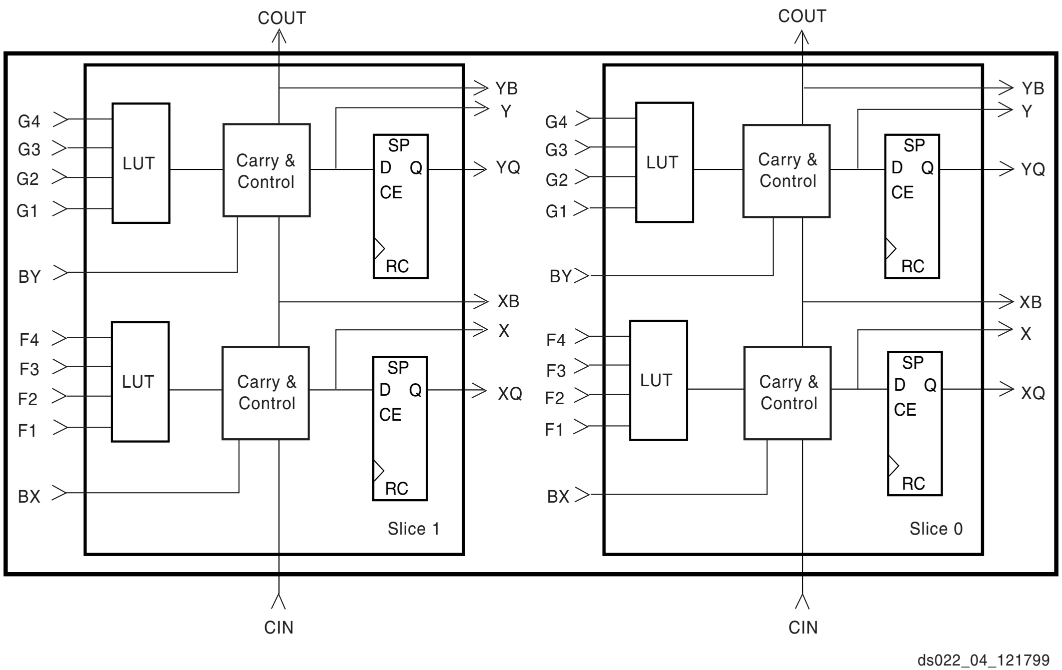


*Figure 4:* **2-Slice Virtex-E CLB**

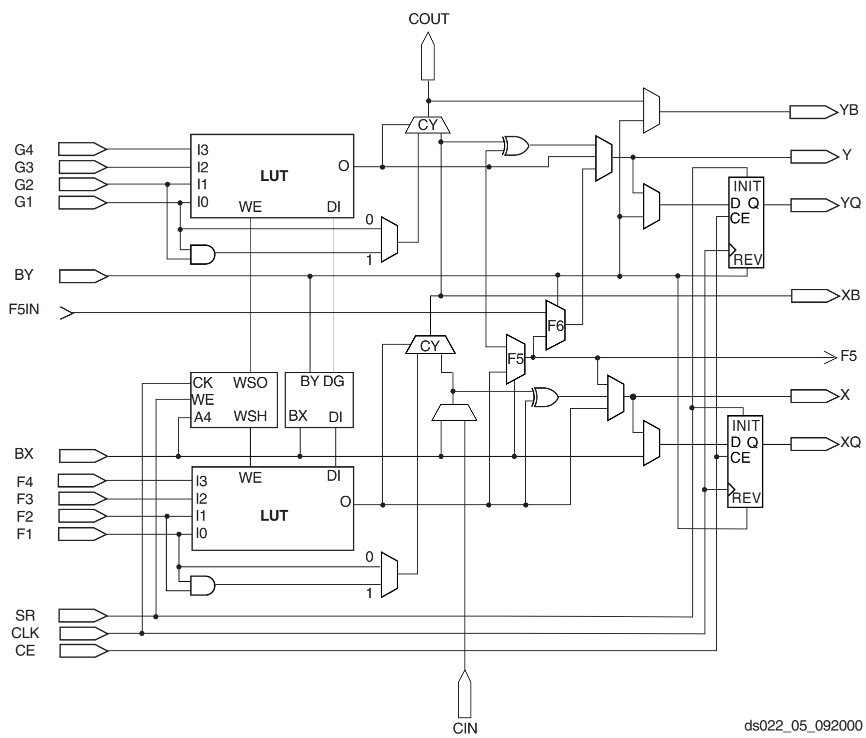


*Figure 5:* **Detailed View of Virtex-E Slice**

In addition to the four basic LCs, the Virtex-E CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

### *Look-Up Tables*

Virtex-E function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be com-

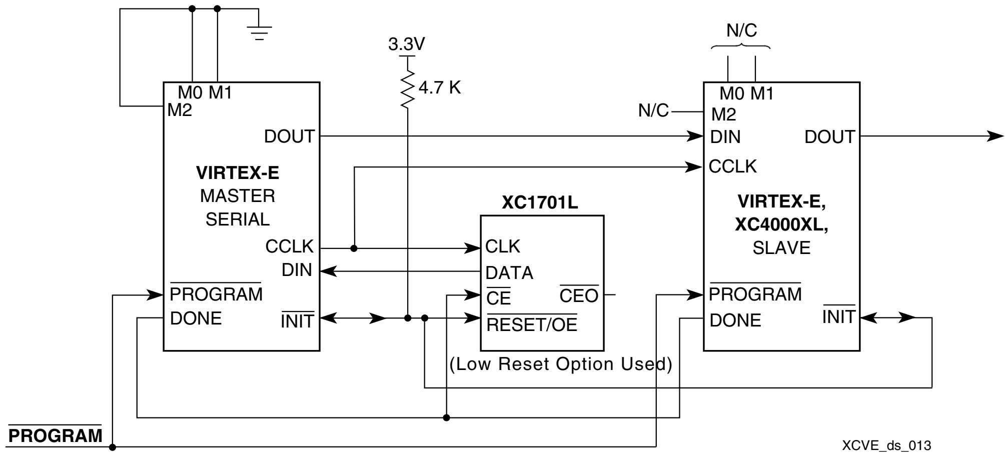


*Figure 13:* **Master/Slave Serial Mode Circuit Diagram**

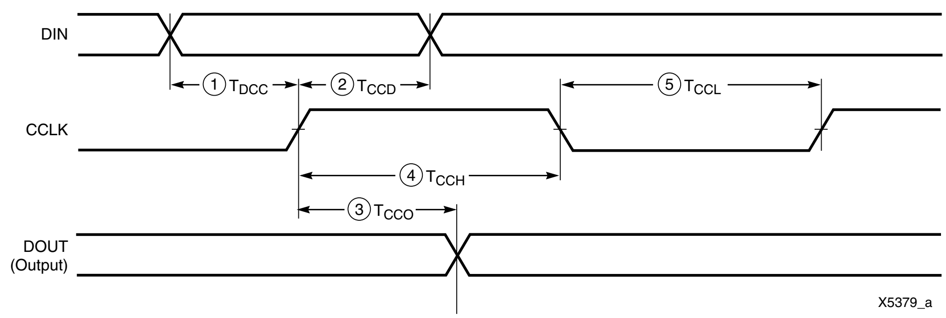


*Figure 14:* **Slave-Serial Mode Programming Switching Characteristics**

### *Master-Serial Mode*

In master-serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave-serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 13 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

## Port Signals

Each block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 15 describes the depth and width aspect ratios for the block SelectRAM+ memory.

*Table 15:* **Block SelectRAM+ Port Aspect Ratios**

| Width | Depth | ADDR Bus | Data Bus |
|---|---|---|---|
| 1 | 4096 | ADDR<11:0> | DATA<0> |
| 2 | 2048 | ADDR<10:0> | DATA<1:0> |
| 4 | 1024 | ADDR<9:0> | DATA<3:0> |
| 8 | 512 | ADDR<8:0> | DATA<7:0> |
| 16 | 256 | ADDR<7:0> | DATA<15:0> |

### *Clock—CLK[A|B]*

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

### *Enable—EN[A|B]*

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

### *Write Enable—WE[A|B]*

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

### *Reset—RST[A|B]*

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

### *Address Bus—ADDR[A|B]<#:0>*

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 15.

### *Data In Bus—DI[A|B]<#:0>*

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 15.

### *Data Output Bus—DO[A|B]<#:0>*

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 15.

## Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

## Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ((\text{ADDR}_{port} + 1) * \text{Width}_{port}) - 1$$

$$\text{End} = \text{ADDR}_{port} * \text{Width}_{port}$$

Table 16 shows low order address mapping for each port width.

*Table 16:* **Port Address Mapping**

<table>
<tr><th>Port Width</th><th colspan="17">Port Addresses</th></tr>
<tr><td>1</td><td>4095...</td><td>15</td><td>14</td><td>13</td><td>12</td><td>11</td><td>10</td><td>09</td><td>08</td><td>07</td><td>06</td><td>05</td><td>04</td><td>03</td><td>02</td><td>01</td><td>00</td></tr>
<tr><td>2</td><td>2047...</td><td colspan="2">07</td><td colspan="2">06</td><td colspan="2">05</td><td colspan="2">04</td><td colspan="2">03</td><td colspan="2">02</td><td colspan="2">01</td><td colspan="2">00</td></tr>
<tr><td>4</td><td>1023...</td><td colspan="4">03</td><td colspan="4">02</td><td colspan="4">01</td><td colspan="4">00</td></tr>
<tr><td>8</td><td>511...</td><td colspan="8">01</td><td colspan="8">00</td></tr>
<tr><td>16</td><td>255...</td><td colspan="16">00</td></tr>
</table>

## Creating Larger RAM Structures

The block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

## Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

## Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 18, each buffer type can support a variety of voltage requirements.

*Table 18:* **Virtex-E Supported I/O Standards**

| I/O Standard | Output $V_{CCO}$ | Input $V_{CCO}$ | Input $V_{REF}$ | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|---|
| LVTTL | 3.3 | 3.3 | N/A | N/A |
| LVCMOS2 | 2.5 | 2.5 | N/A | N/A |
| LVCMOS18 | 1.8 | 1.8 | N/A | N/A |
| SSTL3 I & II | 3.3 | N/A | 1.50 | 1.50 |
| SSTL2 I & II | 2.5 | N/A | 1.25 | 1.25 |
| GTL | N/A | N/A | 0.80 | 1.20 |
| GTL+ | N/A | N/A | 1.0 | 1.50 |
| HSTL I | 1.5 | N/A | 0.75 | 0.75 |
| HSTL III & IV | 1.5 | N/A | 0.90 | 1.50 |
| CTT | 3.3 | N/A | 1.50 | 1.50 |
| AGP-2X | 3.3 | N/A | 1.32 | N/A |
| PCI33_3 | 3.3 | 3.3 | N/A | N/A |
| PCI66_3 | 3.3 | 3.3 | N/A | N/A |
| BLVDS & LVDS | 2.5 | N/A | N/A | N/A |
| LVPECL | 3.3 | N/A | N/A | N/A |

## Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

http://www.jedec.org

### *LVTTL — Low-Voltage TTL*

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3 V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3 V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a termination voltage ($V_{TT}$).

### *LVCMOS2 — Low-Voltage CMOS for 2.5 Volts*

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5 V applications. This standard requires a 2.5 V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$).

### *LVCMOS18 — 1.8 V Low Voltage CMOS*

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$) is not required.

### *PCI — Peripheral Component Interface*

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$), however, it does require a 3.3 V output source voltage ($V_{CCO}$).

### *GTL — Gunning Transceiver Logic Terminated*

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

### *GTL+ — Gunning Transceiver Logic Plus*

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

### *HSTL — High-Speed Transceiver Logic*

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5 V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input. After placing a differential amplifier input signal within a given $V_{REF}$ bank, the same external source must drive all I/O pins configured as a $V_{REF}$ input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

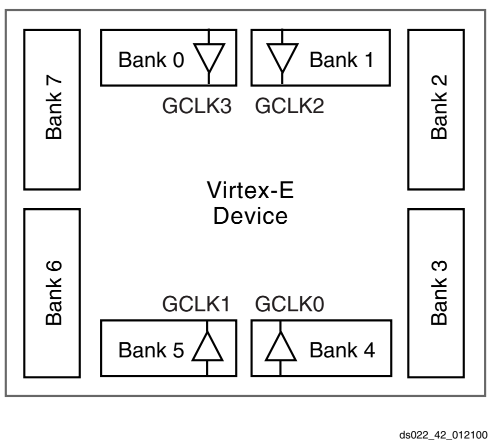


*Figure 38:* **Virtex-E I/O Banks**

*Table 19:* **Xilinx Input Standards Compatibility Requirements**

| | |
|---|---|
| Rule 1 | Standards with the same input $V_{CCO}$, output $V_{CCO}$, and $V_{REF}$ can be placed within the same bank. |

### *IBUFG*

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

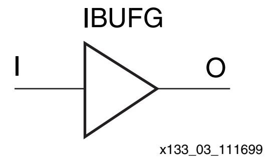


*Figure 39:* **Virtex-E Global Clock Input Buffer (IBUFG) Symbol**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input $V_{REF}$.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent $V_{REF}$ banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a $V_{REF}$ input. After placing a differential amplifier input signal within a given $V_{REF}$ bank, the same external source must drive all I/O pins configured as a $V_{REF}$ input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

Input termination techniques include the following:

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

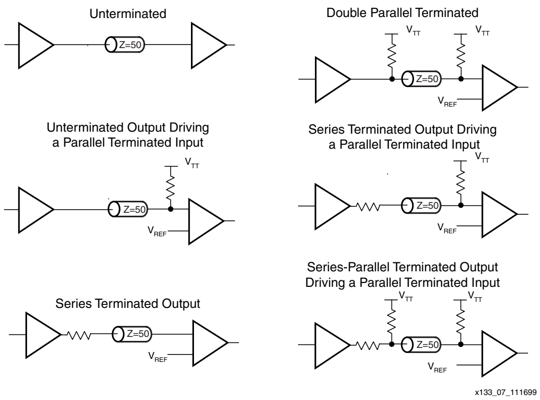


*Figure 43:* **Overview of Standard Input and Output Termination Methods**

### *Simultaneous Switching Guidelines*

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

*Table 21:* **Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

| Standard | Package |
|---|---|
| | **BGA, FGA** |
| LVTTL Slow Slew Rate, 2 mA drive | 68 |
| LVTTL Slow Slew Rate, 4 mA drive | 41 |
| LVTTL Slow Slew Rate, 6 mA drive | 29 |
| LVTTL Slow Slew Rate, 8 mA drive | 22 |
| LVTTL Slow Slew Rate, 12 mA drive | 17 |
| LVTTL Slow Slew Rate, 16 mA drive | 14 |
| LVTTL Slow Slew Rate, 24 mA drive | 9 |
| LVTTL Fast Slew Rate, 2 mA drive | 40 |
| LVTTL Fast Slew Rate, 4 mA drive | 24 |
| LVTTL Fast Slew Rate, 6 mA drive | 17 |
| LVTTL Fast Slew Rate, 8 mA drive | 13 |
| LVTTL Fast Slew Rate, 12 mA drive | 10 |
| LVTTL Fast Slew Rate, 16 mA drive | 8 |
| LVTTL Fast Slew Rate, 24 mA drive | 5 |
| LVCMOS | 10 |
| PCI | 8 |
| GTL | 4 |
| GTL+ | 4 |
| HSTL Class I | 18 |
| HSTL Class III | 9 |
| HSTL Class IV | 5 |
| SSTL2 Class I | 15 |
| SSTL2 Class II | 10 |
| SSTL3 Class I | 11 |
| SSTL3 Class II | 7 |
| CTT | 14 |
| AGP | 9 |

Note: This analysis assumes a 35 pF load for each output.

*Table 22:* **Virtex-E Extended Memory Family Equivalent Power/Ground Pairs**

| Pkg/Part | XCV405E | XCV812E |
|---|---|---|
| BG560 | | 56 |
| FG676 | 56 | |
| FG900 | | |

### *LVTTL*

LVTTL requires no termination. DC voltage specifications appears in Table 34.

*Table 34:* **LVTTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 2.0 | - | 3.6 |
| $V_{IL}$ | –0.5 | - | 0.8 |
| $V_{OH}$ | 2.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –24 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 24 | - | - |

Note: $V_{OL}$ and $V_{OH}$ for lower drive currents sample tested.

### *LVCMOS2*

LVCMOS2 requires no termination. DC voltage specifications appear in Table 35.

*Table 35:* **LVCMOS2 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 1.7 | - | 3.6 |
| $V_{IL}$ | –0.5 | - | 0.7 |
| $V_{OH}$ | 1.9 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –12 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 12 | - | - |

### *LVCMOS18*

LVCMOS18 does not require termination. Table 36 lists DC voltage specifications.

*Table 36:* **LVCMOS18 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 1.70 | 1.80 | 1.90 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH}$ | 0.65 x $V_{CCO}$ | - | 1.95 |
| $V_{IL}$ | – 0.5 | - | 0.2 x $V_{CCO}$ |
| $V_{OH}$ | $V_{CCO}$ – 0.4 | - | - |
| $V_{OL}$ | - | - | 0.4 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | 8 | - | - |

### *AGP-2X*

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 37.

*Table 37:* **AGP-2X Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF} = N \times V_{CCO}^{(1)}$ | 1.17 | 1.32 | 1.48 |
| $V_{TT}$ | - | - | - |
| $V_{IH} = V_{REF} + 0.2$ | 1.37 | 1.52 | - |
| $V_{IL} = V_{REF} - 0.2$ | - | 1.12 | 1.28 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | 3.0 | - |
| $V_{OL} = 0.1 \times V_{CCO}$ | - | 0.33 | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 2 | - | - |
| $I_{OL}$ at $V_{OL}$ (mA) | Note 2 | - | - |

**Notes:**

1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

## IOB Input Switching Characteristics Standard Adjustments

| | | | Speed Grade[1] | | | | |
|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **Standard** | **Min** | **-8** | **-7** | **-6** | **Units** |
| **Data Input Delay Adjustments** | | | | | | | |
| Standard-specific data input delay adjustments | $T_{ILVTTL}$ | LVTTL | 0.0 | 0.0 | 0.0 | 0.0 | ns |
| | $T_{ILVCMOS2}$ | LVCMOS2 | –0.02 | 0.0 | 0.0 | 0.0 | ns |
| | $T_{ILVCMOS18}$ | LVCMOS18 | –0.02 | +0.20 | +0.20 | +0.20 | ns |
| | $T_{ILVDS}$ | LVDS | 0.00 | +0.15 | +0.15 | +0.15 | ns |
| | $T_{ILVPECL}$ | LVPECL | 0.00 | +0.15 | +0.15 | +0.15 | ns |
| | $T_{IPCI33\_3}$ | PCI, 33 MHz, 3.3 V | –0.05 | +0.08 | +0.08 | +0.08 | ns |
| | $T_{IPCI66\_3}$ | PCI, 66 MHz, 3.3 V | –0.05 | –0.11 | –0.11 | –0.11 | ns |
| | $T_{IGTL}$ | GTL | +0.10 | +0.14 | +0.14 | +0.14 | ns |
| | $T_{IGTLPLUS}$ | GTL+ | +0.06 | +0.14 | +0.14 | +0.14 | ns |
| | $T_{IHSTL}$ | HSTL | +0.02 | +0.04 | +0.04 | +0.04 | ns |
| | $T_{ISSTL2}$ | SSTL2 | –0.04 | +0.04 | +0.04 | +0.04 | ns |
| | $T_{ISSTL3}$ | SSTL3 | –0.02 | +0.04 | +0.04 | +0.04 | ns |
| | $T_{ICTT}$ | CTT | +0.01 | +0.10 | +0.10 | +0.10 | ns |
| | $T_{IAGP}$ | AGP | –0.03 | +0.04 | +0.04 | +0.04 | ns |

**Notes:**
1. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

I

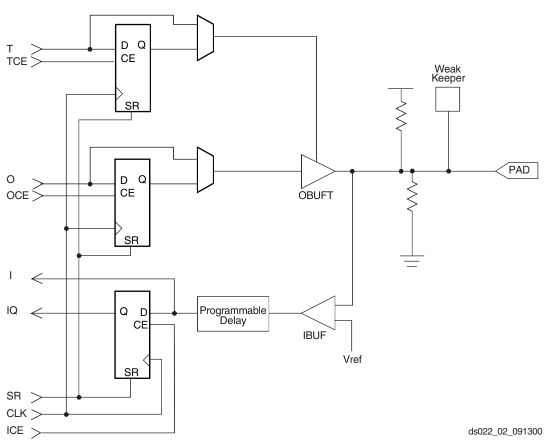


*Figure 1:* **Virtex-E Input/Output Block (IOB)**

## IOB Output Switching Characteristics, Figure 1

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8..

| | | Speed Grade(2) | | | | |
|---|---|---|---|---|---|---|
| **Description(1)** | **Symbol** | **Min3** | **-8** | **-7** | **-6** | **Units** |
| **Propagation Delays** | | | | | | |
| O input to Pad | $T_{IOOP}$ | 1.04 | 2.5 | 2.7 | 2.9 | ns, max |
| O input to Pad via transparent latch | $T_{IOOLP}$ | 1.24 | 2.9 | 3.1 | 3.4 | ns, max |
| **3-State Delays** | | | | | | |
| T input to Pad high-impedance (Note 2) | $T_{IOTHZ}$ | 0.73 | 1.5 | 1.7 | 1.9 | ns, max |
| T input to valid data on Pad | $T_{IOTON}$ | 1.13 | 2.7 | 2.9 | 3.1 | ns, max |
| T input to Pad high-impedance via transparent latch (Note 2) | $T_{IOTLPHZ}$ | 0.86 | 1.8 | 2.0 | 2.2 | ns, max |
| T input to valid data on Pad via transparent latch | $T_{IOTLPON}$ | 1.26 | 3.0 | 3.2 | 3.4 | ns, max |
| GTS to Pad high impedance (Note 2) | $T_{GTS}$ | 1.94 | 4.1 | 4.6 | 4.9 | ns, max |
| **Sequential Delays** | | | | | | |
| **Clock CLK** | | | | | | |
| Minimum Pulse Width, High | $T_{CH}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| Minimum Pulse Width, Low | $T_{CL}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| Clock CLK to Pad | $T_{IOCKP}$ | 0.97 | 2.4 | 2.8 | 2.9 | ns, max |
| Clock CLK to Pad high-impedance (synchronous) (Note 2) | $T_{IOCKHZ}$ | 0.77 | 1.6 | 2.0 | 2.2 | ns, max |
| Clock CLK to valid data on Pad (synchronous) | $T_{IOCKON}$ | 1.17 | 2.8 | 3.2 | 3.4 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| O input | $T_{IOOCK}$ / $T_{IOCKO}$ | 0.43 / 0 | 0.9 / 0 | 1.0 / 0 | 1.1 / 0 | ns, min |
| OCE input | $T_{IOOCECK}$ / $T_{IOCKOCE}$ | 0.28 / 0 | 0.55 / 0.01 | 0.7 / 0 | 0.7 / 0 | ns, min |
| SR input (OFF) | $T_{IOSRCKO}$ / $T_{IOCKOSR}$ | 0.40 / 0 | 0.8 / 0 | 0.9 / 0 | 1.0 / 0 | ns, min |
| **3-State Setup Times, T input** | $T_{IOTCK}$ / $T_{IOCKT}$ | 0.26 / 0 | 0.51 / 0 | 0.6 / 0 | 0.7 / 0 | ns, min |
| **3-State Setup Times, TCE input** | $T_{IOTCECK}$ / $T_{IOCKTCE}$ | 0.30 / 0 | 0.6 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| **3-State Setup Times, SR input (TFF)** | $T_{IOSRCKT}$ / $T_{IOCKTSR}$ | 0.38 / 0 | 0.8 / 0 | 0.9 / 0 | 1.0 / 0 | ns, min |
| **Set/Reset Delays** | | | | | | |
| SR input to Pad (asynchronous) | $T_{IOSRP}$ | 1.30 | 3.1 | 3.3 | 3.5 | ns, max |
| SR input to Pad high-impedance (asynchronous) (Note 2) | $T_{IOSRHZ}$ | 1.08 | 2.2 | 2.4 | 2.7 | ns, max |
| SR input to valid data on Pad (asynchronous) | $T_{IOSRON}$ | 1.48 | 3.4 | 3.7 | 3.9 | ns, max |
| GSR to Pad | $T_{IOGSRQ}$ | 3.88 | 7.6 | 8.5 | 9.7 | ns, max |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. 3-state turn-off delays should not be adjusted.

## CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 2. The values listed below are worst-case. Precise values are provided by the timing analyzer.

| Description[1] | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -8 | -7 | -6 | |
| **Combinatorial Delays** | | | | | | |
| 4-input function: F/G inputs to X/Y outputs | $T_{ILO}$ | 0.19 | 0.40 | 0.42 | 0.47 | ns, max |
| 5-input function: F/G inputs to F5 output | $T_{IF5}$ | 0.36 | 0.76 | 0.8 | 0.9 | ns, max |
| 5-input function: F/G inputs to X output | $T_{IF5X}$ | 0.35 | 0.74 | 0.8 | 0.9 | ns, max |
| 6-input function: F/G inputs to Y output via F6 MUX | $T_{IF6Y}$ | 0.35 | 0.74 | 0.9 | 1.0 | ns, max |
| 6-input function: F5IN input to Y output | $T_{F5INY}$ | 0.04 | 0.11 | 0.20 | 0.22 | ns, max |
| Incremental delay routing through transparent latch to XQ/YQ outputs | $T_{IFNCTL}$ | 0.27 | 0.63 | 0.7 | 0.8 | ns, max |
| BY input to YB output | $T_{BYYB}$ | 0.19 | 0.38 | 0.46 | 0.51 | ns, max |
| **Sequential Delays** | | | | | | |
| FF Clock CLK to XQ/YQ outputs | $T_{CKO}$ | 0.34 | 0.78 | 0.9 | 1.0 | ns, max |
| Latch Clock CLK to XQ/YQ outputs | $T_{CKLO}$ | 0.40 | 0.77 | 0.9 | 1.0 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| 4-input function: F/G Inputs | $T_{ICK}$ / $T_{CKI}$ | 0.39 / 0 | 0.9 / 0 | 1.0 / 0 | 1.1 / 0 | ns, min |
| 5-input function: F/G inputs | $T_{IF5CK}$ / $T_{CKIF5}$ | 0.55 / 0 | 1.3 / 0 | 1.4 / 0 | 1.5 / 0 | ns, min |
| 6-input function: F5IN input | $T_{F5INCK}$ / $T_{CKF5IN}$ | 0.27 / 0 | 0.6 / 0 | 0.8 / 0 | 0.8 / 0 | ns, min |
| 6-input function: F/G inputs via F6 MUX | $T_{IF6CK}$ / $T_{CKIF6}$ | 0.58 / 0 | 1.3 / 0 | 1.5 / 0 | 1.6 / 0 | ns, min |
| BX/BY inputs | $T_{DICK}$ / $T_{CKDI}$ | 0.25 / 0 | 0.6 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| CE input | $T_{CECK}$ / $T_{CKCE}$ | 0.28 / 0 | 0.55 / 0 | 0.7 / 0 | 0.7 / 0 | ns, min |
| SR/BY inputs (synchronous) | $T_{RCK}$ / $T_{CKR}$ | 0.24 / 0 | 0.46 / 0 | 0.52 / 0 | 0.6 / 0 | ns, min |
| **Clock CLK** | | | | | | |
| Minimum Pulse Width, High | $T_{CH}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| Minimum Pulse Width, Low | $T_{CL}$ | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| **Set/Reset** | | | | | | |
| Minimum Pulse Width, SR/BY inputs | $T_{RPW}$ | 0.94 | 1.9 | 2.1 | 2.4 | ns, min |
| Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) | $T_{RQ}$ | 0.39 | 0.8 | 0.9 | 1.0 | ns, max |
| Toggle Frequency (MHz) (for export control) | $F_{TOG}$ | - | 416 | 400 | 357 | MHz |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

| Description(1) | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -8 | -7 | -6 | |
| **Combinatorial Delays** | | | | | | |
| F operand inputs to X via XOR | $T_{OPX}$ | 0.32 | 0.68 | 0.8 | 0.8 | ns, max |
| F operand input to XB output | $T_{OPXB}$ | 0.35 | 0.65 | 0.8 | 0.9 | ns, max |
| F operand input to Y via XOR | $T_{OPY}$ | 0.59 | 1.07 | 1.4 | 1.5 | ns, max |
| F operand input to YB output | $T_{OPYB}$ | 0.48 | 0.89 | 1.1 | 1.3 | ns, max |
| F operand input to COUT output | $T_{OPCYF}$ | 0.37 | 0.71 | 0.9 | 1.0 | ns, max |
| G operand inputs to Y via XOR | $T_{OPGY}$ | 0.34 | 0.72 | 0.8 | 0.9 | ns, max |
| G operand input to YB output | $T_{OPGYB}$ | 0.47 | 0.78 | 1.2 | 1.3 | ns, max |
| G operand input to COUT output | $T_{OPCYG}$ | 0.36 | 0.60 | 0.9 | 1.0 | ns, max |
| BX initialization input to COUT | $T_{BXCY}$ | 0.19 | 0.36 | 0.51 | 0.57 | ns, max |
| CIN input to X output via XOR | $T_{CINX}$ | 0.27 | 0.50 | 0.6 | 0.7 | ns, max |
| CIN input to XB | $T_{CINXB}$ | 0.02 | 0.04 | 0.07 | 0.08 | ns, max |
| CIN input to Y via XOR | $T_{CINY}$ | 0.26 | 0.45 | 0.7 | 0.7 | ns, max |
| CIN input to YB | $T_{CINYB}$ | 0.16 | 0.28 | 0.38 | 0.43 | ns, max |
| CIN input to COUT output | $T_{BYP}$ | 0.05 | 0.10 | 0.14 | 0.15 | ns, max |
| **Multiplier Operation** | | | | | | |
| F1/2 operand inputs to XB output via AND | $T_{FANDXB}$ | 0.10 | 0.30 | 0.35 | 0.39 | ns, max |
| F1/2 operand inputs to YB output via AND | $T_{FANDYB}$ | 0.28 | 0.56 | 0.7 | 0.8 | ns, max |
| F1/2 operand inputs to COUT output via AND | $T_{FANDCY}$ | 0.17 | 0.38 | 0.46 | 0.51 | ns, max |
| G1/2 operand inputs to YB output via AND | $T_{GANDYB}$ | 0.20 | 0.46 | 0.55 | 0.7 | ns, max |
| G1/2 operand inputs to COUT output via AND | $T_{GANDCY}$ | 0.09 | 0.28 | 0.30 | 0.34 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| CIN input to FFX | $T_{CCKX}/T_{CKCX}$ | 0.47 / 0 | 1.0 / 0 | 1.2 / 0 | 1.3 / 0 | ns, min |
| CIN input to FFY | $T_{CCKY}/T_{CKCY}$ | 0.49 / 0 | 0.92 / 0 | 1.2 / 0 | 1.3 / 0 | ns, min |

**Notes:**

1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

*Table 1:* **BG560 BGA — XCV405E and XCV812E**

| Bank | Pin Description | Pin# |
|---|---|---|
| 1 | IO_L27N_YY | C14 |
| 1 | IO_L27P_YY | D14 |
| 1 | IO_L28N_Y | A13 |
| 1 | IO_L28P_Y | E14 |
| 1 | IO_L29N_YY | C13 |
| 1 | IO_VREF_L29P_YY | D13[1] |
| 1 | IO_L30N_YY | C12 |
| 1 | IO_L30P_YY | E13 |
| 1 | IO_L31N | A11 |
| 1 | IO_L31P | D12 |
| 1 | IO_L32N_YY | B11 |
| 1 | IO_L32P_YY | C11 |
| 1 | IO_L33N_YY | B10 |
| 1 | IO_VREF_L33P_YY | D11 |
| 1 | IO_L34N | C10 |
| 1 | IO_L34P | A9 |
| 1 | IO_L35N_YY | C9 |
| 1 | IO_VREF_L35P_YY | D10[1] |
| 1 | IO_L36N_YY | A8 |
| 1 | IO_L36P_YY | B8 |
| 1 | IO_L37N_Y | E10 |
| 1 | IO_L37P_Y | C8 |
| 1 | IO_L38N_YY | B7 |
| 1 | IO_VREF_L38P_YY | A6 |
| 1 | IO_L39N_YY | C7 |
| 1 | IO_L39P_YY | D8 |
| 1 | IO_L40N | A5 |
| 1 | IO_L40P | B5 |
| 1 | IO_L41N_YY | C6 |
| 1 | IO_VREF_L41P_YY | D7 |
| 1 | IO_L42N_YY | A4 |
| 1 | IO_L42P_YY | B4 |
| 1 | IO_L43N_Y | C5 |
| 1 | IO_L43P_Y | E7 |
| 1 | IO_WRITE_L44N_YY | D6 |
| 1 | IO_CS_L44P_YY | A2 |
| | | |

*Table 1:* **BG560 BGA — XCV405E and XCV812E**

| Bank | Pin Description | Pin# |
|---|---|---|
| 2 | IO | D3 |
| 2 | IO | F3 |
| 2 | IO | G1 |
| 2 | IO | J2 |
| 2 | IO_DOUT_BUSY_L45P_YY | D4 |
| 2 | IO_DIN_D0_L45N_YY | E4 |
| 2 | IO_L46P_Y | F5 |
| 2 | IO_L46N_Y | B3 |
| 2 | IO_L47P | F4 |
| 2 | IO_L47N | C1 |
| 2 | IO_VREF_L48P_Y | G5 |
| 2 | IO_L48N_Y | E3 |
| 2 | IO_L49P_Y | D2 |
| 2 | IO_L49N_Y | G4 |
| 2 | IO_L50P_Y | H5 |
| 2 | IO_L50N_Y | E2 |
| 2 | IO_VREF_L51P_YY | H4 |
| 2 | IO_L51N_YY | G3 |
| 2 | IO_L52P_Y | J5 |
| 2 | IO_L52N_Y | F1 |
| 2 | IO_L53P | J4 |
| 2 | IO_L53N | H3 |
| 2 | IO_VREF_L54P_YY | K5[1] |
| 2 | IO_L54N_YY | H2 |
| 2 | IO_L55P_Y | J3 |
| 2 | IO_L55N_Y | K4 |
| 2 | IO_VREF_L56P_YY | L5 |
| 2 | IO_D1_L56N_YY | K3 |
| 2 | IO_D2_L57P_YY | L4 |
| 2 | IO_L57N_YY | K2 |
| 2 | IO_L58P_Y | M5 |
| 2 | IO_L58N_Y | L3 |
| 2 | IO_L59P | L1 |
| 2 | IO_L59N | M4 |
| 2 | IO_VREF_L60P_Y | N5[1] |
| 2 | IO_L60N_Y | M2 |
| 2 | IO_L61P_Y | N4 |

## BG560 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 2:* **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| Global Differential Clock | | | | | |
| 3 | 0 | A17 | C18 | NA | IO LVDS 21 |
| 2 | 1 | D17 | E17 | NA | IO LVDS 21 |
| 1 | 5 | AJ17 | AM18 | NA | IO LVDS 115 |
| 0 | 4 | AL17 | AM17 | NA | IO LVDS 115 |
| IO LVDS<br>Total Outputs: 183, Asyncronous Outputs: 79 | | | | | |
| 0 | 0 | D29 | E28 | NA | - |
| 1 | 0 | A31 | D28 | √ | - |
| 2 | 0 | C29 | E27 | √ | VREF_0 |
| 3 | 0 | D27 | B30 | 1 | - |
| 4 | 0 | B29 | E26 | √ | - |
| 5 | 0 | C27 | D26 | √ | VREF_0 |
| 6 | 0 | A28 | E25 | NA | - |
| 7 | 0 | C26 | D25 | 1 | - |
| 8 | 0 | B26 | E24 | 1 | VREF_0 |
| 9 | 0 | D24 | C25 | 1 | - |
| 10 | 0 | A25 | E23 | √ | VREF_0 |
| 11 | 0 | B24 | D23 | √ | - |
| 12 | 0 | C23 | E22 | NA | - |
| 13 | 0 | D22 | A23 | √ | - |
| 14 | 0 | B22 | E21 | √ | VREF_0 |
| 15 | 0 | C21 | D21 | 1 | - |
| 16 | 0 | E20 | B21 | √ | - |
| 17 | 0 | C20 | D20 | √ | VREF_0 |
| 18 | 0 | E19 | B20 | NA | - |
| 19 | 0 | C19 | D19 | 1 | - |
| 20 | 0 | D18 | A19 | 1 | VREF_0 |
| 21 | 1 | E17 | C18 | NA | GCLK LVDS 3/2 |
| 22 | 1 | B17 | C17 | 1 | - |
| 23 | 1 | D16 | B16 | 1 | VREF_1 |
| 24 | 1 | C16 | E16 | 1 | - |
| 25 | 1 | C15 | A15 | NA | - |
| 26 | 1 | E15 | D15 | √ | VREF_1 |
| 27 | 1 | D14 | C14 | √ | - |
| 28 | 1 | E14 | A13 | 1 | - |
| 29 | 1 | D13 | C13 | √ | VREF_1 |
| 30 | 1 | E13 | C12 | √ | - |
| 31 | 1 | D12 | A11 | NA | - |
| 32 | 1 | C11 | B11 | √ | - |
| 33 | 1 | D11 | B10 | √ | VREF_1 |
| 34 | 1 | A9 | C10 | 2 | - |
| 35 | 1 | D10 | C9 | 1 | VREF_1 |
| 36 | 1 | B8 | A8 | 1 | - |
| 37 | 1 | C8 | E10 | NA | - |
| 38 | 1 | A6 | B7 | √ | VREF_1 |
| 39 | 1 | D8 | C7 | √ | - |
| 40 | 1 | B5 | A5 | 2 | - |
| 41 | 1 | D7 | C6 | √ | VREF_1 |
| 42 | 1 | B4 | A4 | √ | - |
| 43 | 1 | E7 | C5 | NA | - |
| 44 | 1 | A2 | D6 | √ | CS |
| 45 | 2 | D4 | E4 | √ | DIN_D0 |
| 46 | 2 | F5 | B3 | 2 | - |
| 47 | 2 | F4 | C1 | NA | - |
| 48 | 2 | G5 | E3 | 1 | VREF_2 |
| 49 | 2 | D2 | G4 | 1 | - |

*Table 2:* **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

| | | | | | |
|---|---|---|---|---|---|
| 118 | 5 | AK19 | AM20 | NA | - |
| 119 | 5 | AJ19 | AL20 | √ | VREF_5 |
| 120 | 5 | AN21 | AL21 | √ | - |
| 121 | 5 | AJ20 | AM22 | 1 | - |
| 122 | 5 | AK21 | AN23 | √ | VREF_5 |
| 123 | 5 | AJ21 | AM23 | √ | - |
| 124 | 5 | AK22 | AM24 | NA | - |
| 125 | 5 | AL23 | AJ22 | √ | - |
| 126 | 5 | AK23 | AL24 | √ | VREF_5 |
| 127 | 5 | AN26 | AJ23 | 2 | - |
| 128 | 5 | AK24 | AM26 | 1 | VREF_5 |
| 129 | 5 | AM27 | AJ24 | 1 | - |
| 130 | 5 | AL26 | AK25 | NA | - |
| 131 | 5 | AN29 | AJ25 | √ | VREF_5 |
| 132 | 5 | AK26 | AM29 | √ | - |
| 133 | 5 | AM30 | AJ26 | 2 | - |
| 134 | 5 | AK27 | AL29 | √ | VREF_5 |
| 135 | 5 | AN31 | AJ27 | √ | - |
| 136 | 5 | AM31 | AK28 | NA | - |
| 137 | 6 | AJ30 | AH29 | √ | - |
| 138 | 6 | AH30 | AK31 | 2 | - |
| 139 | 6 | AJ31 | AG29 | NA | - |
| 140 | 6 | AG30 | AK32 | 1 | VREF_6 |
| 141 | 6 | AF29 | AH31 | 1 | - |
| 142 | 6 | AF30 | AH32 | NA | - |
| 143 | 6 | AH33 | AE29 | √ | VREF_6 |
| 144 | 6 | AE30 | AG33 | 2 | - |
| 145 | 6 | AF32 | AD29 | NA | - |
| 146 | 6 | AD30 | AE31 | NA | VREF_6 |
| 147 | 6 | AC29 | AE32 | NA | - |
| 148 | 6 | AC30 | AD31 | √ | VREF_6 |
| 149 | 6 | AC31 | AB29 | √ | - |
| 150 | 6 | AB30 | AC33 | 2 | - |
| 151 | 6 | AA29 | AB31 | NA | - |

*Table 2:* **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

| | | | | | |
|---|---|---|---|---|---|
| 152 | 6 | AA31 | AA30 | 1 | VREF_6 |
| 153 | 6 | Y29 | AA32 | 1 | - |
| 154 | 6 | Y30 | AA33 | NA | - |
| 155 | 6 | W29 | Y32 | √ | VREF_6 |
| 156 | 6 | W31 | W30 | 2 | - |
| 157 | 6 | V30 | W33 | NA | - |
| 158 | 6 | V31 | V29 | NA | VREF_6 |
| 159 | 6 | U33 | V32 | NA | - |
| 160 | 7 | U32 | U31 | √ | IRDY |
| 161 | 7 | T30 | T32 | NA | - |
| 162 | 7 | T31 | T29 | NA | VREF_7 |
| 163 | 7 | R31 | R33 | NA | - |
| 164 | 7 | R29 | R30 | 2 | - |
| 165 | 7 | P31 | P32 | √ | VREF_7 |
| 166 | 7 | P29 | P30 | NA | - |
| 167 | 7 | N31 | M32 | 1 | - |
| 168 | 7 | L33 | N30 | 1 | VREF_7 |
| 169 | 7 | L32 | M31 | NA | - |
| 170 | 7 | L31 | M30 | 2 | - |
| 171 | 7 | J33 | M29 | √ | - |
| 172 | 7 | K31 | L30 | √ | VREF_7 |
| 173 | 7 | H33 | L29 | 1 | - |
| 174 | 7 | H32 | J31 | NA | VREF_7 |
| 175 | 7 | H31 | K29 | NA | - |
| 176 | 7 | G32 | J30 | NA | - |
| 177 | 7 | G31 | J29 | √ | VREF_7 |
| 178 | 7 | E32 | E33 | NA | - |
| 179 | 7 | F31 | H29 | 2 | - |
| 180 | 7 | E31 | D32 | 1 | VREF_7 |
| 181 | 7 | C33 | G29 | NA | - |
| 182 | 7 | D31 | F30 | NA | - |

**Notes:**
1. AO in the XCV812E
2. AO in the XCV405E

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| NA | NC | B26 |
| NA | NC | B24 |
| NA | NC | B21 |
| NA | NC | B16 |
| NA | NC | B11 |
| NA | NC | B1 |
| NA | NC | AF25 |
| NA | NC | AF24 |
| NA | NC | AF2 |
| NA | NC | AE6 |
| NA | NC | AE3 |
| NA | NC | AE26 |
| NA | NC | AE24 |
| NA | NC | AE21 |
| NA | NC | AE16 |
| NA | NC | AE14 |
| NA | NC | AE11 |
| NA | NC | AE1 |
| NA | NC | AD25 |
| NA | NC | AD2 |
| NA | NC | AD1 |
| NA | NC | AA6 |
| NA | NC | AA25 |
| NA | NC | AA21 |
| NA | NC | AA2 |
| NA | NC | A3 |
| NA | NC | A25 |
| NA | NC | A2 |
| NA | NC | A15 |
| | | |
| NA | VCCINT | G7 |
| NA | VCCINT | G20 |
| NA | VCCINT | H8 |
| NA | VCCINT | H19 |
| NA | VCCINT | J9 |

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| NA | VCCINT | J10 |
| NA | VCCINT | J11 |
| NA | VCCINT | J16 |
| NA | VCCINT | J17 |
| NA | VCCINT | J18 |
| NA | VCCINT | K9 |
| NA | VCCINT | K18 |
| NA | VCCINT | L9 |
| NA | VCCINT | L18 |
| NA | VCCINT | T9 |
| NA | VCCINT | T18 |
| NA | VCCINT | U9 |
| NA | VCCINT | U18 |
| NA | VCCINT | V9 |
| NA | VCCINT | V10 |
| NA | VCCINT | V11 |
| NA | VCCINT | V16 |
| NA | VCCINT | V17 |
| NA | VCCINT | V18 |
| NA | VCCINT | Y7 |
| NA | VCCINT | Y20 |
| NA | VCCINT | W8 |
| NA | VCCINT | W19 |
| | | |
| 0 | VCCO | J13 |
| 0 | VCCO | J12 |
| 0 | VCCO | H9 |
| 0 | VCCO | H12 |
| 0 | VCCO | H11 |
| 0 | VCCO | H10 |
| 1 | VCCO | J15 |
| 1 | VCCO | J14 |
| 1 | VCCO | H18 |
| 1 | VCCO | H17 |
| 1 | VCCO | H16 |

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 1 | VCCO | H15 |
| 2 | VCCO | N18 |
| 2 | VCCO | M19 |
| 2 | VCCO | M18 |
| 2 | VCCO | L19 |
| 2 | VCCO | K19 |
| 2 | VCCO | J19 |
| 3 | VCCO | V19 |
| 3 | VCCO | U19 |
| 3 | VCCO | T19 |
| 3 | VCCO | R19 |
| 3 | VCCO | R18 |
| 3 | VCCO | P18 |
| 4 | VCCO | W18 |
| 4 | VCCO | W17 |
| 4 | VCCO | W16 |
| 4 | VCCO | W15 |
| 4 | VCCO | V15 |
| 4 | VCCO | V14 |
| 5 | VCCO | W9 |
| 5 | VCCO | W12 |
| 5 | VCCO | W11 |
| 5 | VCCO | W10 |
| 5 | VCCO | V13 |
| 5 | VCCO | V12 |
| 6 | VCCO | V8 |
| 6 | VCCO | U8 |
| 6 | VCCO | T8 |
| 6 | VCCO | R9 |
| 6 | VCCO | R8 |
| 6 | VCCO | P9 |
| 7 | VCCO | N9 |
| 7 | VCCO | M9 |
| 7 | VCCO | M8 |
| 7 | VCCO | L8 |

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 7 | VCCO | K8 |
| 7 | VCCO | J8 |
| | | |
| NA | GND | V25 |
| NA | GND | V2 |
| NA | GND | U17 |
| NA | GND | U16 |
| NA | GND | U15 |
| NA | GND | U14 |
| NA | GND | U13 |
| NA | GND | U12 |
| NA | GND | U11 |
| NA | GND | U10 |
| NA | GND | T17 |
| NA | GND | T16 |
| NA | GND | T15 |
| NA | GND | T14 |
| NA | GND | T13 |
| NA | GND | T12 |
| NA | GND | T11 |
| NA | GND | T10 |
| NA | GND | R17 |
| NA | GND | R16 |
| NA | GND | R15 |
| NA | GND | R14 |
| NA | GND | R13 |
| NA | GND | R12 |
| NA | GND | R11 |
| NA | GND | R10 |
| NA | GND | P25 |
| NA | GND | P17 |
| NA | GND | P16 |
| NA | GND | P15 |
| NA | GND | P14 |
| NA | GND | P13 |

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| NA | GND | P12 |
| NA | GND | P11 |
| NA | GND | P10 |
| NA | GND | N2 |
| NA | GND | N17 |
| NA | GND | N16 |
| NA | GND | N15 |
| NA | GND | N14 |
| NA | GND | N13 |
| NA | GND | N12 |
| NA | GND | N11 |
| NA | GND | N10 |
| NA | GND | M17 |
| NA | GND | M16 |
| NA | GND | M15 |
| NA | GND | M14 |
| NA | GND | M13 |
| NA | GND | M12 |
| NA | GND | M11 |
| NA | GND | M10 |
| NA | GND | L17 |
| NA | GND | L16 |
| NA | GND | L15 |
| NA | GND | L14 |
| NA | GND | L13 |
| NA | GND | L12 |
| NA | GND | L11 |
| NA | GND | L10 |
| NA | GND | K17 |
| NA | GND | K16 |
| NA | GND | K15 |
| NA | GND | K14 |
| NA | GND | K13 |
| NA | GND | K12 |
| NA | GND | K11 |

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| NA | GND | K10 |
| NA | GND | J25 |
| NA | GND | J2 |
| NA | GND | E5 |
| NA | GND | E22 |
| NA | GND | D4 |
| NA | GND | D23 |
| NA | GND | C3 |
| NA | GND | C24 |
| NA | GND | B9 |
| NA | GND | B25 |
| NA | GND | B2 |
| NA | GND | B18 |
| NA | GND | B14 |
| NA | GND | AF26 |
| NA | GND | AF1 |
| NA | GND | AE9 |
| NA | GND | AE25 |
| NA | GND | AE2 |
| NA | GND | AE18 |
| NA | GND | AE13 |
| NA | GND | AD3 |
| NA | GND | AD24 |
| NA | GND | AC4 |
| NA | GND | AC23 |
| NA | GND | AB5 |
| NA | GND | AB22 |
| NA | GND | A26 |
| NA | GND | A1 |

## FG676 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 4:* **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| Global Differential Clock | | | | | |
| 3 | 0 | E13 | B13 | NA | IO_DLL_L21N |
| 2 | 1 | C13 | F14 | NA | IO_DLL_L21P |
| 1 | 5 | AB13 | AF13 | NA | IO_DLL_L115N |
| 0 | 4 | AA14 | AC14 | NA | IO_DLL_L115P |
| IOLVDS<br>Total Pairs: 183, Asynchronous Output Pairs: 97 | | | | | |
| 0 | 0 | F7 | C4 | NA | - |
| 1 | 0 | C5 | G8 | √ | - |
| 2 | 0 | E7 | D6 | √ | VREF |
| 3 | 0 | F8 | A4 | NA | - |
| 4 | 0 | D7 | B5 | NA | - |
| 5 | 0 | G9 | E8 | √ | VREF |
| 6 | 0 | F9 | A5 | √ | - |
| 7 | 0 | C7 | D8 | NA | - |
| 8 | 0 | E9 | B7 | NA | - |
| 9 | 0 | D9 | A7 | NA | - |
| 10 | 0 | G10 | B8 | NA | VREF |
| 11 | 0 | F10 | C9 | √ | - |
| 12 | 0 | E10 | A8 | NA | - |
| 13 | 0 | D10 | G11 | √ | - |
| 14 | 0 | F11 | B10 | √ | - |
| 15 | 0 | E11 | C10 | NA | - |

*Table 4:* **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 16 | 0 | D11 | G12 | √ | - |
| 17 | 0 | F12 | C11 | √ | VREF |
| 18 | 0 | E12 | A11 | √ | - |
| 19 | 0 | C12 | D12 | NA | - |
| 20 | 0 | H13 | A12 | NA | VREF |
| 21 | 1 | F14 | B13 | NA | IO_LVDS_DLL |
| 22 | 1 | F13 | E14 | NA | - |
| 23 | 1 | A14 | D14 | NA | VREF |
| 24 | 1 | H14 | C14 | NA | - |
| 25 | 1 | C15 | G14 | √ | - |
| 26 | 1 | D15 | E15 | √ | VREF |
| 27 | 1 | F15 | C16 | √ | - |
| 28 | 1 | D16 | G15 | - | - |
| 29 | 1 | A17 | E16 | √ | - |
| 30 | 1 | E17 | C17 | √ | - |
| 31 | 1 | D17 | F16 | NA | - |
| 32 | 1 | C18 | F17 | √ | - |
| 33 | 1 | G16 | A18 | √ | VREF |
| 34 | 1 | G17 | C19 | √ | - |
| 35 | 1 | B19 | D18 | NA | - |
| 36 | 1 | E18 | D19 | NA | - |
| 37 | 1 | B20 | F18 | √ | - |
| 38 | 1 | C20 | G19 | √ | VREF |
| 39 | 1 | E19 | G18 | √ | - |
| 40 | 1 | D20 | A21 | √ | - |
| 41 | 1 | C21 | F19 | √ | VREF |
| 42 | 1 | E20 | B22 | √ | - |
| 43 | 1 | D21 | A23 | 2 | - |
| 44 | 1 | E21 | C22 | √ | CS |
| 45 | 2 | E23 | F22 | √ | DIN, D0 |
| 46 | 2 | E24 | F20 | √ | - |
| 47 | 2 | G21 | G22 | 2 | - |
| 48 | 2 | F24 | H20 | 1 | VREF |
| 49 | 2 | E25 | H21 | 1 | - |