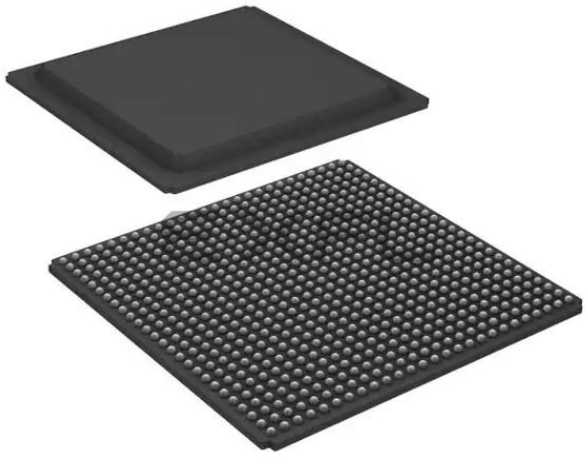

Welcome to E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 2400 |
| Number of Logic Elements/Cells | 10800 |
| Total RAM Bits | 573440 |
| Number of I/O | 404 |
| Number of Gates | 129600 |
| Voltage - Supply | 1.71V ~ 1.89V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 676-BGA |
| Supplier Device Package | 676-FBGA (27x27) |
| Purchase URL | https://www.e-xfl.com/product-detail/xilinx/xcv405e-6fg676i |

DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

For more information about DLL functionality, see the Design Consideration section of the data sheet.

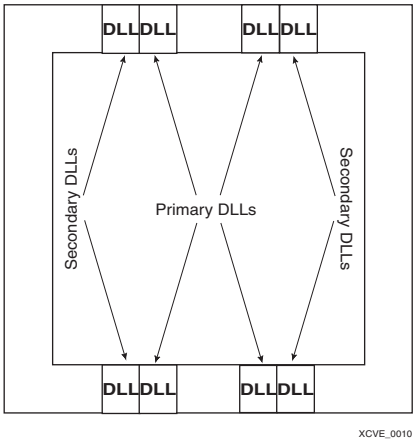


*Figure 10:* **DLL Locations**

## Boundary Scan

Virtex-E devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The JTAG input pins (TDI, TMS, TCK) do not have a $V_{CCO}$ requirement, and operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the $V_{CCO}$ in bank 2, and for proper operation of LVTTL 3.3 V levels, the bank should be supplied with 3.3 V.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 6 lists the boundary-scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

tions and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

## Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRCE® static timing analyzer.

For in-circuit debugging, an optional download and readback cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

# Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Note that attempting to load an incorrect bitstream causes configuration to fail and can damage the device.

Some of the pins used for configuration are dedicated pins, while others can be re-used as general purpose inputs and outputs once configuration is complete.

The following are dedicated pins:

- Mode pins (M2, M1, M0)
- Configuration clock pin (CCLK)
- $\overline{\text{PROGRAM}}$ pin
- DONE pin
- Boundary-scan pins (TDI, TDO, TMS, TCK)

Depending on the configuration mode chosen, CCLK can be an output generated by the FPGA, or it can be generated externally and provided to the FPGA as an input. The $\overline{\text{PROGRAM}}$ pin must be pulled High prior to reconfiguration.

Note that some configuration pins can act as outputs. For correct operation, these pins require a $V_{CCO}$ of 3.3 V to permit LVTTL operation. All of the pins affected are in banks 2 or 3. The configuration pins needed for SelectMap (CS, Write) are located in bank 1.

## Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected. However, it is recommended to drive the configuration mode pins externally.

*Table 8:* **Configuration Codes**

| Configuration Mode | M2 | M1 | M0 | CCLK Direction | Data Width | Serial $D_{out}$ | Configuration Pull-ups |
|---|---|---|---|---|---|---|---|
| Master-serial mode | 0 | 0 | 0 | Out | 1 | Yes | No |
| Boundary-scan mode | 1 | 0 | 1 | N/A | 1 | No | No |
| SelectMAP mode | 1 | 1 | 0 | In | 8 | No | No |
| Slave-serial mode | 1 | 1 | 1 | In | 1 | Yes | No |
| Master-serial mode | 1 | 0 | 0 | Out | 1 | Yes | Yes |

either asserted or de-asserted. Otherwise an abort is initiated, as described below.

2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while $\overline{CS}$ is Low and $\overline{WRITE}$ is High. Similarly, while $\overline{WRITE}$ is High, no more that one $\overline{CS}$ should be asserted.
3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance instead occurs on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

*Table 11:* **SelectMAP Write Timing Characteristics**

| | Description | | Symbol | Values | Units |
|---|---|---|---|---|---|
| CCLK | $D_{0-7}$ Setup/Hold | 1/2 | $T_{SMDCC}/T_{SMCCD}$ | 5.0 / 1.7 | ns, min |
| | $\overline{CS}$ Setup/Hold | 3/4 | $T_{SMCSCC}/T_{SMCCCS}$ | 7.0 / 1.7 | ns, min |
| | $\overline{WRITE}$ Setup/Hold | 5/6 | $T_{SMCCW}/T_{SMWCC}$ | 7.0 / 1.7 | ns, min |
| | BUSY Propagation Delay | 7 | $T_{SMCKBY}$ | 12.0 | ns, max |
| | Maximum Frequency | | $F_{CC}$ | 66 | MHz, max |
| | Maximum Frequency with no handshake | | $F_{CCNH}$ | 50 | MHz, max |

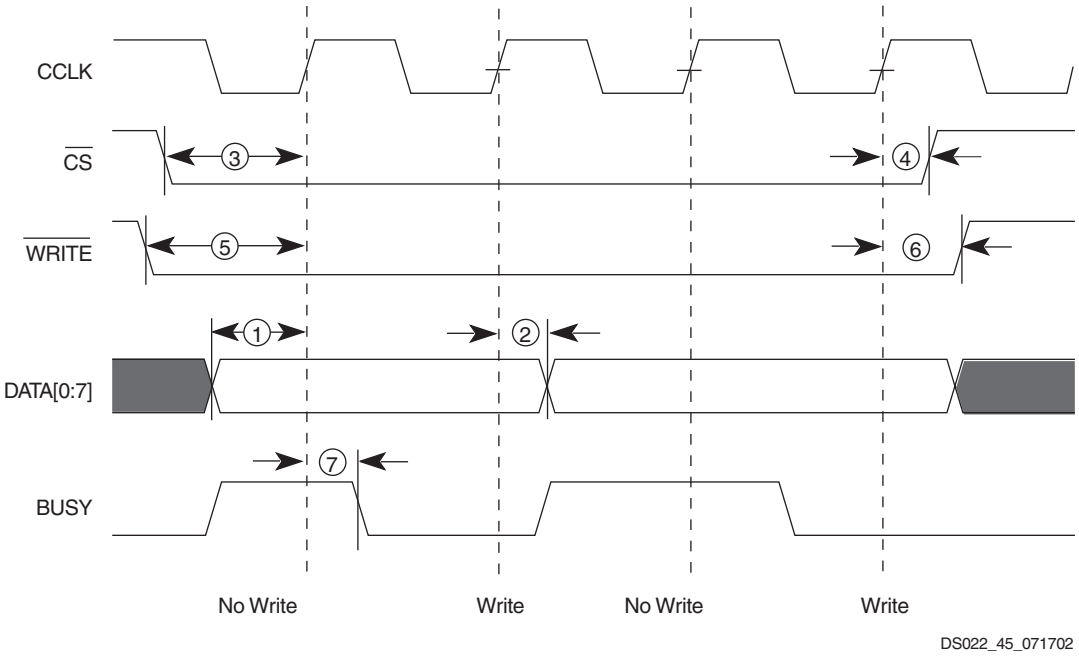


*Figure 17:* **Write Operations**

A flowchart for the write operation appears in Figure 18. Note that if CCLK is slower than $f_{CCNH}$, the FPGA never asserts BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

### Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device remains BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{WRITE}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 19.

## Initialization

The block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 17. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

## Initialization in VHDL and Synopsys

The block SelectRAM+ structures can be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

*Table 17:* **RAM Initialization Properties**

| Property | Memory Cells |
|---|---|
| INIT_00 | 255 to 0 |
| INIT_01 | 511 to 256 |
| INIT_02 | 767 to 512 |
| INIT_03 | 1023 to 768 |
| INIT_04 | 1279 to 1024 |
| INIT_05 | 1535 to 1280 |
| INIT_06 | 1791 to 2047 |
| INIT_07 | 2047 to 1792 |
| INIT_08 | 2303 to 2048 |
| INIT_09 | 2559 to 2304 |
| INIT_0a | 2815 to 2560 |
| INIT_0b | 3071 to 2816 |
| INIT_0c | 3327 to 3072 |
| INIT_0d | 3583 to 3328 |
| INIT_0e | 3839 to 3584 |
| INIT_0f | 4095 to 3840 |

## Initialization in Verilog and Synopsys

The block SelectRAM+ structures can be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

## Design Examples

### *Creating a 32-bit Single-Port RAM*

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single block SelectRAM+ cell as shown inTable 35.

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 ($V_{CC}$), and the LSB of the address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

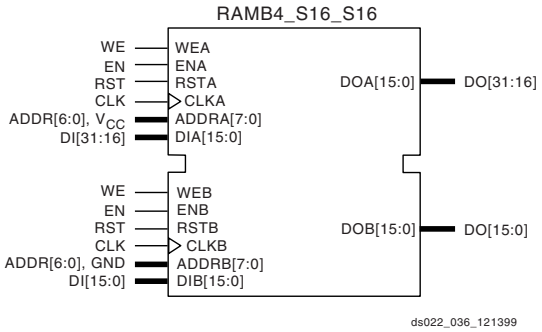


*Figure 35:* **Single Port 128 x 32 RAM**

### *Creating Two Single-Port RAMs*

The true dual-read/write port functionality of the block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in Figure 36.

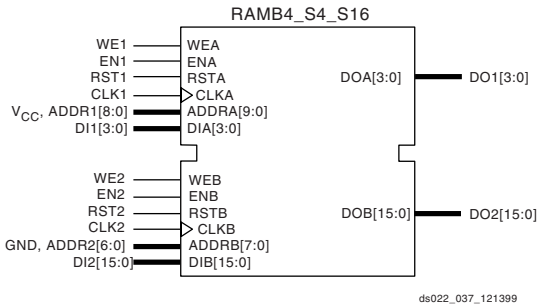


*Figure 36:* **512 x 4 RAM and 128 x 16 RAM**

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single block SelectRAM+. The address space for the RAM is split by fixing the MSB of Port A to 1 ($V_{CC}$) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

## Block Memory Generation

The CoreGen program generates memory structures using the block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

## VHDL Initialization Example

```
library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (

INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);

end BEHAVE;
```

## Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 18, each buffer type can support a variety of voltage requirements.

*Table 18:* **Virtex-E Supported I/O Standards**

| I/O Standard | Output $V_{CCO}$ | Input $V_{CCO}$ | Input $V_{REF}$ | Board Termination Voltage ($V_{TT}$) |
|---|---|---|---|---|
| LVTTL | 3.3 | 3.3 | N/A | N/A |
| LVCMOS2 | 2.5 | 2.5 | N/A | N/A |
| LVCMOS18 | 1.8 | 1.8 | N/A | N/A |
| SSTL3 I & II | 3.3 | N/A | 1.50 | 1.50 |
| SSTL2 I & II | 2.5 | N/A | 1.25 | 1.25 |
| GTL | N/A | N/A | 0.80 | 1.20 |
| GTL+ | N/A | N/A | 1.0 | 1.50 |
| HSTL I | 1.5 | N/A | 0.75 | 0.75 |
| HSTL III & IV | 1.5 | N/A | 0.90 | 1.50 |
| CTT | 3.3 | N/A | 1.50 | 1.50 |
| AGP-2X | 3.3 | N/A | 1.32 | N/A |
| PCI33_3 | 3.3 | 3.3 | N/A | N/A |
| PCI66_3 | 3.3 | 3.3 | N/A | N/A |
| BLVDS & LVDS | 2.5 | N/A | N/A | N/A |
| LVPECL | 3.3 | N/A | N/A | N/A |

## Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification can be found on the Electronic Industry Alliance Jedec website at:

http://www.jedec.org

### *LVTTL — Low-Voltage TTL*

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3 V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3 V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a termination voltage ($V_{TT}$).

### *LVCMOS2 — Low-Voltage CMOS for 2.5 Volts*

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5 V applications. This standard requires a 2.5 V output source voltage ($V_{CCO}$), but does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$).

### *LVCMOS18 — 1.8 V Low Voltage CMOS*

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$) is not required.

### *PCI — Peripheral Component Interface*

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage ($V_{REF}$) or a board termination voltage ($V_{TT}$), however, it does require a 3.3 V output source voltage ($V_{CCO}$).

### *GTL — Gunning Transceiver Logic Terminated*

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

### *GTL+ — Gunning Transceiver Logic Plus*

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

### *HSTL — High-Speed Transceiver Logic*

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5 V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows.

```
OBUFT_<slew_rate>_<drive_strength>
```

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

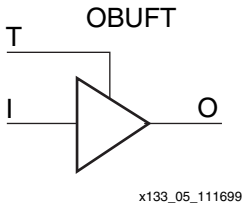


*Figure 41:* **3-State Output Buffer Symbol (OBUFT)**

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP
- OBUFT_LVCMOS18
- OBUFT_LVDS
- OBUFT_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four $V_{CCO}$ banks.

The SelectI/O OBUFT placement restrictions require that within a given $V_{CCO}$ bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require $V_{CCO}$ can be placed within the same $V_{CCO}$ bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak “keeper” circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a $V_{REF}$ have automatic placement of a $V_{REF}$ in the bank with an OBUFT configured with a weak “keeper” circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak “keeper” typically implement a bidirectional I/O. In this case the IBUF (and the corresponding $V_{REF}$) are explicitly placed.

The LOC property can specify a location for the OBUFT.

### *IOBUF*

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 42.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows.

```
IOBUF_<slew_rate>_<drive_strength>
```

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

Input termination techniques include the following:

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

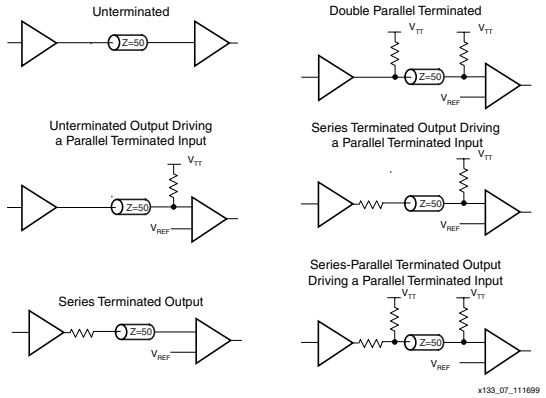


*Figure 43:* **Overview of Standard Input and Output Termination Methods**

### *Simultaneous Switching Guidelines*

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

*Table 21:* **Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

| Standard | Package |
|---|---|
| | BGA, FGA |
| LVTTL Slow Slew Rate, 2 mA drive | 68 |
| LVTTL Slow Slew Rate, 4 mA drive | 41 |
| LVTTL Slow Slew Rate, 6 mA drive | 29 |
| LVTTL Slow Slew Rate, 8 mA drive | 22 |
| LVTTL Slow Slew Rate, 12 mA drive | 17 |
| LVTTL Slow Slew Rate, 16 mA drive | 14 |
| LVTTL Slow Slew Rate, 24 mA drive | 9 |
| LVTTL Fast Slew Rate, 2 mA drive | 40 |
| LVTTL Fast Slew Rate, 4 mA drive | 24 |
| LVTTL Fast Slew Rate, 6 mA drive | 17 |
| LVTTL Fast Slew Rate, 8 mA drive | 13 |
| LVTTL Fast Slew Rate, 12 mA drive | 10 |
| LVTTL Fast Slew Rate, 16 mA drive | 8 |
| LVTTL Fast Slew Rate, 24 mA drive | 5 |
| LVCMOS | 10 |
| PCI | 8 |
| GTL | 4 |
| GTL+ | 4 |
| HSTL Class I | 18 |
| HSTL Class III | 9 |
| HSTL Class IV | 5 |
| SSTL2 Class I | 15 |
| SSTL2 Class II | 10 |
| SSTL3 Class I | 11 |
| SSTL3 Class II | 7 |
| CTT | 14 |
| AGP | 9 |

Note: This analysis assumes a 35 pF load for each output.

*Table 22:* **Virtex-E Extended Memory Family Equivalent Power/Ground Pairs**

| Pkg/Part | XCV405E | XCV812E |
|---|---|---|
| BG560 | | 56 |
| FG676 | 56 | |
| FG900 | | |

## Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

### *Termination Examples*

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

#### GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 44. Table 23 lists DC voltage specifications.

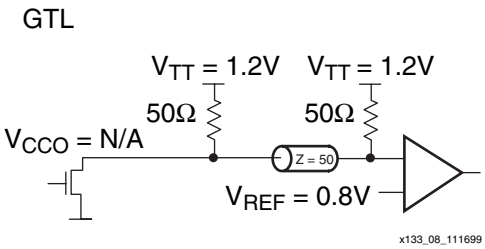


*Figure 44:* **Terminated GTL**

*Table 23:* **GTL Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | N/A | - |
| $V_{REF} = N \times V_{TT}$[1] | 0.74 | 0.8 | 0.86 |
| $V_{TT}$ | 1.14 | 1.2 | 1.26 |
| $V_{IH} = V_{REF} + 0.05$ | 0.79 | 0.85 | - |
| $V_{IL} = V_{REF} - 0.05$ | - | 0.75 | 0.81 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | - | 0.2 | 0.4 |
| $I_{OH}$ at $V_{OH}$(mA) | - | - | - |
| $I_{OL}$at $V_{OL}$(mA) at 0.4V | 32 | - | - |
| $I_{OL}$at $V_{OL}$(mA) at 0.2V | - | - | 40 |

Note: N must be greater than or equal to 0.653 and less than or equal to 0.68.

#### GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 45. DC voltage specifications appear in Table 24.

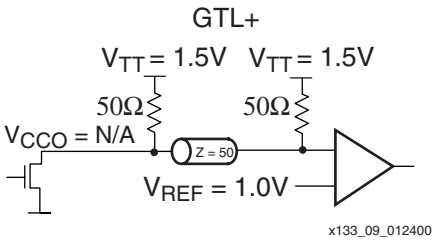


*Figure 45:* **Terminated GTL+**

*Table 24:* **GTL+ Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | - | - | - |
| $V_{REF} = N \times V_{TT}$[1] | 0.88 | 1.0 | 1.12 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} = V_{REF} + 0.1$ | 0.98 | 1.1 | - |
| $V_{IL} = V_{REF} - 0.1$ | - | 0.9 | 1.02 |
| $V_{OH}$ | - | - | - |
| $V_{OL}$ | 0.3 | 0.45 | 0.6 |
| $I_{OH}$ at $V_{OH}$ (mA) | - | - | - |
| $I_{OL}$at $V_{OL}$ (mA) at 0.6V | 36 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) at 0.3V | - | - | 48 |

Note: N must be greater than or equal to 0.653 and less than or equal to 0.68.

### SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 52. DC voltage specifications appear in Table 31.

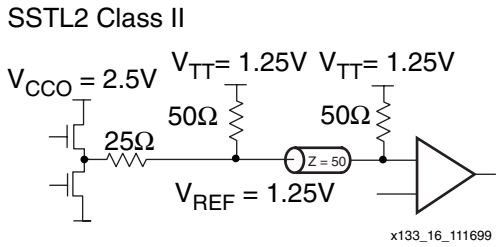


*Figure 52:* **Terminated SSTL2 Class II**

*Table 31:* **SSTL2_II Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.3 | 2.5 | 2.7 |
| $V_{REF} = 0.5 \times V_{CCO}$ | 1.15 | 1.25 | 1.35 |
| $V_{TT} = V_{REF} + N^{(1)}$ | 1.11 | 1.25 | 1.39 |
| $V_{IH} = V_{REF} + 0.18$ | 1.33 | 1.43 | 3.0(2) |
| $V_{IL} = V_{REF} - 0.18$ | –0.3(3) | 1.07 | 1.17 |
| $V_{OH} = V_{REF} + 0.8$ | 1.95 | - | - |
| $V_{OL} = V_{REF} - 0.8$ | - | - | 0.55 |
| $I_{OH}$ at $V_{OH}$ (mA) | –15.2 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 15.2 | - | - |

**Notes:**
1. N must be greater than or equal to –0.04 and less than or equal to 0.04.
2. $V_{IH}$ maximum is $V_{CCO}$ + 0.3.
3. $V_{IL}$ minimum does not conform to the formula.

### CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 53. DC voltage specifications appear in Table 32.

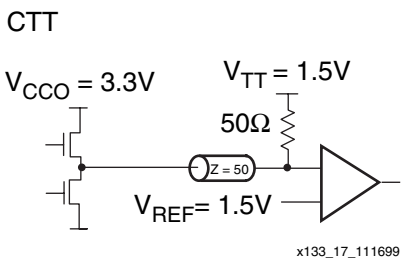


*Figure 53:* **Terminated CTT**

*Table 32:* **CTT Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 2.05(1) | 3.3 | 3.6 |
| $V_{REF}$ | 1.35 | 1.5 | 1.65 |
| $V_{TT}$ | 1.35 | 1.5 | 1.65 |
| $V_{IH} = V_{REF} + 0.2$ | 1.55 | 1.7 | - |
| $V_{IL} = V_{REF} - 0.2$ | - | 1.3 | 1.45 |
| $V_{OH} = V_{REF} + 0.4$ | 1.75 | 1.9 | - |
| $V_{OL}= V_{REF} - 0.4$ | - | 1.1 | 1.25 |
| $I_{OH}$ at $V_{OH}$ (mA) | –8 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | 8 | - | - |

**Notes:**
1. Timing delays are calculated based on $V_{CCO}$ min of 3.0V.

### PCI33_3 & PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 33.

*Table 33:* **PCI33_3 and PCI66_3 Voltage Specifications**

| Parameter | Min | Typ | Max |
|---|---|---|---|
| $V_{CCO}$ | 3.0 | 3.3 | 3.6 |
| $V_{REF}$ | - | - | - |
| $V_{TT}$ | - | - | - |
| $V_{IH} = 0.5 \times V_{CCO}$ | 1.5 | 1.65 | $V_{CCO}$+ 0.5 |
| $V_{IL} = 0.3 \times V_{CCO}$ | –0.5 | 0.99 | 1.08 |
| $V_{OH} = 0.9 \times V_{CCO}$ | 2.7 | - | - |
| $V_{OL}= 0.1 \times V_{CCO}$ | - | - | 0.36 |
| $I_{OH}$ at $V_{OH}$ (mA) | Note 1 | - | - |
| $I_{OL}$at $V_{OL}$ (mA) | Note 1 | - | - |

Note 1: Tested according to the relevant specification.

*Table 44:* **Bidirectional I/O Library Macros *(Continued)***

| Name | Inputs | Bidirectional | Outputs |
|---|---|---|---|
| IOBUFDS_LD_LVDS | D, T, G | IO, IOB | Q |
| IOBUFDS_LDE_LVDS | D, T, GE, G | IO, IOB | Q |
| IOBUFDS_LDC_LVDS | D, T, G, CLR | IO, IOB | Q |
| IOBUFDS_LDCE_LVDS | D, T, GE, G, CLR | IO, IOB | Q |
| IOBUFDS_LDP_LVDS | D, T, G, PRE | IO, IOB | Q |
| IOBUFDS_LDPE_LVDS | D, T, GE, G, PRE | IO, IOB | Q |

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 03/23/00 | 1.0 | Initial Xilinx release. |
| 08/01/00 | 1.1 | Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table. |
| 09/19/00 | 1.2 | • In Table 3 (Module 4), **FG676 Fine-Pitch BGA — XCV405E**, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1.<br>• Min values added to **Virtex-E Electrical Characteristics** tables. |
| 11/20/00 | 1.3 | • Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3).<br>• Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2).<br>• Added to note 2 of **Absolute Maximum Ratings** (Module 3).<br>• Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3).<br>• Revised maximum $T_{DLLPW}$ in -6 speed grade for **DLL Timing Parameters** (Module 3). |
| 04/02/01 | 1.4 | • In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF.<br>• Updated values in Virtex-E Switching Characteristics tables.<br>• Converted data sheet to modularized format. |
| 04/19/01 | 1.5 | • Modified Figure 30, which shows “DLL Generation of 4x Clock in Virtex-E Devices.” |
| 07/23/01 | 1.6 | • Made minor edits to text under Configuration. |
| 11/16/01 | 2.0 | • Added warning under Configuration section that attempting to load an incorrect bitstream causes configuration to fail and can damage the device. |
| 07/17/02 | 2.1 | • Data sheet designation upgraded from Preliminary to Production. |
| 09/10/02 | 2.2 | • Added clarifications in the Input/Output Block, Configuration, Boundary-Scan Mode, and Block SelectRAM+ Memory sections. Revised Figure 18, Table 11, and Table 36. |
| 11/19/02 | 2.3 | • Added clarification in the Boundary Scan section.<br>• Removed last sentence regarding deactivation of duty-cycle correction in Duty Cycle Correction Property section. |

# Virtex-E Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

## IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.

| | | | Speed Grade(2) | | | | |
|---|---|---|---|---|---|---|---|
| **Description(1)** | **Symbol** | **Device** | **Min** | **-8** | **-7** | **-6** | **Units** |
| **Propagation Delays** | | | | | | | |
| Pad to I output, no delay | $T_{IOPI}$ | All | 0.43 | 0.8 | 0.8 | 0.8 | ns, max |
| Pad to I output, with delay | $T_{IOPID}$ | XCV405E | 0.51 | 1.0 | 1.0 | 1.0 | ns, max |
| | | XCV812E | 0.55 | 1.1 | 1.1 | 1.1 | ns, max |
| Pad to output IQ via transparent latch, no delay | $T_{IOPLI}$ | All | 0.75 | 1.4 | 1.5 | 1.6 | ns, max |
| Pad to output IQ via transparent latch, with delay | $T_{IOPLID}$ | XCV405E | 1.55 | 3.5 | 3.6 | 3.7 | ns, max |
| | | XCV812E | 1.55 | 3.5 | 3.6 | 3.7 | ns, max |
| **Propagation Delays** | | | | | | | |
| **Clock** | | | | | | | |
| Minimum Pulse Width, High | $T_{CH}$ | All | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| Minimum Pulse Width, Low | $T_{CL}$ | | 0.56 | 1.2 | 1.3 | 1.4 | ns, min |
| Clock CLK to output IQ | $T_{IOCKIQ}$ | | 0.18 | 0.4 | 0.7 | 0.7 | ns, max |
| **Setup and Hold Times with respect to Clock at IOB Input Register** | | | | | | | |
| Pad, no delay | $T_{IOPICK}$ / $T_{IOICKP}$ | All | 0.69 / 0 | 1.3 / 0 | 1.4 / 0 | 1.5 / 0 | ns, min |
| Pad, with delay | $T_{IOPICKD}$ / $T_{IOICKPD}$ | XCV405E | 1.49 / 0 | 3.4 / 0 | 3.5 / 0 | 3.5 / 0 | ns, min |
| | | XCV812E | 1.49 / 0 | 3.4 / 0 | 3.5 / 0 | 3.5 / 0 | ns, min |
| ICE input | $T_{IOICECK}$ / $T_{IOCKICE}$ | All | 0.28 / 0.0 | 0.55 / 0.01 | 0.7 / 0.01 | 0.7 / 0.01 | ns, min |
| SR input (IFF, synchronous) | $T_{IOSRCKI}$ | All | 0.38 | 0.8 | 0.9 | 1.0 | ns, min |
| **Set/Reset Delays** | | | | | | | |
| SR input to IQ (asynchronous) | $T_{IOSRIQ}$ | All | 0.54 | 1.1 | 1.2 | 1.4 | ns, max |
| GSR to output IQ | $T_{GSRQ}$ | All | 3.88 | 7.6 | 8.5 | 9.7 | ns, max |

**Notes:**
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

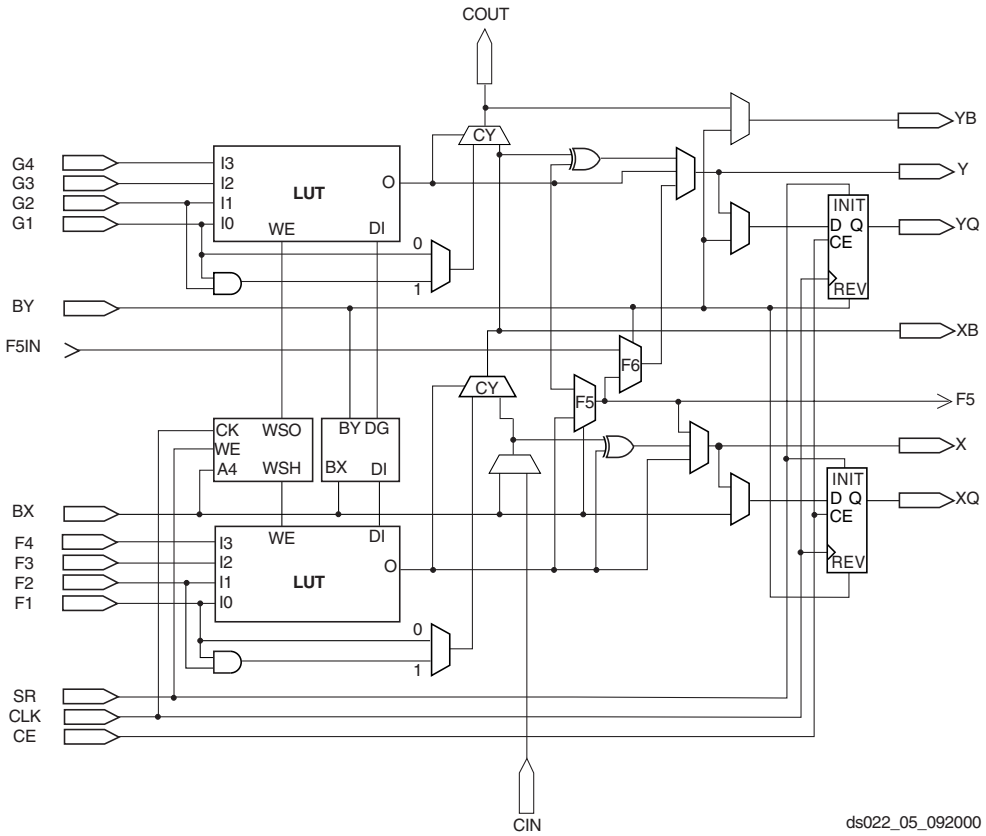


*Figure 2:* **Detailed View of Virtex-E Slice**

## CLB Distributed RAM Switching Characteristics

| Description[1] | Symbol | Speed Grade | | | | Units |
|---|---|---|---|---|---|---|
| | | Min | -8 | -7 | -6 | |
| **Sequential Delays** | | | | | | |
| Clock CLK to X/Y outputs (WE active) 16 x 1 mode | $T_{SHCKO16}$ | 0.67 | 1.38 | 1.5 | 1.7 | ns, max |
| Clock CLK to X/Y outputs (WE active) 32 x 1 mode | $T_{SHCKO32}$ | 0.84 | 1.66 | 1.9 | 2.1 | ns, max |
| **Shift-Register Mode**<br>Clock CLK to X/Y outputs | $T_{REG}$ | 1.25 | 2.39 | 2.9 | 3.2 | ns, max |
| **Setup and Hold Times before/after Clock CLK** | | | | | | |
| F/G address inputs | $T_{AS}/T_{AH}$ | 0.19 / 0 | 0.38 / 0 | 0.42 / 0 | 0.47 / 0 | ns, min |
| BX/BY data inputs (DIN) | $T_{DS}/T_{DH}$ | 0.44 / 0 | 0.87 / 0 | 0.97 / 0 | 1.09 / 0 | ns, min |
| SR input (WE) | $T_{WS}/T_{WH}$ | 0.29 / 0 | 0.57 / 0 | 0.7 / 0 | 0.8 / 0 | ns, min |
| **Clock CLK** | | | | | | |
| Minimum Pulse Width, High | $T_{WPH}$ | 0.96 | 1.9 | 2.1 | 2.4 | ns, min |
| Minimum Pulse Width, Low | $T_{WPL}$ | 0.96 | 1.9 | 2.1 | 2.4 | ns, min |
| Minimum clock period to meet address write cycle time | $T_{WC}$ | 1.92 | 3.8 | 4.2 | 4.8 | ns, min |
| **Shift-Register Mode** | | | | | | |
| Minimum Pulse Width, High | $T_{SRPH}$ | 1.0 | 1.9 | 2.1 | 2.4 | ns, min |
| Minimum Pulse Width, Low | $T_{SRPL}$ | 1.0 | 1.9 | 2.1 | 2.4 | ns, min |

**Notes:**
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

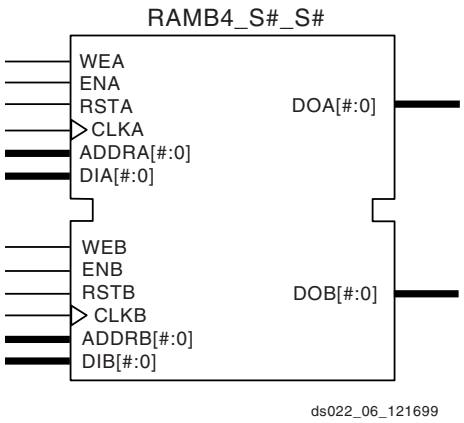


*Figure 3:* **Dual-Port Block SelectRAM**

# Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

## Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

| Description[1] | Symbol | Device[3] | Speed Grade[2] | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -8 | -7 | -6 | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.<br>For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6. | | | | | | | |
| No Delay | $T_{PSDLL}/T_{PHDLL}$ | XCV405E | 1.5 / –0.4 | 1.5 / –0.4 | 1.6 / –0.4 | 1.7 / –0.4 | ns |
| Global Clock and IFF, with DLL | | XCV812E | 1.5 / –0.4 | 1.5 / –0.4 | 1.6 / –0.4 | 1.7 / –0.4 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

## Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

| Description[1] | Symbol | Device[3] | Speed Grade[2] | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | -8 | -7 | -6 | |
| Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard.<br>For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6. | | | | | | | |
| Full Delay | $T_{PSFD}/T_{PHFD}$ | XCV405E | 2.3 / 0 | 2.3 / 0 | 2.3 / 0 | 2.3 / 0 | ns |
| Global Clock and IFF, without DLL | | XCV812E | 2.5 / 0 | 2.5 / 0 | 2.5 / 0 | 2.5 / 0 | ns |

**Notes:**
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

## DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

| | | | CLKDLLHF | | CLKDLL | | |
|---|---|---|---|---|---|---|---|
| **Description** | **Symbol** | **$F_{CLKIN}$** | **Min** | **Max** | **Min** | **Max** | **Units** |
| Input Clock Period Tolerance | $T_{IPTOL}$ | | - | 1.0 | - | 1.0 | ns |
| Input Clock Jitter Tolerance (Cycle to Cycle) | $T_{IJITCC}$ | | - | ± 150 | - | ± 300 | ps |
| Time Required for DLL to Acquire Lock(6) | $T_{LOCK}$ | > 60 MHz | - | 20 | - | 20 | µs |
| | | 50 - 60 MHz | - | - | - | 25 | µs |
| | | 40 - 50 MHz | - | - | - | 50 | µs |
| | | 30 - 40 MHz | - | - | - | 90 | µs |
| | | 25 - 30 MHz | - | - | - | 120 | µs |
| Output Jitter (cycle-to-cycle) for any DLL Clock Output(1) | $T_{OJITCC}$ | | | ± 60 | | ± 60 | ps |
| Phase Offset between CLKIN and CLKO(2) | $T_{PHIO}$ | | | ± 100 | | ± 100 | ps |
| Phase Offset between Clock Outputs on the DLL(3) | $T_{PHOO}$ | | | ± 140 | | ± 140 | ps |
| Maximum Phase Difference between CLKIN and CLKO(4) | $T_{PHIOM}$ | | | ± 160 | | ± 160 | ps |
| Maximum Phase Difference between Clock Outputs on the DLL(5) | $T_{PHOOM}$ | | | ± 200 | | ± 200 | ps |

**Notes:**

1. **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock and is based on a maximum tap delay resolution, *excluding* input clock jitter.
2. **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
3. **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
4. **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
5. **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
6. Add 30% to the value for Industrial grade parts.

## Revision History

The following table shows the revision history for this document.

| Date | Version | Revision |
|---|---|---|
| 03/23/00 | 1.0 | Initial Xilinx release. |
| 08/01/00 | 1.1 | Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table. |
| 09/19/00 | 1.2 | • In Table 3 (Module 4), **FG676 Fine-Pitch BGA — XCV405E**, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1.<br>• Min values added to **Virtex-E Electrical Characteristics** tables. |

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 7 | IO_L182P_YY | E4 |
| | | |
| 2 | CCLK | D24 |
| 3 | DONE | AB21 |
| NA | DXN | AB7 |
| NA | DXP | Y8 |
| NA | M0 | AD4 |
| NA | M1 | W7 |
| NA | M2 | AB6 |
| NA | PROGRAM | AA22 |
| NA | TCK | E6 |
| NA | TDI | D22 |
| 2 | TDO | C23 |
| NA | TMS | F5 |
| | | |
| 0 | NC | A9 |
| 0 | NC | A10 |
| 0 | NC | B4 |
| 0 | NC | B12 |
| 0 | NC | D13 |
| 1 | NC | A13 |
| 1 | NC | A16 |
| 1 | NC | A24 |
| 1 | NC | B15 |
| 1 | NC | B17 |
| 2 | NC | D25 |
| 2 | NC | H26 |
| 2 | NC | K26 |
| 2 | NC | M25 |
| 2 | NC | N26 |
| 3 | NC | AC25 |
| 3 | NC | P26 |
| 3 | NC | R26 |
| 3 | NC | T26 |
| 3 | NC | U26 |

*Table 3:* **FG676 Fine-Pitch BGA — XCV405E**

| Bank | Pin Description | Pin # |
|---|---|---|
| 4 | NC | AE15 |
| 4 | NC | AF14 |
| 4 | NC | AF16 |
| 4 | NC | AF18 |
| 4 | NC | AF23 |
| 5 | NC | AE12 |
| 5 | NC | AF3 |
| 5 | NC | AF10 |
| 5 | NC | AF11 |
| 5 | NC | Y13 |
| 6 | NC | AC1 |
| 6 | NC | P1 |
| 6 | NC | R2 |
| 6 | NC | T1 |
| 6 | NC | V1 |
| 7 | NC | D1 |
| 7 | NC | J1 |
| 7 | NC | L1 |
| 7 | NC | M1 |
| 7 | NC | N1 |
| NA | NC | T25 |
| NA | NC | T2 |
| NA | NC | P2 |
| NA | NC | N25 |
| NA | NC | L25 |
| NA | NC | L2 |
| NA | NC | F6 |
| NA | NC | F25 |
| NA | NC | F21 |
| NA | NC | F2 |
| NA | NC | C26 |
| NA | NC | C25 |
| NA | NC | C2 |
| NA | NC | C1 |
| NA | NC | B6 |

## FG676 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

*Table 4:* **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| Global Differential Clock | | | | | |
| 3 | 0 | E13 | B13 | NA | IO_DLL_L21N |
| 2 | 1 | C13 | F14 | NA | IO_DLL_L21P |
| 1 | 5 | AB13 | AF13 | NA | IO_DLL_L115N |
| 0 | 4 | AA14 | AC14 | NA | IO_DLL_L115P |
| IOLVDS<br>Total Pairs: 183, Asynchronous Output Pairs: 97 | | | | | |
| 0 | 0 | F7 | C4 | NA | - |
| 1 | 0 | C5 | G8 | √ | - |
| 2 | 0 | E7 | D6 | √ | VREF |
| 3 | 0 | F8 | A4 | NA | - |
| 4 | 0 | D7 | B5 | NA | - |
| 5 | 0 | G9 | E8 | √ | VREF |
| 6 | 0 | F9 | A5 | √ | - |
| 7 | 0 | C7 | D8 | NA | - |
| 8 | 0 | E9 | B7 | NA | - |
| 9 | 0 | D9 | A7 | NA | - |
| 10 | 0 | G10 | B8 | NA | VREF |
| 11 | 0 | F10 | C9 | √ | - |
| 12 | 0 | E10 | A8 | NA | - |
| 13 | 0 | D10 | G11 | √ | - |
| 14 | 0 | F11 | B10 | √ | - |
| 15 | 0 | E11 | C10 | NA | - |

*Table 4:* **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 16 | 0 | D11 | G12 | √ | - |
| 17 | 0 | F12 | C11 | √ | VREF |
| 18 | 0 | E12 | A11 | √ | - |
| 19 | 0 | C12 | D12 | NA | - |
| 20 | 0 | H13 | A12 | NA | VREF |
| 21 | 1 | F14 | B13 | NA | IO_LVDS_DLL |
| 22 | 1 | F13 | E14 | NA | - |
| 23 | 1 | A14 | D14 | NA | VREF |
| 24 | 1 | H14 | C14 | NA | - |
| 25 | 1 | C15 | G14 | √ | - |
| 26 | 1 | D15 | E15 | √ | VREF |
| 27 | 1 | F15 | C16 | √ | - |
| 28 | 1 | D16 | G15 | - | - |
| 29 | 1 | A17 | E16 | √ | - |
| 30 | 1 | E17 | C17 | √ | - |
| 31 | 1 | D17 | F16 | NA | - |
| 32 | 1 | C18 | F17 | √ | - |
| 33 | 1 | G16 | A18 | √ | VREF |
| 34 | 1 | G17 | C19 | √ | - |
| 35 | 1 | B19 | D18 | NA | - |
| 36 | 1 | E18 | D19 | NA | - |
| 37 | 1 | B20 | F18 | √ | - |
| 38 | 1 | C20 | G19 | √ | VREF |
| 39 | 1 | E19 | G18 | √ | - |
| 40 | 1 | D20 | A21 | √ | - |
| 41 | 1 | C21 | F19 | √ | VREF |
| 42 | 1 | E20 | B22 | √ | - |
| 43 | 1 | D21 | A23 | 2 | - |
| 44 | 1 | E21 | C22 | √ | CS |
| 45 | 2 | E23 | F22 | √ | DIN, D0 |
| 46 | 2 | E24 | F20 | √ | - |
| 47 | 2 | G21 | G22 | 2 | - |
| 48 | 2 | F24 | H20 | 1 | VREF |
| 49 | 2 | E25 | H21 | 1 | - |

*Table 4:* **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 118 | 5 | AA12 | AD12 | √ | - |
| 119 | 5 | AC12 | AB12 | √ | VREF |
| 120 | 5 | AD11 | Y12 | √ | - |
| 121 | 5 | AB11 | AD10 | NA | - |
| 122 | 5 | AC11 | AE10 | √ | - |
| 123 | 5 | AC10 | AA11 | √ | - |
| 124 | 5 | Y11 | AD9 | NA | - |
| 125 | 5 | AB10 | AF9 | √ | - |
| 126 | 5 | AD8 | AA10 | √ | VREF |
| 127 | 5 | AE8 | Y10 | √ | - |
| 128 | 5 | AC9 | AF8 | NA | - |
| 129 | 5 | AF7 | AB9 | NA | - |
| 130 | 5 | AA9 | AF6 | √ | - |
| 131 | 5 | AC8 | AC7 | √ | VREF |
| 132 | 5 | AD6 | Y9 | √ | - |
| 133 | 5 | AE5 | AA8 | √ | - |
| 134 | 5 | AC6 | AB8 | √ | VREF |
| 135 | 5 | AD5 | AA7 | √ | - |
| 136 | 5 | AF4 | AC5 | NA | - |
| 137 | 6 | AC3 | AA5 | √ | - |
| 138 | 6 | AB4 | AC2 | √ | - |
| 139 | 6 | AA4 | W6 | NA | - |
| 140 | 6 | Y5 | AB3 | NA | VREF |
| 141 | 6 | V7 | AB2 | NA | - |
| 142 | 6 | Y4 | AB1 | √ | - |
| 143 | 6 | W5 | V5 | √ | VREF |
| 144 | 6 | V6 | AA1 | √ | - |
| 145 | 6 | Y3 | W4 | NA | - |
| 146 | 6 | U7 | Y1 | NA | - |
| 147 | 6 | V4 | W1 | √ | - |
| 148 | 6 | U6 | W2 | √ | VREF |
| 149 | 6 | T5 | V3 | √ | - |
| 150 | 6 | U4 | U5 | √ | - |
| 151 | 6 | U3 | T7 | NA | - |

*Table 4:* **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

| Pair | Bank | P Pin | N Pin | AO | Other Functions |
|---|---|---|---|---|---|
| 152 | 6 | T6 | U2 | NA | - |
| 153 | 6 | T4 | U1 | NA | - |
| 154 | 6 | T3 | R7 | NA | - |
| 155 | 6 | R6 | R4 | √ | VREF |
| 156 | 6 | R5 | R3 | √ | - |
| 157 | 6 | P7 | P8 | NA | - |
| 158 | 6 | P6 | R1 | NA | VREF |
| 159 | 6 | P4 | P5 | √ | - |
| 160 | 7 | N8 | N5 | √ | - |
| 161 | 7 | N3 | N6 | √ | - |
| 162 | 7 | M2 | N4 | NA | VREF |
| 163 | 7 | M7 | N7 | NA | - |
| 164 | 7 | M3 | M6 | √ | - |
| 165 | 7 | M5 | M4 | √ | VREF |
| 166 | 7 | L7 | L3 | NA | - |
| 167 | 7 | K2 | L6 | NA | - |
| 168 | 7 | K1 | L4 | NA | - |
| 169 | 7 | L5 | K3 | NA | - |
| 170 | 7 | J3 | K5 | √ | - |
| 171 | 7 | J4 | K4 | √ | - |
| 172 | 7 | K6 | H3 | √ | VREF |
| 173 | 7 | G3 | K7 | √ | - |
| 174 | 7 | H1 | J5 | NA | - |
| 175 | 7 | J6 | G2 | NA | - |
| 176 | 7 | F1 | J7 | √ | - |
| 177 | 7 | G4 | H4 | √ | VREF |
| 178 | 7 | H5 | F3 | NA | - |
| 179 | 7 | H6 | E2 | NA | - |
| 180 | 7 | F4 | G5 | NA | VREF |
| 181 | 7 | G6 | H7 | NA | - |
| 182 | 7 | E4 | E3 | √ | - |

## Virtex-E Extended Memory Device/Package Combinations and Maximum I/O

| Virtex-E Extended Memory Series Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins) | | |
|---|---|---|
| **Package** | **XCV405E** | **XCV812E** |
| BG560 | 404 | 404 |
| FG676 | 404 | |
| FG900 | | 556 |

## Virtex-E Ordering Information

Virtex-II ordering information is shown in Figure 1

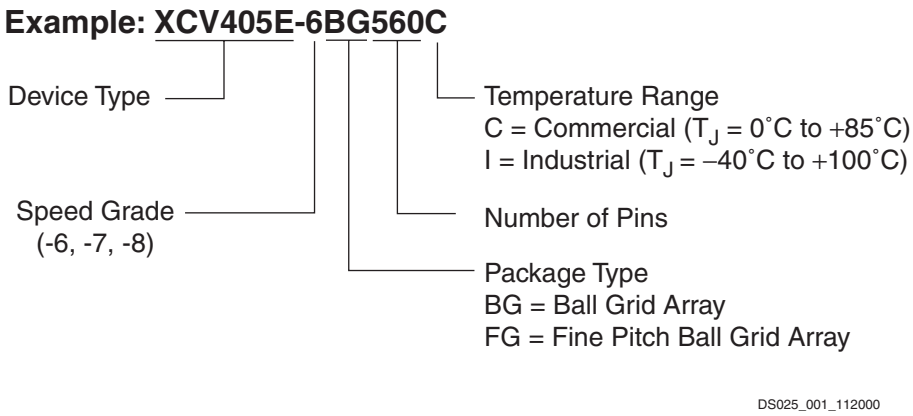


*Figure 1:* **Virtex Ordering Information**