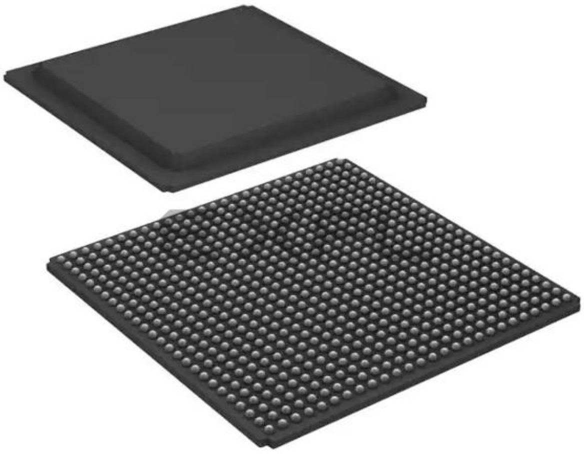
AMD Xilinx - XCV405E-7FG676I Datasheet



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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	573440
Number of I/O	404
Number of Gates	129600
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	676-BGA
Supplier Device Package	676-FBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv405e-7fg676i

Email: info@E-XFL.COM Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Table 1: **Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} with the exception of LVCMOS18, LVCMOS25, GTL, GTL+, LVDS, and LVPECL.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but IOs can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF} The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking" on page 2.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 - 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking" on page 2.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of

DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

For more information about DLL functionality, see the Design Consideration section of the data sheet.

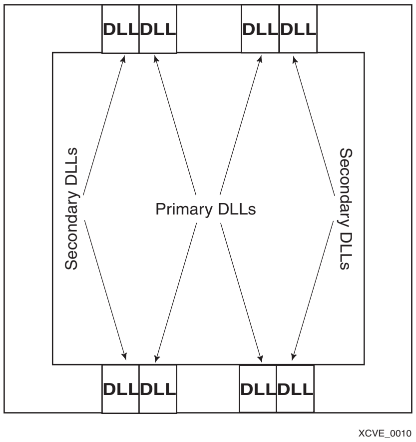

Figure 10: **DLL Locations**

Boundary Scan

Virtex-E devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The JTAG input pins (TDI, TMS, TCK) do not have a V_{CCO} requirement, and operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the V_{CCO} in bank 2, and for proper operation of LVTTL 3.3 V levels, the bank should be supplied with 3.3 V.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections, provided the user design or application is turned off.

Table 6 lists the boundary-scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They can also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 11 is a diagram of the Virtex-E Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

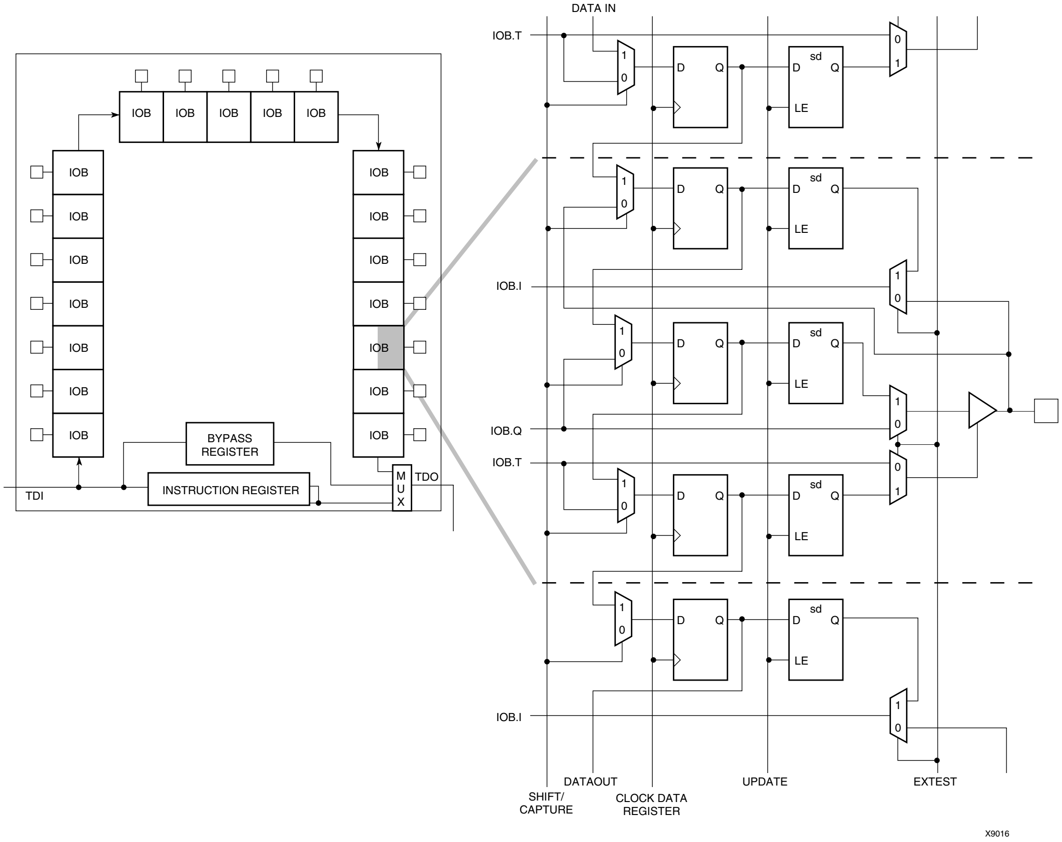

Figure 11: **Virtex-E Family Boundary Scan Logic**

Table 6: **Boundary Scan Instructions**

Boundary-Scan Command	**Binary Code (4:0)**	**Description**
EXTEST	00000	Enable boundary-scan EXTEST operation.
SAMPLE/ PRELOAD	00001	Enable boundary-scan SAMPLE/PRELOAD operation.
USER1	00010	Access user-defined register 1.
USER2	00011	Access user-defined register 2.
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enable boundary-scan INTEST operation.
USERCODE	01000	Enable shifting out USER code.
IDCODE	01001	Enable shifting out of ID Code.
HIGHZ	01010	3-state output pins while enabling the Bypass Register.
JSTART	01100	Clock the start-up sequence when StartupClk is TCK.
BYPASS	11111	Enable BYPASS.
RESERVED	All other codes	Xilinx reserved instructions.

Instruction Set

The Virtex-E Series boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 6.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only.

Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (T DO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 12.

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

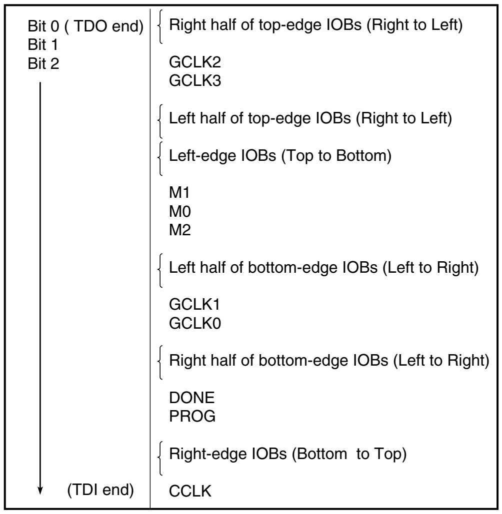

Figure 12: **Boundary Scan Bit Sequence**

Table 8: **Configuration Codes**

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Table 9 lists the total number of bits required to configure each device.

Table 9: **Virtex-E Bitstream Lengths**

Device	# of Configuration Bits
XCV405E	3,430,400
XCV812E	6,519,648

Slave-Serial Mode

In slave-serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be set up at the DIN input pin a short time before each rising edge of an externally generated CCLK.

For more detailed information on serial PROMs see the PROM data sheet at **http://www.xilinx.com/bvdocs/publications/ds026.pdf**.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. Data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families but does not cause a problem for mixed configuration chains. This change was made to improve serial configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave-serial mode should be connected as shown in the right-most device.

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave-serial the default mode if the pins are left unconnected. However, it is recommended to drive the configuration mode pins externally. Figure 14 shows slave-serial mode programming switching characteristics.

Table 10 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the $\overline{\text{INIT}}$ pins of all daisy-chained FPGAs are High.

Table 10: **Master/Slave Serial Mode Programming Switching**

	Description	Figure References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{CKDS}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% –30%	

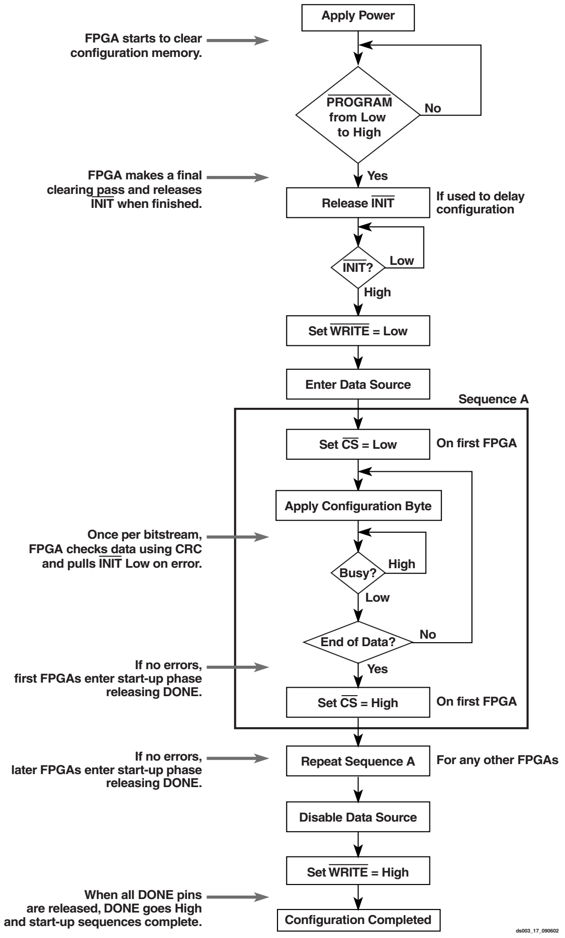

Figure 18: **SelectMAP Flowchart for Write Operations**

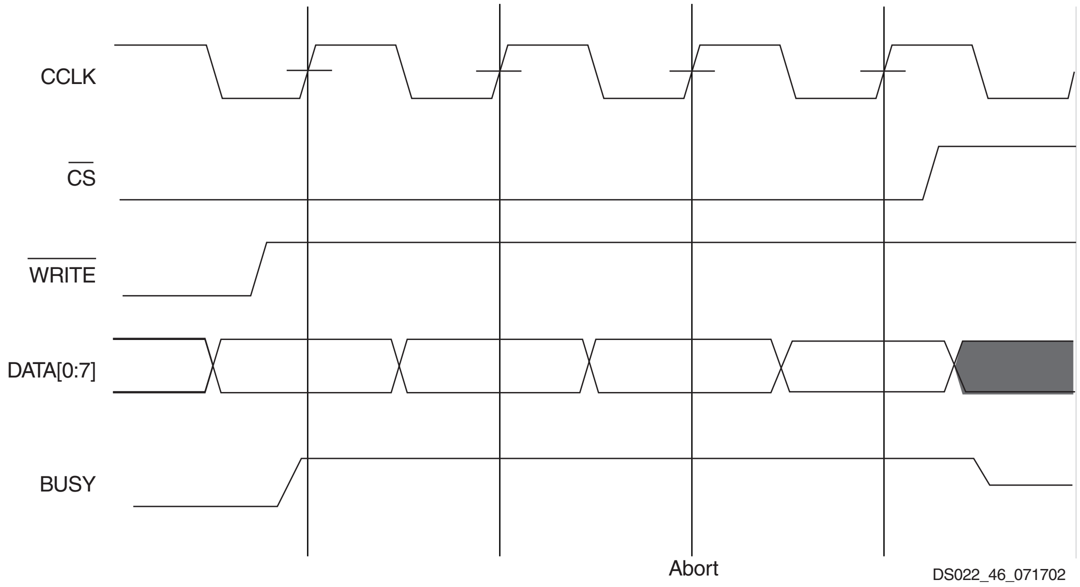

Figure 19: **SelectMAP Write Abort Waveforms**

Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the PROGRAM pin must be pulled High prior to reconfiguration. A Low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

Conflict Resolution

The block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
    - The write succeeds
    - The data out on the writing port accurately reflects the data written.
    - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 33 shows a timing diagram for a single port of a block SelectRAM+ memory. The block SelectRAM+ AC switching characteristics are specified in the data sheet. The block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 34 shows a timing diagram for a true dual-port read/write block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location are invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory are correct, but the read port has invalid data. At the first rising edge of CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.

The voltage reference signal is "banked" within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 19 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

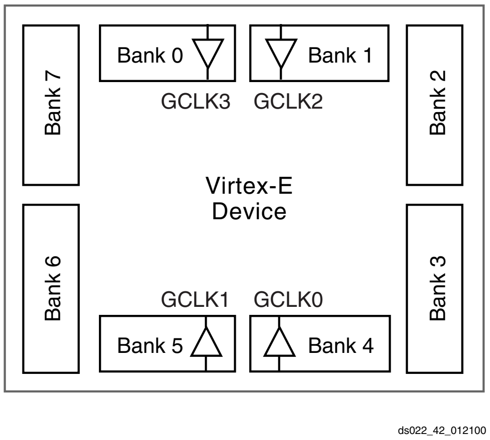

Figure 38: **Virtex-E I/O Banks**

Table 19: **Xilinx Input Standards Compatibility Requirements**

Rule 1	Standards with the same input V_{CCO}, output V_{CCO}, and V_{REF} can be placed within the same bank.

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG should only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 39.

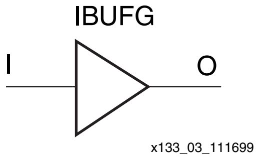

Figure 39: **Virtex-E Global Clock Input Buffer (IBUFG) Symbol**

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is "banked" within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 40.

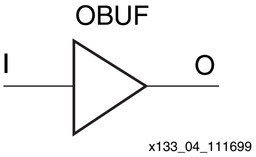

Figure 40: **Virtex-E Output Buffer (OBUF) Symbol**

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows.

`OBUF_<slew_rate>_<drive_strength>`

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank.

Table 20 summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 20: **Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards that share compatible V_{CCO} can be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 41, typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

IOB Flip-Flop/Latch Property

The Virtex-E series I/O block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

```
map -pr b <filename>
```

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form.

```
LOC=A42
LOC=P37
```

Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

```
SLEW=SLOW
SLEW=FAST
```

Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

```
DRIVE=2
DRIVE=4
DRIVE=6
DRIVE=8
DRIVE=12 (Default)
DRIVE=16
DRIVE=24
```

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, LVCMOS18, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following are output termination techniques:

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Input termination techniques include the following:

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

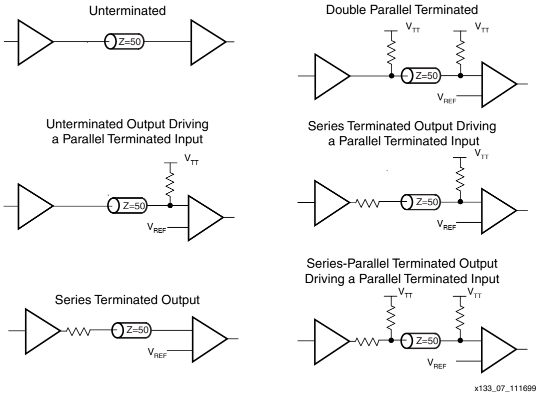

Figure 43: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 21: **Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

	Package
Standard	**BGA, FGA**
LVTTL Slow Slew Rate, 2 mA drive	68
LVTTL Slow Slew Rate, 4 mA drive	41
LVTTL Slow Slew Rate, 6 mA drive	29
LVTTL Slow Slew Rate, 8 mA drive	22
LVTTL Slow Slew Rate, 12 mA drive	17
LVTTL Slow Slew Rate, 16 mA drive	14
LVTTL Slow Slew Rate, 24 mA drive	9
LVTTL Fast Slew Rate, 2 mA drive	40
LVTTL Fast Slew Rate, 4 mA drive	24
LVTTL Fast Slew Rate, 6 mA drive	17
LVTTL Fast Slew Rate, 8 mA drive	13
LVTTL Fast Slew Rate, 12 mA drive	10
LVTTL Fast Slew Rate, 16 mA drive	8
LVTTL Fast Slew Rate, 24 mA drive	5
LVCMOS	10
PCI	8
GTL	4
GTL+	4
HSTL Class I	18
HSTL Class III	9
HSTL Class IV	5
SSTL2 Class I	15
SSTL2 Class II	10
SSTL3 Class I	11
SSTL3 Class II	7
CTT	14
AGP	9

Note: This analysis assumes a 35 pF load for each output.

Table 22: **Virtex-E Extended Memory Family Equivalent Power/Ground Pairs**

Pkg/Part	**XCV405E**	**XCV812E**
BG560		56
FG676	56	
FG900		

Calculation of T_{ioop} as a Function of Capacitance

T_{ioop} is the propagation delay from the O Input of the IOB to the pad. The values for T_{ioop} are based on the standard capacitive load (Csl) for each I/O standard as listed in Table 2.

Table 2: **Constants for Use in Calculation of T_{ioop}**

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.10
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33 MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Notes:

1. I/O parameter measurements are made with the capacitance values shown above. See the Application Examples for appropriate terminations.
2. I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}.

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 3: **Delay Measurement Methodology**

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	0.80
GTL+	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	1.0
HSTL Class I	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.75
HSTL Class III	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} –0.5	V_{REF} +0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} –1.0	V_{REF} +1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} –0.75	V_{REF} +0.75	V_{REF}	1.25
CTT	V_{REF} –0.2	V_{REF} +0.2	V_{REF}	1.5
AGP	V_{REF} – ($0.2xV_{CCO}$)	V_{REF} + ($0.2xV_{CCO}$)	V_{REF}	Per AGP Spec
LVDS	1.2 – 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 – 0.3	1.6 + 0.3	1.6	

Notes:

1. Input waveform switches between V_L and V_H.
2. Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.

   I/O parameter measurements are made with the capacitance values shown in Table 2. See the Application Examples for appropriate terminations.

   I/O standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

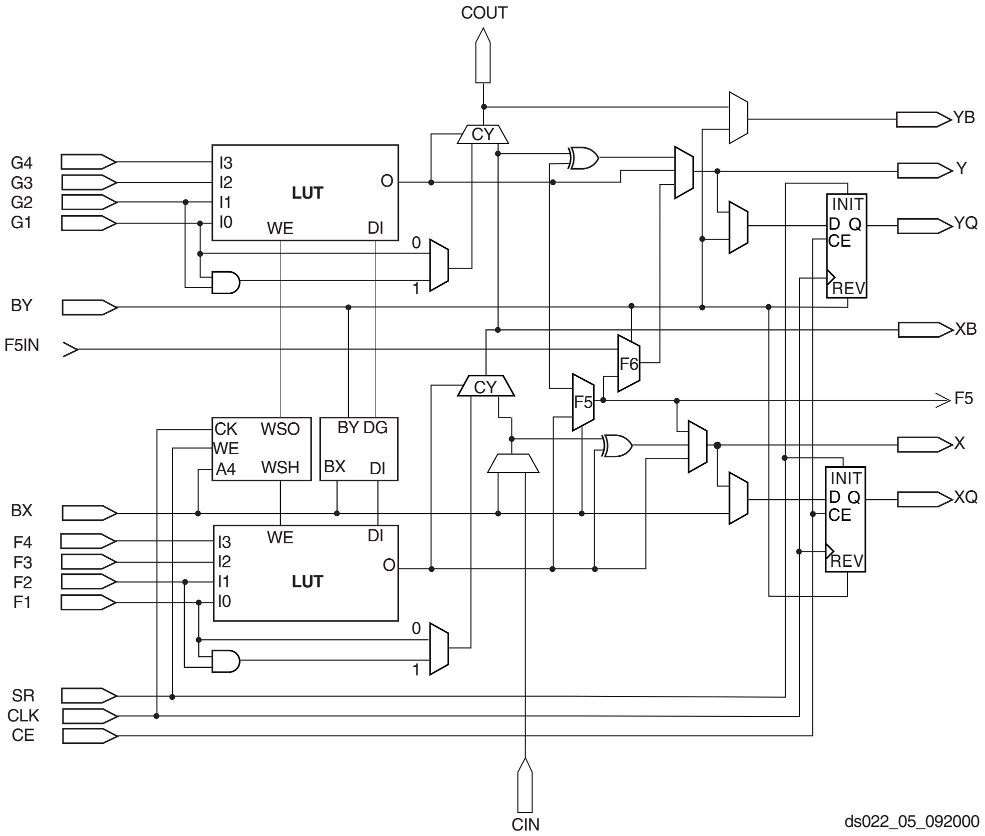

Figure 2: **Detailed View of Virtex-E Slice**

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

			Speed Grade						
			-8		-7		-6		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	320	60	320	60	260	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥25 MHz	5.0		5.0		5.0		ns
		≥50 MHz	3.0		3.0		3.0		ns
		≥100 MHz	2.4		2.4		2.4		ns
		≥150 MHz	2.0		2.0		2.0		ns
		≥200 MHz	1.8		1.8		1.8		ns
		≥250 MHz	1.5		1.5		1.5		ns
		≥300 MHz	1.3		1.3		NA		ns

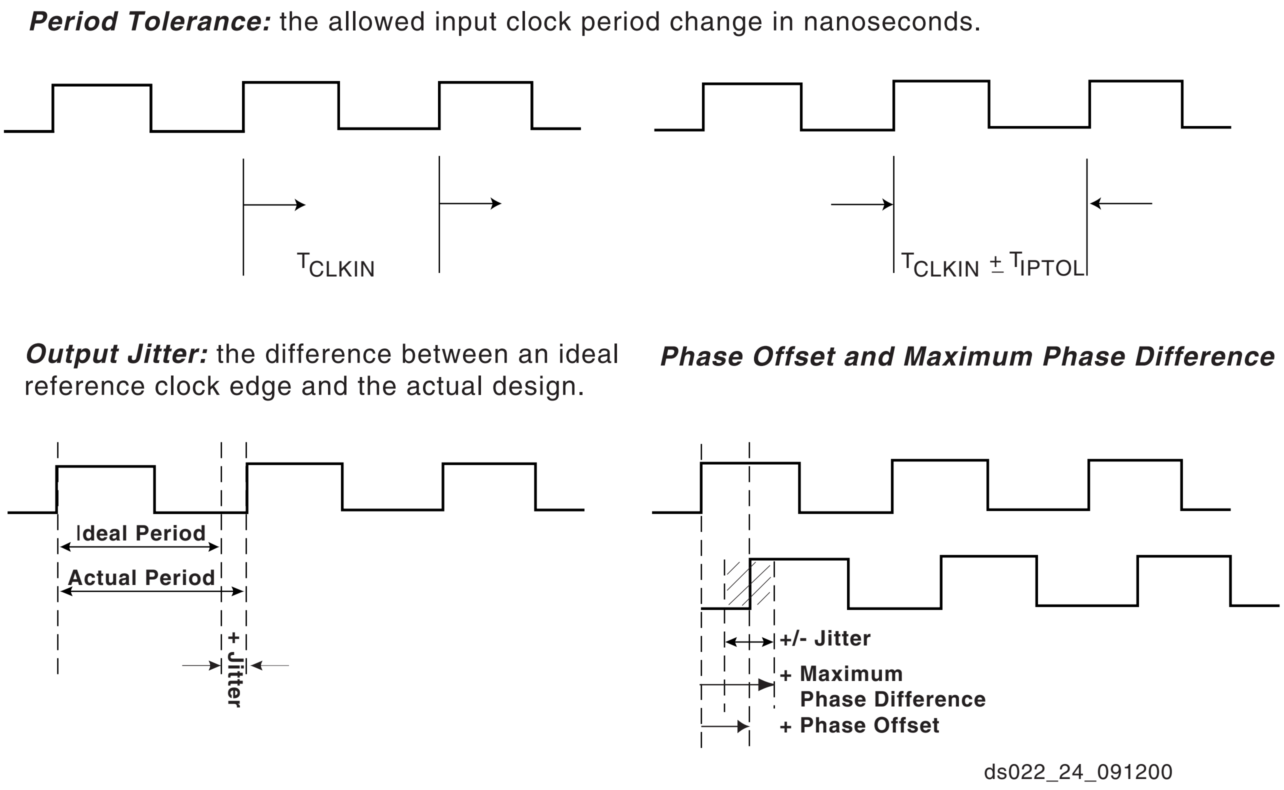

Figure 4: **DLL Timing Waveforms**

Date	Version	Revision
11/20/00	1.3	• Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3). • Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2). • Added to note 2 of **Absolute Maximum Ratings** (Module 3). • Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3). • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters** (Module 3).
04/02/01	1.4	• In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF. • Updated values in Virtex-E Switching Characteristics tables. • Converted data sheet to modularized format. See the Virtex-E Extended Memory Data Sheet section.
04/19/01	1.5	• Updated values in Virtex-E Switching Characteristics tables.
07/23/01	1.6	• Under Absolute Maximum Ratings, changed (T_{SOL}) to 220 °C . • Changes made to SSTL symbol names in IOB Input Switching Characteristics Standard Adjustments table.
07/26/01	1.7	• Removed T_{SOL} parameter and added footnote to Absolute Maximum Ratings table.
09/18/01	1.8	• Reworded power supplies footnote to Absolute Maximum Ratings table.
10/25/01	1.9	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device. • Updated Power-On Power Supply Requirements table.
11/09/01	2.0	• Updated the XCV405E device speed grade designation to Preliminary in Table 1. • Updated Power-On Power Supply Requirements table.
02/01/02	2.1	• Updated footnotes to the DC Input and Output Levels and DLL Clock Tolerance, Jitter, and Phase Information tables.
07/17/02	2.2	• Data sheet designation upgraded from Preliminary to Production. • Removed mention of MIL-M-38510/605 specification. • Added link to XAPP158 from the Power-On Power Supply Requirements section.
09/10/02	2.3	• Revised V_{IN} in Absolute Maximum Ratings Table. Added Clock CLK switching characteristics to "IOB Input Switching Characteristics" on page 5 and "IOB Output Switching Characteristics, Figure 1" on page 7.
12/22/02	2.3.1	• Added footnote regarding V_{IN} PCI compliance to Absolute Maximum Ratings table.
03/14/03	2.3.2	• Under Power-On Power Supply Requirements, the fastest ramp rate is no longer a "suggested" rate.

Virtex-E Extended Memory Data Sheet

The Virtex-E Extended Memory Data Sheet contains the following modules:

- DS025-1, Virtex-E 1.8V Extended Memory FPGAs: Introduction and Ordering Information (Module 1)
- DS025-2, Virtex-E 1.8V Extended Memory FPGAs: Functional Description (Module 2)
- DS025-3, Virtex-E 1.8V Extended Memory FPGAs: **DC and Switching Characteristics (Module 3)**
- DS025-4, Virtex-E 1.8V Extended Memory FPGAs: Pinout Tables (Module 4)

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
4	IO_L92N_YY	AJ6
4	IO_L93P	AK5
4	IO_L93N	AN3
4	IO_L94P_YY	AL5
4	IO_L94N_YY	AJ7
4	IO_VREF_L95P_YY	AM4
4	IO_L95N_YY	AM5
4	IO_L96P_Y	AK7
4	IO_L96N_Y	AL6
4	IO_L97P_YY	AM6
4	IO_L97N_YY	AN6
4	IO_VREF_L98P_YY	AL7
4	IO_L98N_YY	AJ9
4	IO_L99P	AN7
4	IO_L99N	AL8
4	IO_L100P_YY	AM8
4	IO_L100N_YY	AJ10
4	IO_VREF_L101P_YY	AL9[1]
4	IO_L101N_YY	AM9
4	IO_L102P_Y	AK10
4	IO_L102N_Y	AN9
4	IO_VREF_L103P_YY	AL10
4	IO_L103N_YY	AM10
4	IO_L104P_YY	AL11
4	IO_L104N_YY	AJ12
4	IO_L105P	AN11
4	IO_L105N	AK12
4	IO_L106P_YY	AL12
4	IO_L106N_YY	AM12
4	IO_VREF_L107P_YY	AK13[1]
4	IO_L107N_YY	AL13
4	IO_L108P_Y	AM13
4	IO_L108N_Y	AN13
4	IO_L109P_YY	AJ14
4	IO_L109N_YY	AK14
4	IO_VREF_L110P_YY	AM14
4	IO_L110N_YY	AN15
4	IO_L111P	AJ15
4	IO_L111N	AK15
4	IO_L112P_YY	AL15
4	IO_L112N_YY	AM16
4	IO_VREF_L113P_YY	AL16
4	IO_L113N_YY	AJ16
4	IO_L114P_Y	AK16
4	IO_L114N_Y	AN17
4	IO_LVDS_DLL_L115P	AM17
5	GCK1	AJ17
5	IO	AL18
5	IO	AL25
5	IO	AL28
5	IO	AL30
5	IO	AN28
5	IO_LVDS_DLL_L115N	AM18
5	IO_L116P_YY	AK18
5	IO_VREF_L116N_YY	AJ18
5	IO_L117P_YY	AN19
5	IO_L117N_YY	AL19
5	IO_L118P	AK19
5	IO_L118N	AM20
5	IO_L119P_YY	AJ19
5	IO_VREF_L119N_YY	AL20
5	IO_L120P_YY	AN21
5	IO_L120N_YY	AL21
5	IO_L121P_Y	AJ20
5	IO_L121N_Y	AM22
5	IO_L122P_YY	AK21
5	IO_VREF_L122N_YY	AN23[1]
5	IO_L123P_YY	AJ21
5	IO_L123N_YY	AM23
5	IO_L124P	AK22
5	IO_L124N	AM24
5	IO_L125P_YY	AL23
5	IO_L125N_YY	AJ22

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
5	IO_L118N_YY	AD12
5	IO_L119P_YY	AC12
5	IO_VREF_L119N_YY	AB12
5	IO_L120P_YY	AD11
5	IO_L120N_YY	Y12
5	IO_L121P	AB11
5	IO_L121N	AD10
5	IO_L122P_YY	AC11
5	IO_L122N_YY	AE10
5	IO_L123P_YY	AC10
5	IO_L123N_YY	AA11
5	IO_L124P_Y	Y11
5	IO_L124N_Y	AD9
5	IO_L125P_YY	AB10
5	IO_L125N_YY	AF9
5	IO_L126P_YY	AD8
5	IO_VREF_L126N_YY	AA10
5	IO_L127P_YY	AE8
5	IO_L127N_YY	Y10
5	IO_L128P_Y	AC9
5	IO_L128N_Y	AF8
5	IO_L129P_Y	AF7
5	IO_L129N_Y	AB9
5	IO_L130P_YY	AA9
5	IO_L130N_YY	AF6
5	IO_L131P_YY	AC8
5	IO_VREF_L131N_YY	AC7
5	IO_L132P_YY	AD6
5	IO_L132N_YY	Y9
5	IO_L133P_YY	AE5
5	IO_L133N_YY	AA8
5	IO_L134P_YY	AC6
5	IO_VREF_L134N_YY	AB8
5	IO_L135P_YY	AD5
5	IO_L135N_YY	AA7

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
5	IO_L136P_Y	AF4
5	IO_L136N_Y	AC5
6	IO	P3
6	IO	AA3
6	IO	W3
6	IO	Y2
6	IO	Y6
6	IO_L137N_YY	AA5
6	IO_L137P_YY	AC3
6	IO_L138N_YY	AC2
6	IO_L138P_YY	AB4
6	IO_L139N_Y	W6
6	IO_L139P_Y	AA4
6	IO_VREF_L140N_Y	AB3
6	IO_L140P_Y	Y5
6	IO_L141N_Y	AB2
6	IO_L141P_Y	V7
6	IO_L142N_YY	AB1
6	IO_L142P_YY	Y4
6	IO_VREF_L143N_YY	V5
6	IO_L143P_YY	W5
6	IO_L144N_YY	AA1
6	IO_L144P_YY	V6
6	IO_L145N_Y	W4
6	IO_L145P_Y	Y3
6	IO_L146N_Y	Y1
6	IO_L146P_Y	U7
6	IO_L147N_YY	W1
6	IO_L147P_YY	V4
6	IO_L148N_YY	W2
6	IO_VREF_L148P_YY	U6
6	IO_L149N_YY	V3
6	IO_L149P_YY	T5
6	IO_L150N_YY	U5

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
3	IO_L131P_YY	Y22
3	IO_VREF_L131N_YY	AC27
3	IO_L132P	AD28
3	IO_L132N	AB25
3	IO_L133P	AC26
3	IO_L133N	AE30
3	IO_L134P_YY	AD27
3	IO_L134N_YY	AF30
3	IO_L135P_Y	AF29
3	IO_VREF_L135N_Y	AB24
3	IO_L136P	AB23
3	IO_L136N	AE28
3	IO_L138P	AE26
3	IO_L138N	AG29
3	IO_L139P_Y	AH30
3	IO_L139N_Y	AC24
3	IO_D7_L141P_YY	AH29
3	IO_INIT_L141N_YY	AA22
4	GCK0	AJ16
4	IO	AB19
4	IO	AC16
4	IO	AC19
4	IO	AD19
4	IO	AD20
4	IO	AE21
4	IO	AF19
4	IO	AH17
4	IO	AH23
4	IO	AH26
4	IO	AH27
4	IO	AK18
4	IO_VREF_4	AA18
4	IO_L142P_YY	AF27
4	IO_L142N_YY	AK28
4	IO_L144P_Y	AD23
4	IO_L144N_Y	AJ27
4	IO_L145P_Y	AB21
4	IO_L145N_Y	AF25
4	IO_L147P_YY	AA21
4	IO_L147N_YY	AG25
4	IO_VREF_4_L148P_YY	AJ26
4	IO_L148N_YY	AD22
4	IO_L149P	AA20
4	IO_L149N	AH25
4	IO_L150P	AC21
4	IO_L150N	AF24
4	IO_L151P_YY	AG24
4	IO_L151N_YY	AK26
4	IO_VREF_4_L152P_YY	AJ24
4	IO_L152N_YY	AF23
4	IO_L153P	AE23
4	IO_L153N	AB20
4	IO_L154P	AC20
4	IO_L154N	AG23
4	IO_L155P_YY	AF22
4	IO_L155N_YY	AE22
4	IO_VREF_4_L156P_YY	AJ22
4	IO_L156N_YY	AG22
4	IO_L158P	AA19
4	IO_L158N	AF21
4	IO_L160P	AG21
4	IO_L160N	AK23
4	IO_L162P_Y	AE20
4	IO_L162N_Y	AJ21
4	IO_L163P_Y	AG20
4	IO_L163N_Y	AF20
4	IO_L165P_YY	AJ20

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
113	3	U24	V29	√	VREF
114	3	W30	U22	-	-
115	3	U21	W29	-	-
116	3	V26	W27	√	-
117	3	W26	Y29	√	VREF
118	3	W25	Y30	-	-
120	3	AA30	W24	-	-
121	3	AA29	V20	√	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	-	-
126	3	W22	Y23	-	-
127	3	Y24	AB28	-	VREF
128	3	AC30	AA25	-	-
129	3	W21	AA24	√	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	-	-
133	3	AC26	AE30	-	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	√	VREF
136	3	AB23	AE28	-	-
138	3	AE26	AG29	-	-
139	3	AH30	AC24	√	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
144	4	AD23	AJ27	√	-
145	4	AB21	AF25	√	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	-	-
150	4	AC21	AF24	-	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	-	-
154	4	AC20	AG23	-	-
155	4	AF22	AE22	√	-
156	4	AJ22	AG22	√	VREF
158	4	AA19	AF21	-	-
160	4	AG21	AK23	-	-
162	4	AE20	AJ21	√	-
163	4	AG20	AF20	√	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	-	-
168	4	AJ19	AD17	-	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	-	-
172	4	AK19	AD16	-	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
176	4	AG16	AK17	-	-
177	5	AF16	AH16	-	GCLK LVDS 1/0
179	5	AB15	AF15	-	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	-	-
183	5	AH14	AJ14	-	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	-	-
187	5	AC13	AA13	-	-
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
191	5	AG11	AF11	√	-
192	5	AH11	AJ11	√	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	-	-
197	5	AJ9	AE9	-	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	-	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
201	5	AC11	AG8	-	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	-	-
205	5	AH6	AC10	-	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
209	5	AC9	AJ4	√	-
210	5	AG5	AK4	√	-
212	6	AC6	AF3	√	-
214	6	AE4	AB9	√	-
215	6	AH1	AE3	-	-
217	6	AA10	AG1	-	-
218	6	AD4	AA9	√	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	-	-
221	6	AA7	AA8	-	-
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	√	-
225	6	AB4	Y8	-	-
226	6	W9	AB3	-	VREF
228	6	V10	AB1	-	-
230	6	AA3	V11	-	-
232	6	AA6	W7	√	-
233	6	Y4	Y6	-	-
235	6	Y2	Y3	-	-
236	6	W5	Y5	√	VREF
237	6	W6	W4	√	-
238	6	W2	V6	-	-
239	6	V4	U9	-	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	√	-
243	6	U3	T7	-	-
244	6	V2	T5	-	VREF
246	6	U2	T4	-	-
247	7	R10	T1	-	IRDY
249	7	R4	R8	-	-
250	7	R3	R7	-	-
251	7	P6	P10	-	VREF
252	7	P2	P5	-	-
253	7	P4	P7	√	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF
256	7	N6	M6	-	-
257	7	N1	N5	-	-
258	7	M5	M4	√	-
259	7	M1	M2	√	VREF
260	7	L2	L4	-	-
262	7	M8	L1	-	-
263	7	M9	K2	√	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	-	-
268	7	J5	L8	-	-
269	7	H4	K6	-	VREF
270	7	K7	H1	-	-
271	7	J2	J7	√	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	-	-
275	7	E1	G3	-	-
276	7	E2	H6	√	-
277	7	K9	E4	√	VREF
278	7	F4	J8	-	-
280	7	C2	G6	-	-
281	7	F5	D2	-	-