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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	2400
Number of Logic Elements/Cells	10800
Total RAM Bits	573440
Number of I/O	404
Number of Gates	129600
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv405e-8bg560c

Table 1: **Supported I/O Standards**

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. After configuration, clamping diodes are connected to V_{CCO} with the exception of LVCMOS18, LVCMOS25, GTL, GTL+, LVDS, and LVPECL.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but IOs can optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking" on page 2.

There are optional pull-up and pull-down resistors at each user I/O input for use after configuration. Their value is in the range 50 - 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See "I/O Banking" on page 2.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in Figure 15.

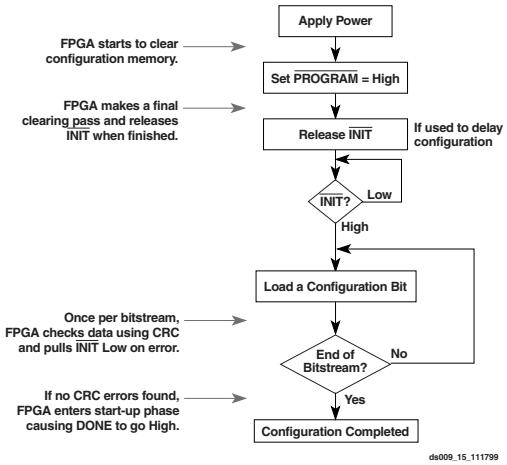

Figure 15: **Serial Configuration Flowchart**

Figure 16 shows the timing of master-serial configuration. Master-serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 16

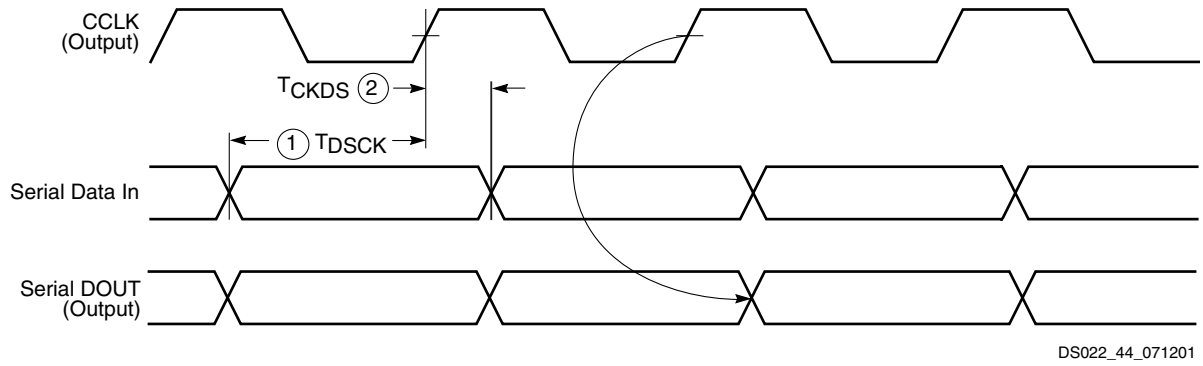

Figure 16: **Master-Serial Mode Programming Switching Characteristics**

At power-up, V_{CC} must rise from 1.0 V to V_{CC} min in less than 50 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If $\overline{\text{WRITE}}$ is not asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port can be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent SelectMAP-port pins from being used as user I/O.

Multiple Virtex-E FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. See Table 11 for SelectMAP Write Timing Characteristics.

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of $\overline{\text{CS}}$, illustrated in Figure 17.

1. Assert $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain

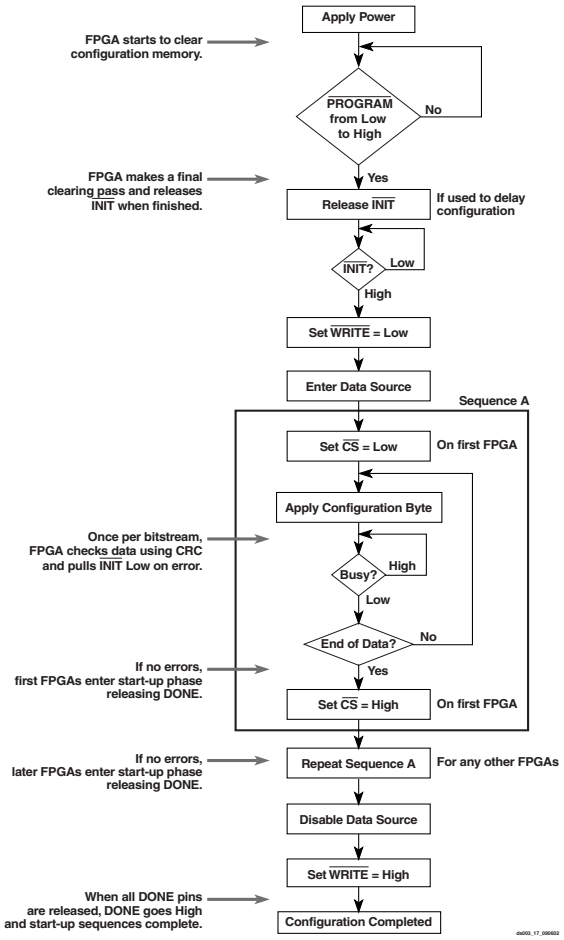

Figure 18: **SelectMAP Flowchart for Write Operations**

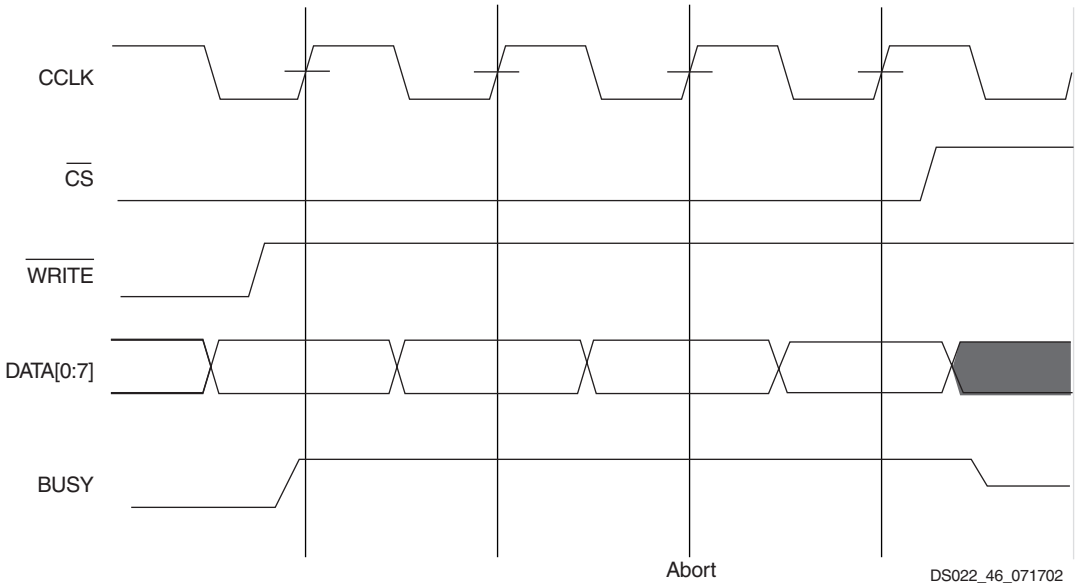

Figure 19: **SelectMAP Write Abort Waveforms**

Boundary-Scan Mode

In the boundary-scan mode, configuration is done through the IEEE 1149.1 Test Access Port. Note that the PROGRAM pin must be pulled High prior to reconfiguration. A Low on the PROGRAM pin resets the TAP controller and no JTAG operations can be performed.

VHDL Instantiation

```
data0_p:   IOBUF_LVDS port map
(I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));

data0_inv: INV        port map
(I=>data_out(0),   O=>data_n_out(0));

data0_n  : IOBUF_LVDS port map
(I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

Verilog Instantiation

```
IOBUF_LVDS data0_p(.I(data_out[0]),
.T(data_tri), .IO(data_p[0]),
.O(data_int[0]);

INV        data0_inv (.I(data_out[0],
.O(data_n_out[0]);

IOBUF_LVDS
data0_n(.I(data_n_out[0]),.T(data_tri),.
IO(data_n[0]).O());
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the UCF or NCF file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB), then any IO_L#PIN pair can be used. If the output side of the bidirectional buffers are asynchronous (no output register), then they must use one of the pairs that is a part of the asynchronous LVDS IOB group. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that can be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product's lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE), and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the "map -pr [i|o|b]", where "i" is inputs only, "o" is outputs only, and "b" is both inputs and outputs. To improve design coding times, VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 44.

The 3-state is configured to be 3-stated at GSR and when the PRE, CLR, S, or R is asserted and shares its clock enable with the output and input register. If this is not desirable, then the library can be updated with the desired functionality by the user. The I/O and IOB inputs to the macros are the external net connections.

Table 44: **Bidirectional I/O Library Macros**

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q

Virtex-E Switching Characteristics

All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.

			Speed Grade(2)				
Description(1)	**Symbol**	**Device**	**Min**	**-8**	**-7**	**-6**	**Units**
Propagation Delays							
Pad to I output, no delay	T_{IOPI}	All	0.43	0.8	0.8	0.8	ns, max
Pad to I output, with delay	T_{IOPID}	XCV405E	0.51	1.0	1.0	1.0	ns, max
		XCV812E	0.55	1.1	1.1	1.1	ns, max
Pad to output IQ via transparent latch, no delay	T_{IOPLI}	All	0.75	1.4	1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	T_{IOPLID}	XCV405E	1.55	3.5	3.6	3.7	ns, max
		XCV812E	1.55	3.5	3.6	3.7	ns, max
Propagation Delays							
Clock							
Minimum Pulse Width, High	T_{CH}	All	0.56	1.2	1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}		0.56	1.2	1.3	1.4	ns, min
Clock CLK to output IQ	T_{IOCKIQ}		0.18	0.4	0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register							
Pad, no delay	T_{IOPICK} / T_{IOICKP}	All	0.69 / 0	1.3 / 0	1.4 / 0	1.5 / 0	ns, min
Pad, with delay	$T_{IOPICKD}$ / $T_{IOICKPD}$	XCV405E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
		XCV812E	1.49 / 0	3.4 / 0	3.5 / 0	3.5 / 0	ns, min
ICE input	$T_{IOICECK}$ / $T_{IOCKICE}$	All	0.28 / 0.0	0.55 / 0.01	0.7 / 0.01	0.7 / 0.01	ns, min
SR input (IFF, synchronous)	$T_{IOSRCKI}$	All	0.38	0.8	0.9	1.0	ns, min
Set/Reset Delays							
SR input to IQ (asynchronous)	T_{IOSRIQ}	All	0.54	1.1	1.2	1.4	ns, max
GSR to output IQ	T_{GSRQ}	All	3.88	7.6	8.5	9.7	ns, max

Notes:
1. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
2. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

			Speed Grade				
Description	**Symbol**	**Standard**	**Min**	**-8**	**-7**	**-6**	**Units**
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	+14.7	+14.7	+14.7	ns
	T_{OLVTTL_S4}	4 mA	2.5	+7.5	+7.5	+7.5	ns
	T_{OLVTTL_S6}	6 mA	1.8	+4.8	+4.8	+4.8	ns
	T_{OLVTTL_S8}	8 mA	1.2	+3.0	+3.0	+3.0	ns
	T_{OLVTTL_S12}	12 mA	1.0	+1.9	+1.9	+1.9	ns
	T_{OLVTTL_S16}	16 mA	0.9	+1.7	+1.7	+1.7	ns
	T_{OLVTTL_S24}	24 mA	0.8	+1.3	+1.3	+1.3	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA	1.9	+13.1	+13.1	+13.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	+5.3	+5.3	+5.3	ns
	T_{OLVTTL_F6}	6 mA	0.20	+3.1	+3.1	+3.1	ns
	T_{OLVTTL_F8}	8 mA	0.10	+1.0	+1.0	+1.0	ns
	T_{OLVTTL_F12}	12 mA	0.0	0.0	0.0	0.0	ns
	T_{OLVTTL_F16}	16 mA	–0.10	–0.05	–0.05	–0.05	ns
	T_{OLVTTL_F24}	24 mA	–0.10	–0.20	–0.20	–0.20	ns
	$T_{OLVCMOS\_2}$	LVCMOS2	0.10	+0.09	+0.09	+0.09	ns
	$T_{OLVCMOS\_18}$	LVCMOS18	0.10	+0.7	+0.7	+0.7	ns
	T_{OLVDS}	LVDS	–0.39	–1.2	–1.2	–1.2	ns
	$T_{OLVPECL}$	LVPECL	–0.20	–0.41	–0.41	–0.41	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	+2.3	+2.3	+2.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	–0.41	–0.41	–0.41	ns
	T_{OGTL}	GTL	0.6	+0.49	+0.49	+0.49	ns
	T_{OGTLP}	GTL+	0.7	+0.8	+0.8	+0.8	ns
	T_{OHSTL_I}	HSTL I	0.10	–0.51	–0.51	–0.51	ns
	T_{OHSTL_IIII}	HSTL III	–0.10	–0.91	–0.91	–0.91	ns
	T_{OHSTL_IV}	HSTL IV	–0.20	–1.01	–1.01	–1.01	ns
	T_{OSSTL2_I}	SSTL2 I	–0.10	–0.51	–0.51	–0.51	ns
	T_{OSSTL2_II}	SSTL2 II	–0.20	–0.91	–0.91	–0.91	ns
	T_{OSSTL3_I}	SSTL3 I	–0.20	–0.51	–0.51	–0.51	ns
	T_{OSSTL3_II}	SSTL3 II	–0.30	–1.01	–1.01	–1.01	ns
	T_{OCTT}	CTT	0.0	–0.61	–0.61	–0.61	ns
	T_{OAGP}	AGP	–0.1	–0.91	–0.91	–0.91	ns

CLB Distributed RAM Switching Characteristics

Description[1]	Symbol	Speed Grade				Units
		Min	-8	-7	-6	
Sequential Delays						
Clock CLK to X/Y outputs (WE active) 16 x 1 mode	$T_{SHCKO16}$	0.67	1.38	1.5	1.7	ns, max
Clock CLK to X/Y outputs (WE active) 32 x 1 mode	$T_{SHCKO32}$	0.84	1.66	1.9	2.1	ns, max
Shift-Register Mode Clock CLK to X/Y outputs	T_{REG}	1.25	2.39	2.9	3.2	ns, max
Setup and Hold Times before/after Clock CLK						
F/G address inputs	T_{AS}/T_{AH}	0.19 / 0	0.38 / 0	0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.44 / 0	0.87 / 0	0.97 / 0	1.09 / 0	ns, min
SR input (WE)	T_{WS}/T_{WH}	0.29 / 0	0.57 / 0	0.7 / 0	0.8 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	0.96	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}	0.96	1.9	2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	1.92	3.8	4.2	4.8	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.0	1.9	2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.0	1.9	2.1	2.4	ns, min

Notes:
1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

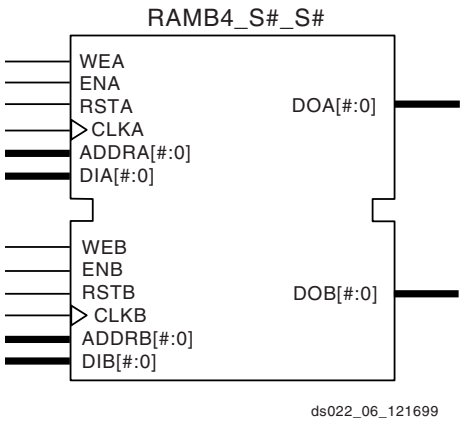

Figure 3: **Dual-Port Block SelectRAM**

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
2	IO_L61N_Y	N3
2	IO_L62P_Y	N2
2	IO_L62N_Y	P5
2	IO_VREF_L63P_YY	P4
2	IO_D3_L63N_YY	P3
2	IO_L64P_Y	P2
2	IO_L64N_Y	R5
2	IO_L65P_Y	R4
2	IO_L65N_Y	R3
2	IO_VREF_L66P_Y	R1
2	IO_L66N_Y	T4
2	IO_L67P_Y	T5
2	IO_L67N_Y	T3
2	IO_L68P_YY	T2
2	IO_L68N_YY	U3
3	IO	U4
3	IO	AE3
3	IO	AF3
3	IO	AH3
3	IO	AK3
3	IO_L69P_Y	U1
3	IO_L69N_Y	U2
3	IO_L70P_Y	V2
3	IO_VREF_L70N_Y	V4
3	IO_L71P_Y	V5
3	IO_L71N_Y	V3
3	IO_L72P	W1
3	IO_L72N	W3
3	IO_D4_L73P_YY	W4
3	IO_VREF_L73N_YY	W5
3	IO_L74P_Y	Y3
3	IO_L74N_Y	Y4
3	IO_L75P	AA1
3	IO_L75N	Y5
3	IO_L76P_Y	AA3
3	IO_VREF_L76N_Y	AA4[1]

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
3	IO_L77P	AB3
3	IO_L77N	AA5
3	IO_L78P	AC1
3	IO_L78N	AB4
3	IO_L79P_YY	AC3
3	IO_D5_L79N_YY	AB5
3	IO_D6_L80P_YY	AC4
3	IO_VREF_L80N_YY	AD3
3	IO_L81P_Y	AE1
3	IO_L81N_Y	AC5
3	IO_L82P_YY	AD4
3	IO_VREF_L82N_YY	AF1[1]
3	IO_L83P_Y	AF2
3	IO_L83N_Y	AD5
3	IO_L84P_Y	AG2
3	IO_L84N_Y	AE4
3	IO_L85P_YY	AH1
3	IO_VREF_L85N_YY	AE5
3	IO_L86P_Y	AF4
3	IO_L86N_Y	AJ1
3	IO_L87P_Y	AJ2
3	IO_L87N_Y	AF5
3	IO_L88P_Y	AG4
3	IO_VREF_L88N_Y	AK2
3	IO_L89P_Y	AJ3
3	IO_L89N_Y	AG5
3	IO_L90P_Y	AL1
3	IO_L90N_Y	AH4
3	IO_D7_L91P_YY	AJ4
3	IO_INIT_L91N_YY	AH5
4	GCK0	AL17
4	IO	AJ8
4	IO	AJ11
4	IO	AK6
4	IO	AK9
4	IO_L92P_YY	AL4

Table 5: FG900 Fine-Pitch BGA Package — XCV812E

Bank	Description	Pin
4	IO_L165N_YY	AE19
4	IO_VREF_4_L166P_YY	AK22
4	IO_L166N_YY	AH20
4	IO_L167P	AG19
4	IO_L167N	AB17
4	IO_L168P	AJ19
4	IO_L168N	AD17
4	IO_L169P_YY	AA16
4	IO_L169N_YY	AA17
4	IO_VREF_4_L170P_YY	AK21
4	IO_L170N_YY	AB16
4	IO_L171P	AG18
4	IO_L171N	AK20
4	IO_L172P	AK19
4	IO_L172N	AD16
4	IO_L173P_YY	AE16
4	IO_L173N_YY	AE17
4	IO_VREF_4_L174P_YY	AG17
4	IO_L174N_YY	AJ17
4	IO_L176P	AG16
4	IO_L176N	AK17
4	IO_LVDS_DLL_L177P	AF16
5	GCK1	AK16
5	IO	AD8
5	IO	AD14
5	IO	AE10
5	IO	AE12
5	IO	AG15
5	IO	AH5
5	IO	AH8
5	IO	AK12
5	IO_LVDS_DLL_L177N	AH16
5	IO_L179P	AB15

Table 5: FG900 Fine-Pitch BGA Package — XCV812E

Bank	Description	Pin
5	IO_L179N	AF15
5	IO_L180P_YY	AA15
5	IO_VREF_5_L180N_YY	AF14
5	IO_L181P_YY	AH15
5	IO_L181N_YY	AK15
5	IO_L182P	AB14
5	IO_L182N	AF13
5	IO_L183P	AH14
5	IO_L183N	AJ14
5	IO_L184P_YY	AE14
5	IO_VREF_5_L184N_YY	AG13
5	IO_L185P_YY	AK13
5	IO_L185N_YY	AD13
5	IO_L186P	AE13
5	IO_L186N	AF12
5	IO_L187P	AC13
5	IO_L187N	AA13
5	IO_L188P_YY	AA12
5	IO_VREF_5_L188N_YY	AJ12
5	IO_L189P_YY	AB12
5	IO_L189N_YY	AE11
5	IO_L191P_Y	AG11
5	IO_L191N_Y	AF11
5	IO_L192P_Y	AH11
5	IO_L192N_Y	AJ11
5	IO_L194P_YY	AD12
5	IO_L194N_YY	AK11
5	IO_L195P_YY	AJ10
5	IO_VREF_5_L195N_YY	AC12
5	IO_L196P	AK10
5	IO_L196N	AD11
5	IO_L197P	AJ9
5	IO_L197N	AE9
5	IO_L198P_YY	AH10

Table 5: FG900 Fine-Pitch BGA Package — XCV812E

Bank	Description	Pin
5	IO_VREF_5_L198N_YY	AF9
5	IO_L199P_YY	AH9
5	IO_L199N_YY	AK9
5	IO_L200P	AF8
5	IO_L200N	AB11
5	IO_L201P	AC11
5	IO_L201N	AG8
5	IO_L202P_YY	AK8
5	IO_VREF_5_L202N_YY	AF7
5	IO_L203P_YY	AG7
5	IO_L203N_YY	AK7
5	IO_L204P	AJ7
5	IO_L204N	AD10
5	IO_L205P	AH6
5	IO_L205N	AC10
5	IO_L206P_YY	AD9
5	IO_VREF_5_L206N_YY	AG6
5	IO_L207P_YY	AB10
5	IO_L207N_YY	AJ5
5	IO_L209P_Y	AC9
5	IO_L209N_Y	AJ4
5	IO_L210P_Y	AG5
5	IO_L210N_Y	AK4
6	IO	T6
6	IO	U1
6	IO	U6
6	IO	V7
6	IO	V8
6	IO	W10
6	IO	Y10
6	IO	AA2
6	IO	AA4
6	IO	AD1

Table 5: FG900 Fine-Pitch BGA Package — XCV812E

Bank	Description	Pin
6	IO	AD6
6	IO	AG2
6	IO_L212N_YY	AF3
6	IO_L212P_YY	AC6
6	IO_L214N_Y	AB9
6	IO_L214P_Y	AE4
6	IO_L215N	AE3
6	IO_L215P	AH1
6	IO_L217N	AG1
6	IO_L217P	AA10
6	IO_VREF_L218N_Y	AA9
6	IO_L218P_Y	AD4
6	IO_L219N_YY	AD5
6	IO_L219P_YY	AD2
6	IO_L220N	AD3
6	IO_L220P	AF2
6	IO_L221N	AA8
6	IO_L221P	AA7
6	IO_VREF_L222N_YY	AF1
6	IO_L222P_YY	Y9
6	IO_L223N_YY	AB6
6	IO_L223P_YY	AC4
6	IO_L224N_Y	AE1
6	IO_L224P_Y	W8
6	IO_L225N	Y8
6	IO_L225P	AB4
6	IO_VREF_L226N	AB3
6	IO_L226P	W9
6	IO_L228N	AB1
6	IO_L228P	V10
6	IO_VREF	AC1
6	IO_L230N	V11
6	IO_L230P	AA3
6	IO_L232N_Y	W7

Table 5: FG900 Fine-Pitch BGA Package — XCV812E

Bank	Description	Pin
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13
NA	VCCO_0	C12
NA	VCCO_1	B25
NA	VCCO_1	C19
NA	VCCO_1	M18
NA	VCCO_1	M17
NA	VCCO_1	L17
NA	VCCO_1	H17
NA	VCCO_1	L16
NA	VCCO_1	M16
NA	VCCO_2	F29
NA	VCCO_2	M28
NA	VCCO_2	P23
NA	VCCO_2	R20
NA	VCCO_2	P20
NA	VCCO_2	R19

Table 5: FG900 Fine-Pitch BGA Package — XCV812E

Bank	Description	Pin
NA	VCCO_2	N19
NA	VCCO_2	P19
NA	VCCO_3	AE29
NA	VCCO_3	W28
NA	VCCO_3	U23
NA	VCCO_3	U20
NA	VCCO_3	T20
NA	VCCO_3	V19
NA	VCCO_3	T19
NA	VCCO_3	U19
NA	VCCO_4	AJ25
NA	VCCO_4	AH19
NA	VCCO_4	W18
NA	VCCO_4	AC17
NA	VCCO_4	Y17
NA	VCCO_4	W17
NA	VCCO_4	W16
NA	VCCO_4	Y16
NA	VCCO_5	AJ6
NA	VCCO_5	Y15
NA	VCCO_5	W15
NA	VCCO_5	AC14
NA	VCCO_5	Y14
NA	VCCO_5	W14
NA	VCCO_5	W13
NA	VCCO_5	AH12
NA	VCCO_6	AE2
NA	VCCO_6	V12
NA	VCCO_6	U12
NA	VCCO_6	T12
NA	VCCO_6	U11
NA	VCCO_6	T11
NA	VCCO_6	U8
NA	VCCO_6	W3

Table 5: FG900 Fine-Pitch BGA Package — XCV812E

Bank	Description	Pin
NA	GND	AC8
NA	GND	H8
NA	GND	AD7
NA	GND	B8
NA	GND	AE6
NA	GND	G7
NA	GND	F6
NA	GND	AF5
NA	GND	E5
NA	GND	AG4
NA	GND	D4
NA	GND	V3
NA	GND	N3
NA	GND	C3
NA	GND	AK2
NA	GND	AH3
NA	GND	AC2
NA	GND	H2
NA	GND	B2
NA	GND	A2
NA	GND	AK1
NA	GND	AJ2
NA	GND	AJ1
NA	GND	A1
NA	GND	B1

FG900 Differential Pin Pairs

Virtex-E Extended Memory devices have differential pin pairs that can also provide other functions when not used as a differential pair. A √ in the AO column indicates that the pin pair can be used as an asynchronous output for all devices provided in this package.

Pairs with a note number in the AO column are device dependent. They can have asynchronous outputs if the pin pair is in the same CLB row and column in the device. Numbers in this column refer to footnotes that indicate which devices have pin pairs that can be asynchronous outputs. The Other Functions column indicates alternative function(s) not available when the pair is used as a differential pair or differential clock.

Table 6: FG900 Differential Pin Pair Summary — XCV812E

Pair	Bank	P Pin	N Pin	AO	Other Functions
GCLK LVDS					
3	0	C15	A15	NA	IO LVDS 34
2	1	E15	E16	NA	IO LVDS 34
1	5	AK16	AH16	NA	IO LVDS 177
0	4	AJ16	AF16	NA	IO LVDS 177
IO LVDS Total Pairs: 235, Asynchronous Output Pairs: 85					
1	0	G8	D5	√	-
2	0	H9	A3	√	-
4	0	D6	A4	√	-
5	0	B5	E7	√	VREF
6	0	F8	A5	-	-
7	0	N11	D7	-	-
8	0	E8	G9	√	-
9	0	J11	A6	√	VREF
10	0	B7	C7	-	-
11	0	H10	C8	-	-
12	0	F10	G10	√	-
13	0	H11	A8	√	VREF
15	0	J12	B9	-	-
17	0	B10	G11	-	-
19	0	F11	H13	√	-
20	0	D11	E11	√	-
22	0	C11	F12	√	-
23	0	D12	A10	√	VREF
24	0	A11	E12	-	-

2	IO_L97P	N25
2	IO_L97N	N27
2	IO_VREF_L98P_YY	N30
2	IO_D3_L98N_YY	P21
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P_Y	P29
2	IO_L100N_Y	N24
2	IO_L101P	P22
2	IO_L101N	R26
2	IO_VREF_2_L102P	P25

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
5	IO_VREF_5_L198N_YY	AF9
5	IO_L199P_YY	AH9
5	IO_L199N_YY	AK9
5	IO_L200P	AF8
5	IO_L200N	AB11
5	IO_L201P	AC11
5	IO_L201N	AG8
5	IO_L202P_YY	AK8
5	IO_VREF_5_L202N_YY	AF7
5	IO_L203P_YY	AG7
5	IO_L203N_YY	AK7
5	IO_L204P	AJ7
5	IO_L204N	AD10
5	IO_L205P	AH6
5	IO_L205N	AC10
5	IO_L206P_YY	AD9
5	IO_VREF_5_L206N_YY	AG6
5	IO_L207P_YY	AB10
5	IO_L207N_YY	AJ5
5	IO_L209P_Y	AC9
5	IO_L209N_Y	AJ4
5	IO_L210P_Y	AG5
5	IO_L210N_Y	AK4
6	IO	T6
6	IO	U1
6	IO	U6
6	IO	V7
6	IO	V8
6	IO	W10
6	IO	Y10
6	IO	AA2
6	IO	AA4
6	IO	AD1

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
6	IO	AD6
6	IO	AG2
6	IO_L212N_YY	AF3
6	IO_L212P_YY	AC6
6	IO_L214N_Y	AB9
6	IO_L214P_Y	AE4
6	IO_L215N	AE3
6	IO_L215P	AH1
6	IO_L217N	AG1
6	IO_L217P	AA10
6	IO_VREF_L218N_Y	AA9
6	IO_L218P_Y	AD4
6	IO_L219N_YY	AD5
6	IO_L219P_YY	AD2
6	IO_L220N	AD3
6	IO_L220P	AF2
6	IO_L221N	AA8
6	IO_L221P	AA7
6	IO_VREF_L222N_YY	AF1
6	IO_L222P_YY	Y9
6	IO_L223N_YY	AB6
6	IO_L223P_YY	AC4
6	IO_L224N_Y	AE1
6	IO_L224P_Y	W8
6	IO_L225N	Y8
6	IO_L225P	AB4
6	IO_VREF_L226N	AB3
6	IO_L226P	W9
6	IO_L228N	AB1
6	IO_L228P	V10
6	IO_VREF	AC1
6	IO_L230N	V11
6	IO_L230P	AA3
6	IO_L232N_Y	W7

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
7	IO_VREF_L266P_YY	K3
7	IO_L267N	L7
7	IO_L267P	K4
7	IO_L268N	L8
7	IO_L268P	J5
7	IO_L269N	K6
7	IO_VREF_L269P	H4
7	IO_L270N	H1
7	IO_L270P	K7
7	IO_L271N_Y	J7
7	IO_L271P_Y	J2
7	IO_L272N_YY	H5
7	IO_L272P_YY	G2
7	IO_L273N_YY	L9
7	IO_VREF_L273P_YY	G5
7	IO_L274N	F3
7	IO_L274P	K8
7	IO_L275N	G3
7	IO_L275P	E1
7	IO_L276N_YY	H6
7	IO_L276P_YY	E2
7	IO_L277N_Y	E4
7	IO_VREF_L277P_Y	K9
7	IO_L278N	J8
7	IO_L278P	F4
7	IO_L280N	G6
7	IO_L280P	C2
7	IO_L281N_Y	D2
7	IO_L281P_Y	F5
2	DONE	AJ28
NA	DXN	AJ3
NA	DXP	AH4
3	CCLK	F26

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	M0	AF4
NA	M1	AC7
NA	M2	AK3
NA	PROGRAM	AG28
NA	TCK	B3
NA	TDI	H22
2	TDO	D26
NA	TMS	C1
NA	VCCINT	L11
NA	VCCINT	L12
NA	VCCINT	L19
NA	VCCINT	L20
NA	VCCINT	M11
NA	VCCINT	M12
NA	VCCINT	M19
NA	VCCINT	M20
NA	VCCINT	N13
NA	VCCINT	N14
NA	VCCINT	N15
NA	VCCINT	N16
NA	VCCINT	N17
NA	VCCINT	N18
NA	VCCINT	P13
NA	VCCINT	P18
NA	VCCINT	R13
NA	VCCINT	R18
NA	VCCINT	T13
NA	VCCINT	T18
NA	VCCINT	U18
NA	VCCINT	U13
NA	VCCINT	V13
NA	VCCINT	V14
NA	VCCINT	V15

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	VCCINT	V16
NA	VCCINT	V17
NA	VCCINT	V18
NA	VCCINT	W11
NA	VCCINT	W12
NA	VCCINT	W19
NA	VCCINT	W20
NA	VCCINT	Y11
NA	VCCINT	Y12
NA	VCCINT	Y19
NA	VCCINT	Y20
NA	VCCO_0	B6
NA	VCCO_0	M15
NA	VCCO_0	M14
NA	VCCO_0	L15
NA	VCCO_0	L14
NA	VCCO_0	H14
NA	VCCO_0	M13
NA	VCCO_0	C12
NA	VCCO_1	B25
NA	VCCO_1	C19
NA	VCCO_1	M18
NA	VCCO_1	M17
NA	VCCO_1	L17
NA	VCCO_1	H17
NA	VCCO_1	L16
NA	VCCO_1	M16
NA	VCCO_2	F29
NA	VCCO_2	M28
NA	VCCO_2	P23
NA	VCCO_2	R20
NA	VCCO_2	P20
NA	VCCO_2	R19

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
NA	VCCO_2	N19
NA	VCCO_2	P19
NA	VCCO_3	AE29
NA	VCCO_3	W28
NA	VCCO_3	U23
NA	VCCO_3	U20
NA	VCCO_3	T20
NA	VCCO_3	V19
NA	VCCO_3	T19
NA	VCCO_3	U19
NA	VCCO_4	AJ25
NA	VCCO_4	AH19
NA	VCCO_4	W18
NA	VCCO_4	AC17
NA	VCCO_4	Y17
NA	VCCO_4	W17
NA	VCCO_4	W16
NA	VCCO_4	Y16
NA	VCCO_5	AJ6
NA	VCCO_5	Y15
NA	VCCO_5	W15
NA	VCCO_5	AC14
NA	VCCO_5	Y14
NA	VCCO_5	W14
NA	VCCO_5	W13
NA	VCCO_5	AH12
NA	VCCO_6	AE2
NA	VCCO_6	V12
NA	VCCO_6	U12
NA	VCCO_6	T12
NA	VCCO_6	U11
NA	VCCO_6	T11
NA	VCCO_6	U8
NA	VCCO_6	W3