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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4704
Number of Logic Elements/Cells	21168
Total RAM Bits	1146880
Number of I/O	404
Number of Gates	254016
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv812e-7bg560c

IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

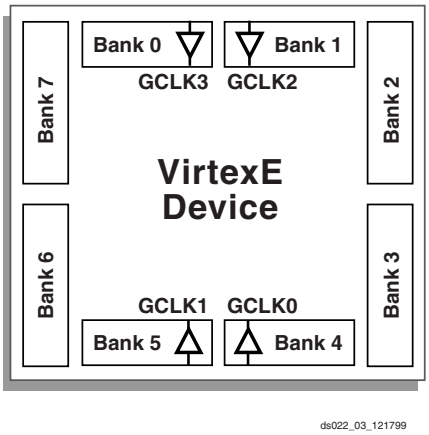

Figure 3: **Virtex-E I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8 V	LVCMOS18, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank.

In Virtex-E, input buffers with LVTTL, LVCMOS2, LVCMOS18, PCI33_3, PCI66_3 standards are supplied by V_{CCO} rather than V_{CCINT}. For these standards, only input and output buffers that have the same V_{CCO} can be mixed together.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a super set of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or they can be connected to the V_{CCO} voltage to permit migration to a larger device, if necessary.

Configurable Logic Block

The basic building block of the Virtex-E CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex-E CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

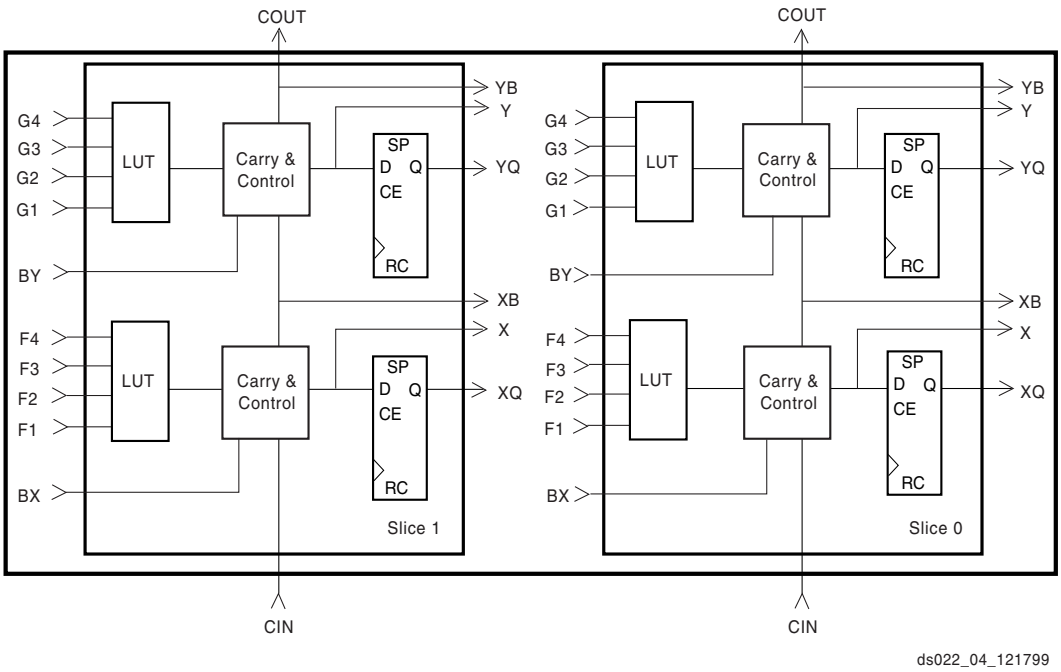

Figure 4: **2-Slice Virtex-E CLB**

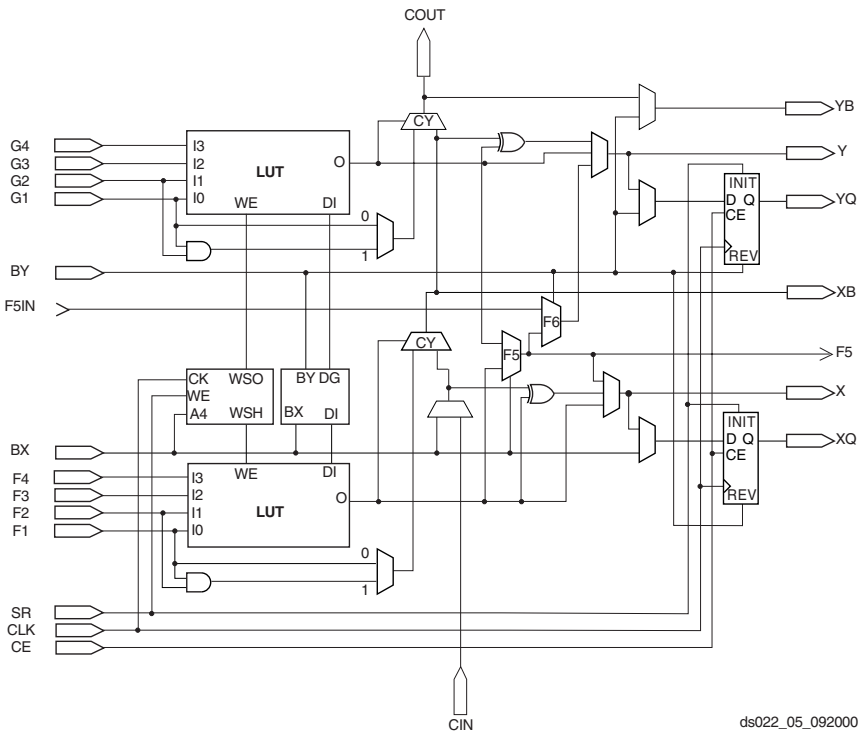

Figure 5: **Detailed View of Virtex-E Slice**

In addition to the four basic LCs, the Virtex-E CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex-E function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be com-

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or <001> on the mode pins (M2, M1, M0). For details on TAP characteristics, refer to XAPP139.

Configuration Sequence

The configuration of Virtex-E devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process can also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 20.

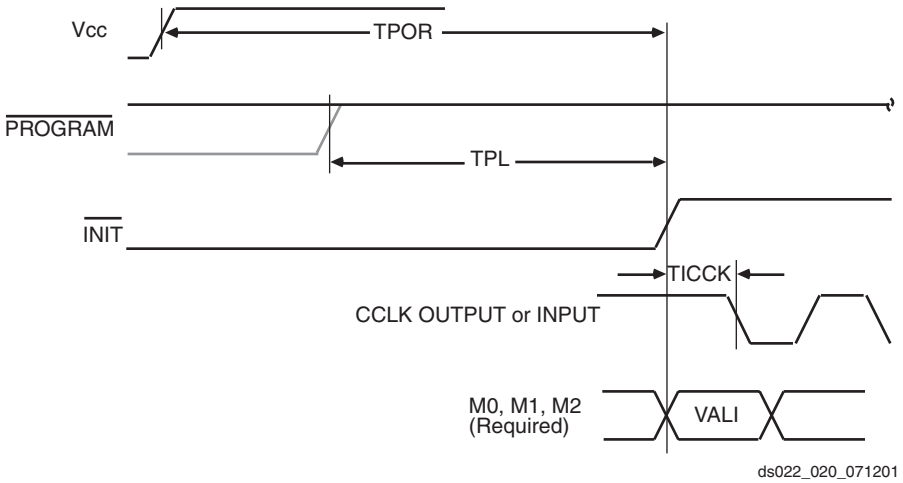

Figure 20: **Power-Up Timing Configuration Signals**

The corresponding timing characteristics are listed in Table 12.

Table 12: **Power-up Timing Characteristics**

Description	Symbol	Value	Units
Power-on Reset[1]	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Notes:
1. T_{POR} delay is the initialization time required after V_{CCINT} reaches the recommended operating voltage.

Delaying Configuration

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global 3-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits

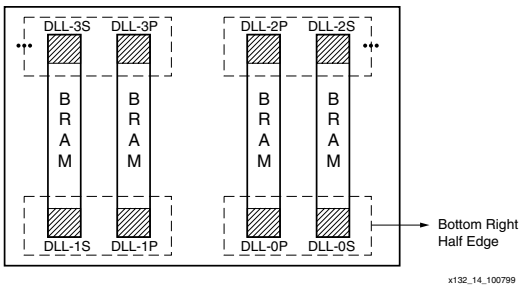

Figure 26: **Virtex Series DLLs**

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 µs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED stays High and remains High when the clock is restored.

When the clock is stopped, one to four more clocks are still observed as the delay line is flushed. When the clock is restarted, the output clocks are not observed for one to four clocks as the delay line is filled. The most common case is two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates one to four clocks to the output after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Useful Application Examples

The Virtex-E DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications. The Verilog and VHDL example files are available at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Standard Usage

The circuit shown in Figure 27 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

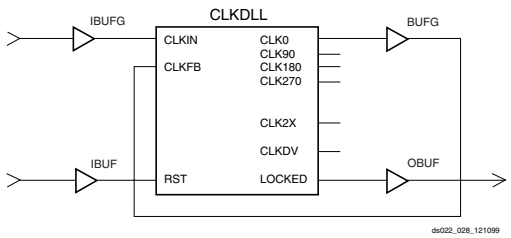

Figure 27: **Standard DLL Implementation**

Board Level De-Skew of Multiple Non-Virtex-E Devices

The circuit shown in Figure 28 can be used to de-skew a system clock between a Virtex-E chip and other non-Virtex-E chips on the same board. This application is commonly used when the Virtex-E device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

Conflict Resolution

The block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 33 shows a timing diagram for a single port of a block SelectRAM+ memory. The block SelectRAM+ AC switching characteristics are specified in the data sheet. The block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 34 shows a timing diagram for a true dual-port read/write block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location are invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory are correct, but the read port has invalid data. At the first rising edge of CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.

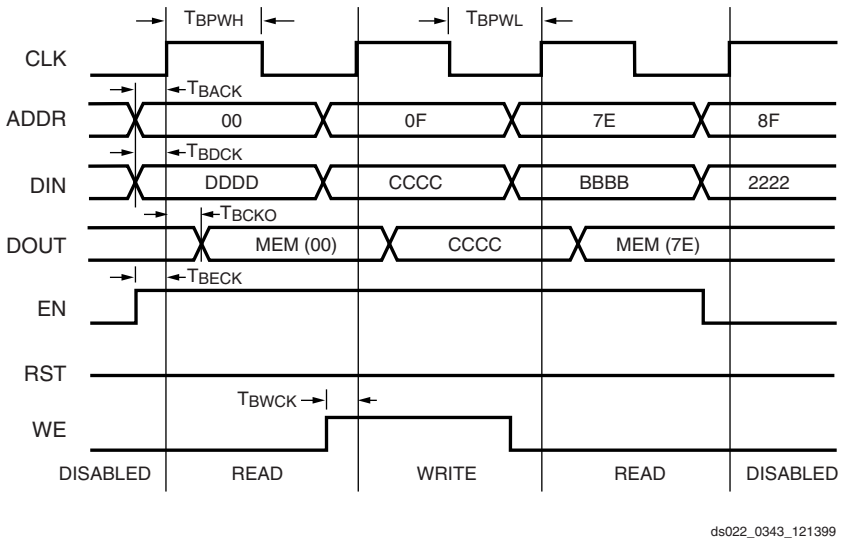

Figure 33: **Timing Diagram for Single Port Block SelectRAM+ Memory**

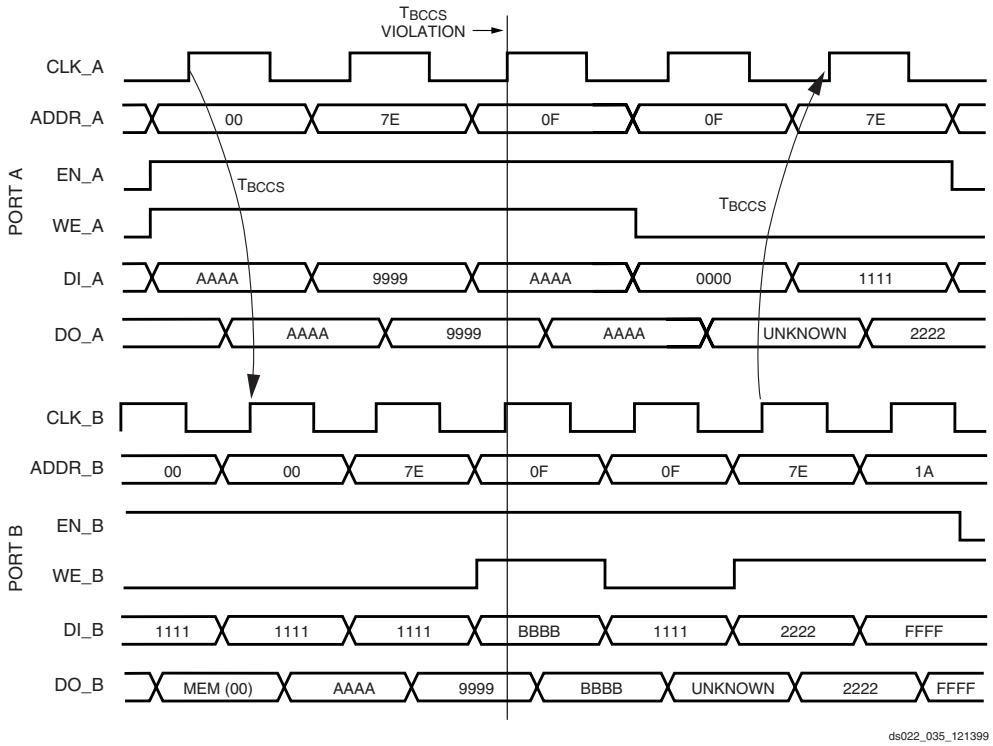

Figure 34: **Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory**

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x0F is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 40.

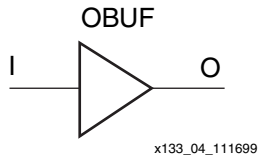

Figure 40: **Virtex-E Output Buffer (OBUF) Symbol**

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows.

```
OBUF_<slew_rate>_<drive_strength>
```

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank.

Table 20 summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 20: **Output Standards Compatibility Requirements**

Rule 1	Only outputs with standards that share compatible V_{CCO} can be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 41, typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows.

```
OBUFT_<slew_rate>_<drive_strength>
```

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

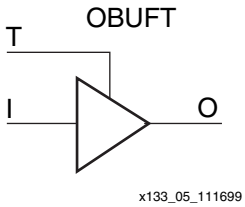

Figure 41: **3-State Output Buffer Symbol (OBUFT)**

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP
- OBUFT_LVCMOS18
- OBUFT_LVDS
- OBUFT_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

The SelectI/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak “keeper” circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak “keeper” circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak “keeper” typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 42.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows.

```
IOBUF_<slew_rate>_<drive_strength>
```

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

Input termination techniques include the following:

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

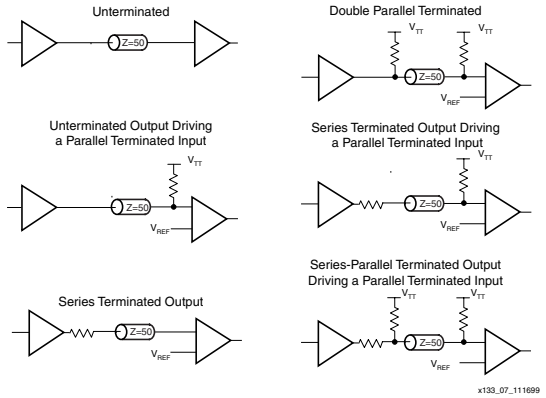

Figure 43: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 21: **Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package
	BGA, FGA
LVTTL Slow Slew Rate, 2 mA drive	68
LVTTL Slow Slew Rate, 4 mA drive	41
LVTTL Slow Slew Rate, 6 mA drive	29
LVTTL Slow Slew Rate, 8 mA drive	22
LVTTL Slow Slew Rate, 12 mA drive	17
LVTTL Slow Slew Rate, 16 mA drive	14
LVTTL Slow Slew Rate, 24 mA drive	9
LVTTL Fast Slew Rate, 2 mA drive	40
LVTTL Fast Slew Rate, 4 mA drive	24
LVTTL Fast Slew Rate, 6 mA drive	17
LVTTL Fast Slew Rate, 8 mA drive	13
LVTTL Fast Slew Rate, 12 mA drive	10
LVTTL Fast Slew Rate, 16 mA drive	8
LVTTL Fast Slew Rate, 24 mA drive	5
LVCMOS	10
PCI	8
GTL	4
GTL+	4
HSTL Class I	18
HSTL Class III	9
HSTL Class IV	5
SSTL2 Class I	15
SSTL2 Class II	10
SSTL3 Class I	11
SSTL3 Class II	7
CTT	14
AGP	9

Note: This analysis assumes a 35 pF load for each output.

Table 22: **Virtex-E Extended Memory Family Equivalent Power/Ground Pairs**

Pkg/Part	XCV405E	XCV812E
BG560		56
FG676	56	
FG900		

LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 34.

Table 34: **LVTTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	3.6
V_{IL}	–0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–24	-	-
I_{OL}at V_{OL} (mA)	24	-	-

Note: $V_{OL}$and V_{OH} for lower drive currents sample tested.

LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 35.

Table 35: **LVCMOS2 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	3.6
V_{IL}	–0.5	-	0.7
V_{OH}	1.9	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–12	-	-
I_{OL}at V_{OL} (mA)	12	-	-

LVCMOS18

LVCMOS18 does not require termination. Table 36 lists DC voltage specifications.

Table 36: **LVCMOS18 Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	1.70	1.80	1.90
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	0.65 x V_{CCO}	-	1.95
V_{IL}	– 0.5	-	0.2 x V_{CCO}
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 37.

Table 37: **AGP-2X Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}$(1)	1.17	1.32	1.48
V_{TT}	-	-	-
$V_{IH} = V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} = V_{REF} – 0.2$	-	1.12	1.28
$V_{OH} = 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} = 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL}at V_{OL} (mA)	Note 2	-	-

Notes:
1. N must be greater than or equal to 0.39 and less than or equal to 0.41.
2. Tested according to the relevant specification.

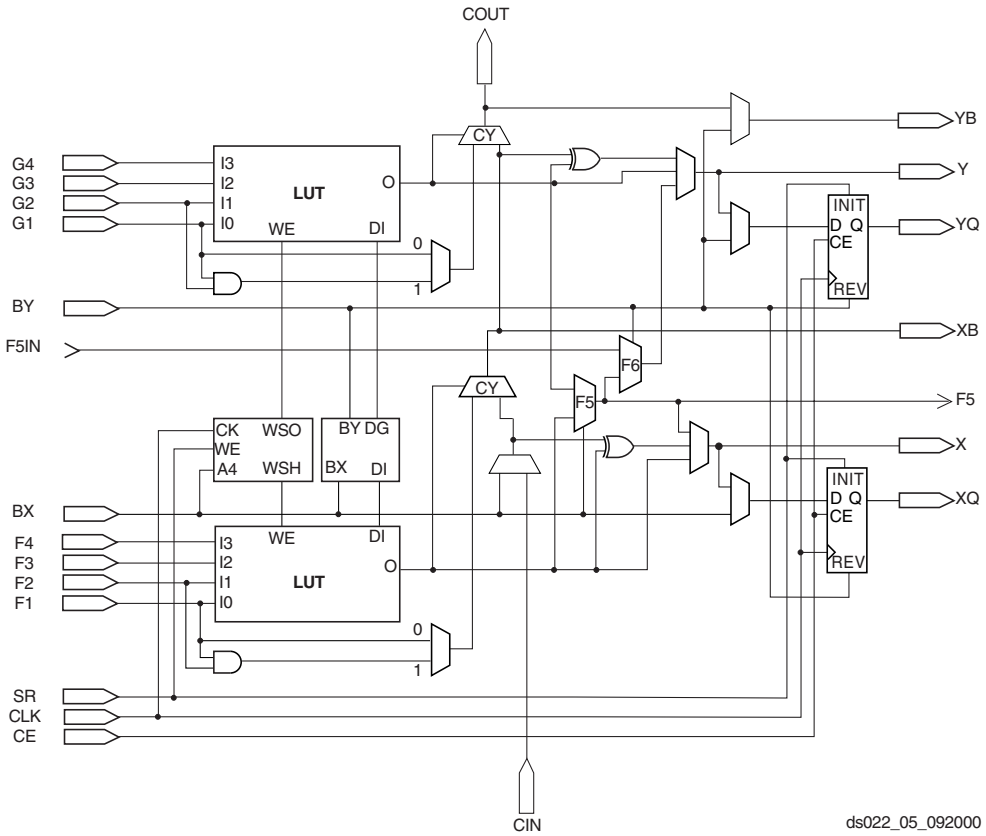

Figure 2: **Detailed View of Virtex-E Slice**

Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

Description[1]	Symbol	Device[3]	Speed Grade[2]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.							
No Delay	T_{PSDLL}/T_{PHDLL}	XCV405E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
Global Clock and IFF, with DLL		XCV812E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description[1]	Symbol	Device[3]	Speed Grade[2]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.							
Full Delay	T_{PSFD}/T_{PHFD}	XCV405E	2.3 / 0	2.3 / 0	2.3 / 0	2.3 / 0	ns
Global Clock and IFF, without DLL		XCV812E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

118	5	AK19	AM20	NA	-
119	5	AJ19	AL20	√	VREF_5
120	5	AN21	AL21	√	-
121	5	AJ20	AM22	1	-
122	5	AK21	AN23	√	VREF_5
123	5	AJ21	AM23	√	-
124	5	AK22	AM24	NA	-
125	5	AL23	AJ22	√	-
126	5	AK23	AL24	√	VREF_5
127	5	AN26	AJ23	2	-
128	5	AK24	AM26	1	VREF_5
129	5	AM27	AJ24	1	-
130	5	AL26	AK25	NA	-
131	5	AN29	AJ25	√	VREF_5
132	5	AK26	AM29	√	-
133	5	AM30	AJ26	2	-
134	5	AK27	AL29	√	VREF_5
135	5	AN31	AJ27	√	-
136	5	AM31	AK28	NA	-
137	6	AJ30	AH29	√	-
138	6	AH30	AK31	2	-
139	6	AJ31	AG29	NA	-
140	6	AG30	AK32	1	VREF_6
141	6	AF29	AH31	1	-
142	6	AF30	AH32	NA	-
143	6	AH33	AE29	√	VREF_6
144	6	AE30	AG33	2	-
145	6	AF32	AD29	NA	-
146	6	AD30	AE31	NA	VREF_6
147	6	AC29	AE32	NA	-
148	6	AC30	AD31	√	VREF_6
149	6	AC31	AB29	√	-
150	6	AB30	AC33	2	-
151	6	AA29	AB31	NA	-

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

152	6	AA31	AA30	1	VREF_6
153	6	Y29	AA32	1	-
154	6	Y30	AA33	NA	-
155	6	W29	Y32	√	VREF_6
156	6	W31	W30	2	-
157	6	V30	W33	NA	-
158	6	V31	V29	NA	VREF_6
159	6	U33	V32	NA	-
160	7	U32	U31	√	IRDY
161	7	T30	T32	NA	-
162	7	T31	T29	NA	VREF_7
163	7	R31	R33	NA	-
164	7	R29	R30	2	-
165	7	P31	P32	√	VREF_7
166	7	P29	P30	NA	-
167	7	N31	M32	1	-
168	7	L33	N30	1	VREF_7
169	7	L32	M31	NA	-
170	7	L31	M30	2	-
171	7	J33	M29	√	-
172	7	K31	L30	√	VREF_7
173	7	H33	L29	1	-
174	7	H32	J31	NA	VREF_7
175	7	H31	K29	NA	-
176	7	G32	J30	NA	-
177	7	G31	J29	√	VREF_7
178	7	E32	E33	NA	-
179	7	F31	H29	2	-
180	7	E31	D32	1	VREF_7
181	7	C33	G29	NA	-
182	7	D31	F30	NA	-

Notes:
1. AO in the XCV812E
2. AO in the XCV405E

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	GND	P12
NA	GND	P11
NA	GND	P10
NA	GND	N2
NA	GND	N17
NA	GND	N16
NA	GND	N15
NA	GND	N14
NA	GND	N13
NA	GND	N12
NA	GND	N11
NA	GND	N10
NA	GND	M17
NA	GND	M16
NA	GND	M15
NA	GND	M14
NA	GND	M13
NA	GND	M12
NA	GND	M11
NA	GND	M10
NA	GND	L17
NA	GND	L16
NA	GND	L15
NA	GND	L14
NA	GND	L13
NA	GND	L12
NA	GND	L11
NA	GND	L10
NA	GND	K17
NA	GND	K16
NA	GND	K15
NA	GND	K14
NA	GND	K13
NA	GND	K12
NA	GND	K11

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
NA	GND	K10
NA	GND	J25
NA	GND	J2
NA	GND	E5
NA	GND	E22
NA	GND	D4
NA	GND	D23
NA	GND	C3
NA	GND	C24
NA	GND	B9
NA	GND	B25
NA	GND	B2
NA	GND	B18
NA	GND	B14
NA	GND	AF26
NA	GND	AF1
NA	GND	AE9
NA	GND	AE25
NA	GND	AE2
NA	GND	AE18
NA	GND	AE13
NA	GND	AD3
NA	GND	AD24
NA	GND	AC4
NA	GND	AC23
NA	GND	AB5
NA	GND	AB22
NA	GND	A26
NA	GND	A1

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
118	5	AA12	AD12	√	-
119	5	AC12	AB12	√	VREF
120	5	AD11	Y12	√	-
121	5	AB11	AD10	NA	-
122	5	AC11	AE10	√	-
123	5	AC10	AA11	√	-
124	5	Y11	AD9	NA	-
125	5	AB10	AF9	√	-
126	5	AD8	AA10	√	VREF
127	5	AE8	Y10	√	-
128	5	AC9	AF8	NA	-
129	5	AF7	AB9	NA	-
130	5	AA9	AF6	√	-
131	5	AC8	AC7	√	VREF
132	5	AD6	Y9	√	-
133	5	AE5	AA8	√	-
134	5	AC6	AB8	√	VREF
135	5	AD5	AA7	√	-
136	5	AF4	AC5	NA	-
137	6	AC3	AA5	√	-
138	6	AB4	AC2	√	-
139	6	AA4	W6	NA	-
140	6	Y5	AB3	NA	VREF
141	6	V7	AB2	NA	-
142	6	Y4	AB1	√	-
143	6	W5	V5	√	VREF
144	6	V6	AA1	√	-
145	6	Y3	W4	NA	-
146	6	U7	Y1	NA	-
147	6	V4	W1	√	-
148	6	U6	W2	√	VREF
149	6	T5	V3	√	-
150	6	U4	U5	√	-
151	6	U3	T7	NA	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
152	6	T6	U2	NA	-
153	6	T4	U1	NA	-
154	6	T3	R7	NA	-
155	6	R6	R4	√	VREF
156	6	R5	R3	√	-
157	6	P7	P8	NA	-
158	6	P6	R1	NA	VREF
159	6	P4	P5	√	-
160	7	N8	N5	√	-
161	7	N3	N6	√	-
162	7	M2	N4	NA	VREF
163	7	M7	N7	NA	-
164	7	M3	M6	√	-
165	7	M5	M4	√	VREF
166	7	L7	L3	NA	-
167	7	K2	L6	NA	-
168	7	K1	L4	NA	-
169	7	L5	K3	NA	-
170	7	J3	K5	√	-
171	7	J4	K4	√	-
172	7	K6	H3	√	VREF
173	7	G3	K7	√	-
174	7	H1	J5	NA	-
175	7	J6	G2	NA	-
176	7	F1	J7	√	-
177	7	G4	H4	√	VREF
178	7	H5	F3	NA	-
179	7	H6	E2	NA	-
180	7	F4	G5	NA	VREF
181	7	G6	H7	NA	-
182	7	E4	E3	√	-

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
0	IO_L29N	D14
0	IO_L29P	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_LVDS_DLL_L34N	A15
1	GCk2	E15
1	IO	B18
1	IO	B21
1	IO	B28
1	IO	C23
1	IO	C26
1	IO	D20
1	IO	D23
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N	B16
1	IO_L35P	F16
1	IO_L36N	A16
1	IO_L36P	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N	A17
1	IO_L39P	E17
1	IO_L40N	F17
1	IO_L40P	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N	B19

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
1	IO_L43P	G18
1	IO_L44N	D19
1	IO_L44P	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N	H19
1	IO_L53P	B22
1	IO_L54N	E21
1	IO_L54P	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N	G21
1	IO_L57P	A23
1	IO_L58N	A24
1	IO_L58P	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N	E23
1	IO_L61P	C25
1	IO_L62N	D24

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
1	IO_L62P	A26
1	IO_L63N_YY	B26
1	IO_VREF_L63P_YY	K20
1	IO_L64N_YY	D25
1	IO_L64P_YY	J21
1	IO_L66N_Y	B27
1	IO_L66P_Y	G23
1	IO_L67N_Y	A27
1	IO_L67P_Y	F24
1	IO_WRITE_L69N_YY	K21
1	IO_CS_L69P_YY	C27
2	IO	D28
2	IO	F27
2	IO	H25
2	IO	J25
2	IO	J28
2	IO	K28
2	IO	K30
2	IO	M23
2	IO	N20
2	IO	N23
2	IO	R27
2	IO	R28
2	IO	R30
2	IO_DOUT_BUSY_L70P_YY	J22
2	IO_DIN_D0_L70N_YY	E27
2	IO_L72P_Y	G25
2	IO_L72N_Y	E25
2	IO_L73P	E28
2	IO_L73N	C30
2	IO_L75P	D30
2	IO_L75N	J23
2	IO_VREF_L76P_Y	L21

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
2	IO_L76N_Y	F28
2	IO_L77P_YY	G28
2	IO_L77N_YY	E30
2	IO_L78P	G27
2	IO_L78N	E29
2	IO_L79P	K23
2	IO_L79N	H26
2	IO_VREF_L80P_YY	F30
2	IO_L80N_YY	L22
2	IO_L81P_YY	H27
2	IO_L81N_YY	G29
2	IO_L82P_Y	G30
2	IO_L82N_Y	M21
2	IO_L83P	J24
2	IO_L83N	J26
2	IO_VREF_L84P	H30
2	IO_L84N	L23
2	IO_L86P	J29
2	IO_L86N	K24
2	IO_VREF	J30
2	IO_D1_L88P	M22
2	IO_D2_L88N	K29
2	IO_L90P_Y	N21
2	IO_L90N_Y	K25
2	IO_L91P	L24
2	IO_L91N	L27
2	IO_L93P	L26
2	IO_L93N	L28
2	IO_VREF_L94P_Y	L30
2	IO_L94N_Y	M27
2	IO_L95P_YY	M26
2	IO_L95N_YY	M29
2	IO_L96P	N29
2	IO_L96N	M30

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
25	0	B12	G13	-	-
26	0	K13	A12	√	-
27	0	B13	F13	√	VREF
28	0	E13	G14	-	-
29	0	B14	D14	-	-
30	0	J14	A14	√	-
31	0	J15	K14	√	VREF
34	1	E16	A15	-	GCLK LVDS 3/2
35	1	F16	B16	-	-
36	1	H16	A16	-	-
37	1	K15	C16	√	VREF
38	1	G16	K16	√	-
39	1	E17	A17	-	-
40	1	C17	F17	-	-
41	1	A18	E18	√	VREF
42	1	A19	D18	√	-
43	1	G18	B19	-	-
44	1	H18	D19	-	-
45	1	F19	F18	√	VREF
46	1	K17	B20	√	-
48	1	C20	G19	√	-
49	1	E20	K18	√	-
51	1	A21	F20	√	-
52	1	A22	C21	√	VREF
53	1	B22	H19	-	-
54	1	D22	E21	-	-
55	1	C22	F21	√	VREF
56	1	E22	H20	√	-
57	1	A23	G21	-	-
58	1	K19	A24	-	-
59	1	B24	C24	√	VREF
60	1	G22	H21	√	-
61	1	C25	E23	-	-
62	1	A26	D24	-	-
63	1	K20	B26	√	VREF
64	1	J21	D25	√	-
66	1	G23	B27	√	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
67	1	F24	A27	√	-
69	1	C27	K21	√	CS
70	2	J22	E27	√	DIN_D0
72	2	G25	E25	√	-
73	2	E28	C30	-	-
75	2	D30	J23	-	-
76	2	L21	F28	√	VREF
77	2	G28	E30	√	-
78	2	G27	E29	-	-
79	2	K23	H26	-	-
80	2	F30	L22	√	VREF
81	2	H27	G29	√	-
82	2	G30	M21	√	-
83	2	J24	J26	-	-
84	2	H30	L23	-	VREF
86	2	J29	K24	-	-
88	2	M22	K29	-	D2
90	2	N21	K25	√	-
91	2	L24	L27	-	-
93	2	L26	L28	-	-
94	2	L30	M27	√	VREF
95	2	M26	M29	√	-
96	2	N29	M30	-	-
97	2	N25	N27	-	-
98	2	N30	P21	√	D3
99	2	N26	P28	√	-
100	2	P29	N24	√	-
101	2	P22	R26	-	-
102	2	P25	R29	-	VREF
104	2	R25	T30	-	-
106	3	R24	U29	-	TRDY
107	3	R22	T27	-	-
108	3	R23	T28	-	-
109	3	T21	T25	-	VREF
110	3	U28	U30	-	-
111	3	T23	U27	√	-
112	3	U25	V27	√	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
113	3	U24	V29	√	VREF
114	3	W30	U22	-	-
115	3	U21	W29	-	-
116	3	V26	W27	√	-
117	3	W26	Y29	√	VREF
118	3	W25	Y30	-	-
120	3	AA30	W24	-	-
121	3	AA29	V20	√	-
123	3	Y26	AB30	√	D5
124	3	V21	AA28	√	VREF
125	3	Y25	AA27	-	-
126	3	W22	Y23	-	-
127	3	Y24	AB28	-	VREF
128	3	AC30	AA25	-	-
129	3	W21	AA24	√	-
130	3	AB26	AD30	√	-
131	3	Y22	AC27	√	VREF
132	3	AD28	AB25	-	-
133	3	AC26	AE30	-	-
134	3	AD27	AF30	√	-
135	3	AF29	AB24	√	VREF
136	3	AB23	AE28	-	-
138	3	AE26	AG29	-	-
139	3	AH30	AC24	√	-
141	3	AH29	AA22	√	INIT
142	4	AF27	AK28	√	-
144	4	AD23	AJ27	√	-
145	4	AB21	AF25	√	-
147	4	AA21	AG25	√	-
148	4	AJ26	AD22	√	VREF
149	4	AA20	AH25	-	-
150	4	AC21	AF24	-	-
151	4	AG24	AK26	√	-
152	4	AJ24	AF23	√	VREF
153	4	AE23	AB20	-	-
154	4	AC20	AG23	-	-
155	4	AF22	AE22	√	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
156	4	AJ22	AG22	√	VREF
158	4	AA19	AF21	-	-
160	4	AG21	AK23	-	-
162	4	AE20	AJ21	√	-
163	4	AG20	AF20	√	-
165	4	AJ20	AE19	√	-
166	4	AK22	AH20	√	VREF
167	4	AG19	AB17	-	-
168	4	AJ19	AD17	-	-
169	4	AA16	AA17	√	-
170	4	AK21	AB16	√	VREF
171	4	AG18	AK20	-	-
172	4	AK19	AD16	-	-
173	4	AE16	AE17	√	-
174	4	AG17	AJ17	√	VREF
176	4	AG16	AK17	-	-
177	5	AF16	AH16	-	GCLK LVDS 1/0
179	5	AB15	AF15	-	-
180	5	AA15	AF14	√	VREF
181	5	AH15	AK15	√	-
182	5	AB14	AF13	-	-
183	5	AH14	AJ14	-	-
184	5	AE14	AG13	√	VREF
185	5	AK13	AD13	√	-
186	5	AE13	AF12	-	-
187	5	AC13	AA13	-	-
188	5	AA12	AJ12	√	VREF
189	5	AB12	AE11	√	-
191	5	AG11	AF11	√	-
192	5	AH11	AJ11	√	-
194	5	AD12	AK11	√	-
195	5	AJ10	AC12	√	VREF
196	5	AK10	AD11	-	-
197	5	AJ9	AE9	-	-
198	5	AH10	AF9	√	VREF
199	5	AH9	AK9	√	-
200	5	AF8	AB11	-	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
201	5	AC11	AG8	-	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	-	-
205	5	AH6	AC10	-	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
209	5	AC9	AJ4	√	-
210	5	AG5	AK4	√	-
212	6	AC6	AF3	√	-
214	6	AE4	AB9	√	-
215	6	AH1	AE3	-	-
217	6	AA10	AG1	-	-
218	6	AD4	AA9	√	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	-	-
221	6	AA7	AA8	-	-
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	√	-
225	6	AB4	Y8	-	-
226	6	W9	AB3	-	VREF
228	6	V10	AB1	-	-
230	6	AA3	V11	-	-
232	6	AA6	W7	√	-
233	6	Y4	Y6	-	-
235	6	Y2	Y3	-	-
236	6	W5	Y5	√	VREF
237	6	W6	W4	√	-
238	6	W2	V6	-	-
239	6	V4	U9	-	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	√	-
243	6	U3	T7	-	-
244	6	V2	T5	-	VREF
246	6	U2	T4	-	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
247	7	R10	T1	-	IRDY
249	7	R4	R8	-	-
250	7	R3	R7	-	-
251	7	P6	P10	-	VREF
252	7	P2	P5	-	-
253	7	P4	P7	√	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF
256	7	N6	M6	-	-
257	7	N1	N5	-	-
258	7	M5	M4	√	-
259	7	M1	M2	√	VREF
260	7	L2	L4	-	-
262	7	M8	L1	-	-
263	7	M9	K2	√	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	-	-
268	7	J5	L8	-	-
269	7	H4	K6	-	VREF
270	7	K7	H1	-	-
271	7	J2	J7	√	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	-	-
275	7	E1	G3	-	-
276	7	E2	H6	√	-
277	7	K9	E4	√	VREF
278	7	F4	J8	-	-
280	7	C2	G6	-	-
281	7	F5	D2	-	-