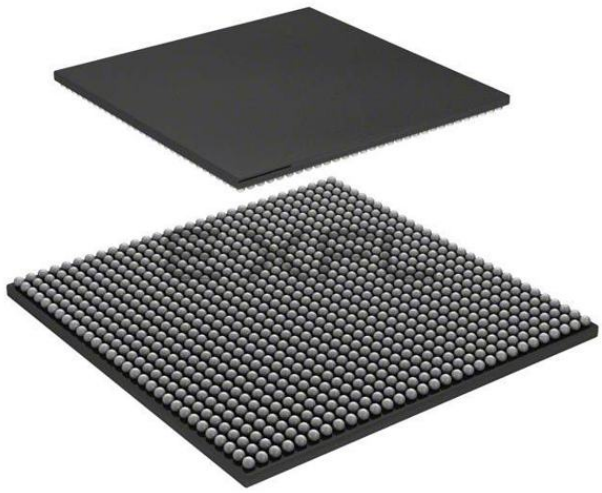
AMD Xilinx - XCV812E-7FG900C Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4704
Number of Logic Elements/Cells	21168
Total RAM Bits	1146880
Number of I/O	556
Number of Gates	254016
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	900-BBGA
Supplier Device Package	900-FBGA (31x31)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv812e-7fg900c

Table 2: **Performance for Common Circuit Functions**

Function	Bits	Virtex-E -7
Register-to-Register		
Adder	16 64	4.3 ns 6.3 ns
Pipelined Multiplier	8 x 8 16 x 16	4.4 ns 5.1 ns
Address Decoder	16 64	3.8 ns 5.5 ns
16:1 Multiplexer		4.6 ns
Parity Tree	9 18 36	3.5 ns 4.3 ns 5.9 ns
Chip-to-Chip		
HSTL Class IV		
LVTTL,16mA, fast slew		
LVDS		
LVPECL		

Virtex-E Extended Memory Device/Package Combinations and Maximum I/O

Table 3: **Virtex-EM Family Maximum User I/O by Device/Package (Excluding Dedicated Clock Pins)**

Package	XCV405E	XCV812E
BG560	404	404
FG676	404	
FG900		556

Virtex-E Extended Memory Ordering Information

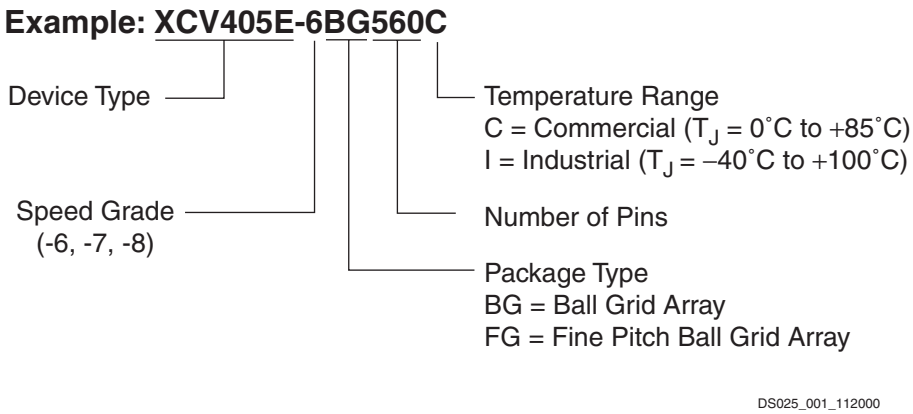

Figure 1: **Virtex Ordering Information**

IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

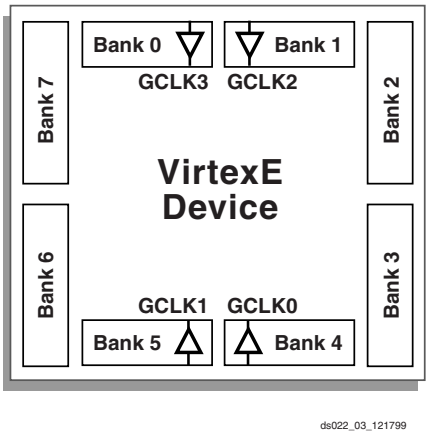

Figure 3: **Virtex-E I/O Banks**

Within a bank, output standards can be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 2. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 2: **Compatible Output Standards**

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8 V	LVCMOS18, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage can be used within a bank.

In Virtex-E, input buffers with LVTTL, LVCMOS2, LVCMOS18, PCI33_3, PCI66_3 standards are supplied by V_{CCO} rather than V_{CCINT}. For these standards, only input and output buffers that have the same V_{CCO} can be mixed together.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a super set of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins can be left unconnected externally, or they can be connected to the V_{CCO} voltage to permit migration to a larger device, if necessary.

Configurable Logic Block

The basic building block of the Virtex-E CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex-E CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

bined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Virtex-E LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals can be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, two per slice. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex-E CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Virtex-E CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing" on page 7. Each Virtex-E BUFT has an independent 3-state control pin and an independent input pin.

Block SelectRAM+ Memory

Virtex-E FPGAs incorporate large block SelectRAM memories. These complement the Distributed SelectRAM memories that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns, starting at the left (column 0) and right outside edges and inserted every four CLB columns (see notes for smaller devices). Each memory block is four CLBs high, and each memory column extends the full height of the chip, immediately adjacent (to the right, except for column 0) of the CLB column locations indicated in Table 3.

Table 3: **CLB/Block RAM Column Locations**

Virtex-E Device	0	4	8	12	16	20	24	28	32	36	40	44	48	52	56	60	64	68	72	76	80	84
XCV405E	√	√	√	√	√	√	√			√	√	√	√	√	√	√						
XCV812E	√	√	√	√	√	√	√	√	√	√			√	√	√	√	√	√	√	√	√	√

Table 4 shows the amount of block SelectRAM memory that is available in each Virtex-E device.

Table 4: **Virtex-E Block SelectRAM Amounts**

Virtex-E Device	# of Blocks	Block SelectRAM Bits
XCV405E	140	573,440
XCV812E	280	1,146,880

Each block SelectRAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported (True Dual Port) 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

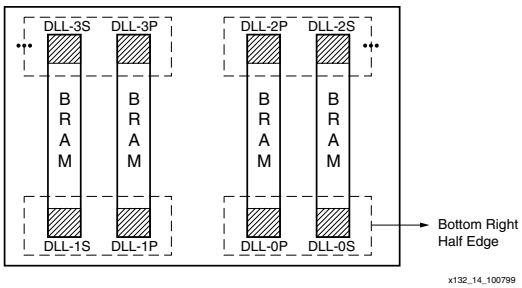

Figure 26: **Virtex Series DLLs**

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 µs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED stays High and remains High when the clock is restored.

When the clock is stopped, one to four more clocks are still observed as the delay line is flushed. When the clock is restarted, the output clocks are not observed for one to four clocks as the delay line is filled. The most common case is two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates one to four clocks to the output after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Useful Application Examples

The Virtex-E DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications. The Verilog and VHDL example files are available at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Standard Usage

The circuit shown in Figure 27 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

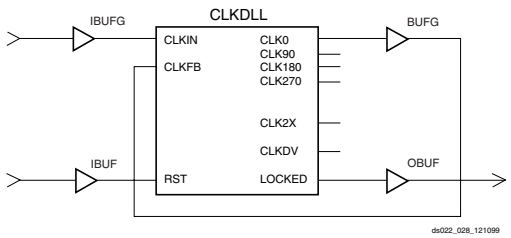

Figure 27: **Standard DLL Implementation**

Board Level De-Skew of Multiple Non-Virtex-E Devices

The circuit shown in Figure 28 can be used to de-skew a system clock between a Virtex-E chip and other non-Virtex-E chips on the same board. This application is commonly used when the Virtex-E device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

Conflict Resolution

The block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 33 shows a timing diagram for a single port of a block SelectRAM+ memory. The block SelectRAM+ AC switching characteristics are specified in the data sheet. The block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 34 shows a timing diagram for a true dual-port read/write block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 33.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location are invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory are correct, but the read port has invalid data. At the first rising edge of CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.

IOB Flip-Flop/Latch Property

The Virtex-E series I/O block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

```
map -pr b <filename>
```

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form.

```
LOC=A42
LOC=P37
```

Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

```
SLEW=SLOW
SLEW=FAST
```

Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

```
DRIVE=2
DRIVE=4
DRIVE=6
DRIVE=8
DRIVE=12 (Default)
DRIVE=16
DRIVE=24
```

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is “banked” within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, LVCMOS18, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following are output termination techniques:

- None
- Series
- Parallel (Shunt)
- Series and Parallel (Series-Shunt)

Input termination techniques include the following:

- None
- Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 43.

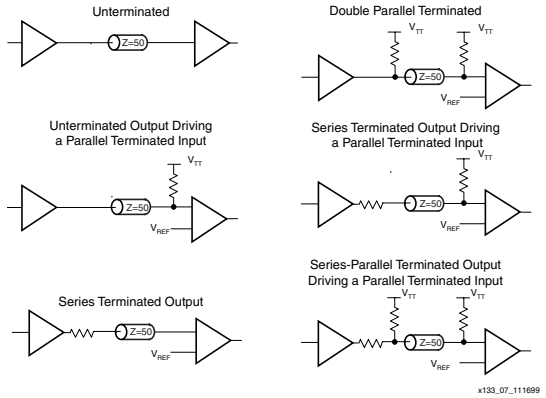

Figure 43: **Overview of Standard Input and Output Termination Methods**

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 21 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 22 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 21: **Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair**

Standard	Package
	BGA, FGA
LVTTL Slow Slew Rate, 2 mA drive	68
LVTTL Slow Slew Rate, 4 mA drive	41
LVTTL Slow Slew Rate, 6 mA drive	29
LVTTL Slow Slew Rate, 8 mA drive	22
LVTTL Slow Slew Rate, 12 mA drive	17
LVTTL Slow Slew Rate, 16 mA drive	14
LVTTL Slow Slew Rate, 24 mA drive	9
LVTTL Fast Slew Rate, 2 mA drive	40
LVTTL Fast Slew Rate, 4 mA drive	24
LVTTL Fast Slew Rate, 6 mA drive	17
LVTTL Fast Slew Rate, 8 mA drive	13
LVTTL Fast Slew Rate, 12 mA drive	10
LVTTL Fast Slew Rate, 16 mA drive	8
LVTTL Fast Slew Rate, 24 mA drive	5
LVCMOS	10
PCI	8
GTL	4
GTL+	4
HSTL Class I	18
HSTL Class III	9
HSTL Class IV	5
SSTL2 Class I	15
SSTL2 Class II	10
SSTL3 Class I	11
SSTL3 Class II	7
CTT	14
AGP	9

Note: This analysis assumes a 35 pF load for each output.

Table 22: **Virtex-E Extended Memory Family Equivalent Power/Ground Pairs**

Pkg/Part	XCV405E	XCV812E
BG560		56
FG676	56	
FG900		

Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 44. Table 23 lists DC voltage specifications.

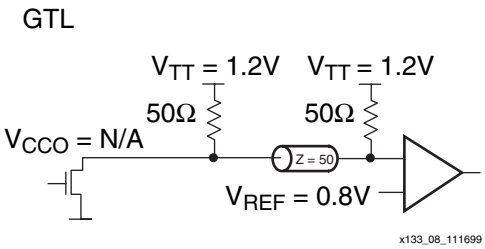

Figure 44: **Terminated GTL**

Table 23: **GTL Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$[1]	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH}(mA)	-	-	-
I_{OL}at V_{OL}(mA) at 0.4V	32	-	-
I_{OL}at V_{OL}(mA) at 0.2V	-	-	40

Note: N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 45. DC voltage specifications appear in Table 24.

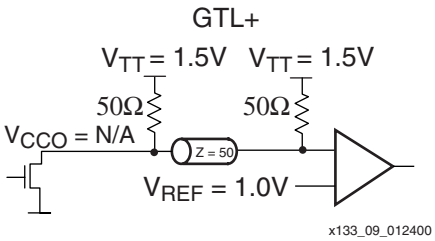

Figure 45: **Terminated GTL+**

Table 24: **GTL+ Voltage Specifications**

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$[1]	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} - 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL}at V_{OL} (mA) at 0.6V	36	-	-
I_{OL}at V_{OL} (mA) at 0.3V	-	-	48

Note: N must be greater than or equal to 0.653 and less than or equal to 0.68.

Creating LVDS Output 3-State Buffers

LVDS output 3-state buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both output 3-state buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one High and one Low). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

VHDL Instantiation

```
data0_p:   OBUFT_LVDS port map
(I=>data_int(0), T=>data_tri,
O=>data_p(0));

data0_inv: INV port map
(I=>data_int(0), O=>data_n_int(0));

data0_n:    OBUFT_LVDS port map
(I=>data_n_int(0), T=>data_tri,
O=>data_n(0));
```

Verilog Instantiation

```
OBUFT_LVDS data0_p   (.I(data_int[0]),
.T(data_tri), .O(data_p[0]));

INV        data0_inv (.I(data_int[0],
.O(data_n_int[0]);

OBUFT_LVDS data0_n   (.I(data_n_int[0]),
.T(data_tri), .O(data_n[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the UCF or NCF file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous 3-State Outputs

If the outputs are synchronous (registered in the IOB), then any IO_L#P|N pair can be used. If the outputs are asynchronous (no output register), then they must use one of the pairs that are part of the same IOB group at the end of a ROW or at the top/bottom of a COLUMN in the device. This applies for either the 3-state pin or the data out pin.

LVDS pairs that can be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as “asynchronous capable” for all devices in that package, and others are marked as available only for that device in the package. If the device size might be changed at some point in the product lifetime, then only the common pairs for all packages should be used.

Adding Output and 3-State Registers

All LVDS buffers can have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The input library macros are listed below. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output register. If this is not desirable, the library can be updated by the user for the desired functionality. The O and OB inputs to the macros are the external net connections.

Creating LVDS Bidirectional Buffer

LVDS bidirectional buffers can be placed in a wide number of IOB locations. The exact locations are dependent on the package used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side, where # is the pair number.

HDL Instantiation

Both bidirectional buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). If 3-state registers are used, they must be initialized to the same state. Failure to follow these rules leads to DRC errors in the software.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

			Speed Grade				
Description	**Symbol**	**Standard**	**Min**	**-8**	**-7**	**-6**	**Units**
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	+14.7	+14.7	+14.7	ns
	T_{OLVTTL_S4}	4 mA	2.5	+7.5	+7.5	+7.5	ns
	T_{OLVTTL_S6}	6 mA	1.8	+4.8	+4.8	+4.8	ns
	T_{OLVTTL_S8}	8 mA	1.2	+3.0	+3.0	+3.0	ns
	T_{OLVTTL_S12}	12 mA	1.0	+1.9	+1.9	+1.9	ns
	T_{OLVTTL_S16}	16 mA	0.9	+1.7	+1.7	+1.7	ns
	T_{OLVTTL_S24}	24 mA	0.8	+1.3	+1.3	+1.3	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA	1.9	+13.1	+13.1	+13.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	+5.3	+5.3	+5.3	ns
	T_{OLVTTL_F6}	6 mA	0.20	+3.1	+3.1	+3.1	ns
	T_{OLVTTL_F8}	8 mA	0.10	+1.0	+1.0	+1.0	ns
	T_{OLVTTL_F12}	12 mA	0.0	0.0	0.0	0.0	ns
	T_{OLVTTL_F16}	16 mA	–0.10	–0.05	–0.05	–0.05	ns
	T_{OLVTTL_F24}	24 mA	–0.10	–0.20	–0.20	–0.20	ns
	$T_{OLVCMOS\_2}$	LVCMOS2	0.10	+0.09	+0.09	+0.09	ns
	$T_{OLVCMOS\_18}$	LVCMOS18	0.10	+0.7	+0.7	+0.7	ns
	T_{OLVDS}	LVDS	–0.39	–1.2	–1.2	–1.2	ns
	$T_{OLVPECL}$	LVPECL	–0.20	–0.41	–0.41	–0.41	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	+2.3	+2.3	+2.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	–0.41	–0.41	–0.41	ns
	T_{OGTL}	GTL	0.6	+0.49	+0.49	+0.49	ns
	T_{OGTLP}	GTL+	0.7	+0.8	+0.8	+0.8	ns
	T_{OHSTL_I}	HSTL I	0.10	–0.51	–0.51	–0.51	ns
	T_{OHSTL_IIII}	HSTL III	–0.10	–0.91	–0.91	–0.91	ns
	T_{OHSTL_IV}	HSTL IV	–0.20	–1.01	–1.01	–1.01	ns
	T_{OSSTL2_I}	SSTL2 I	–0.10	–0.51	–0.51	–0.51	ns
	T_{OSSTL2_II}	SSTL2 II	–0.20	–0.91	–0.91	–0.91	ns
	T_{OSSTL3_I}	SSTL3 I	–0.20	–0.51	–0.51	–0.51	ns
	T_{OSSTL3_II}	SSTL3 II	–0.30	–1.01	–1.01	–1.01	ns
	T_{OCTT}	CTT	0.0	–0.61	–0.61	–0.61	ns
	T_{OAGP}	AGP	–0.1	–0.91	–0.91	–0.91	ns

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description[1]	Symbol	Speed Grade				Units
		Min	-8	-7	-6	
Combinatorial Delays						
F operand inputs to X via XOR	T_{OPX}	0.32	0.68	0.8	0.8	ns, max
F operand input to XB output	T_{OPXB}	0.35	0.65	0.8	0.9	ns, max
F operand input to Y via XOR	T_{OPY}	0.59	1.07	1.4	1.5	ns, max
F operand input to YB output	T_{OPYB}	0.48	0.89	1.1	1.3	ns, max
F operand input to COUT output	T_{OPCYF}	0.37	0.71	0.9	1.0	ns, max
G operand inputs to Y via XOR	T_{OPGY}	0.34	0.72	0.8	0.9	ns, max
G operand input to YB output	T_{OPGYB}	0.47	0.78	1.2	1.3	ns, max
G operand input to COUT output	T_{OPCYG}	0.36	0.60	0.9	1.0	ns, max
BX initialization input to COUT	T_{BXCY}	0.19	0.36	0.51	0.57	ns, max
CIN input to X output via XOR	T_{CINX}	0.27	0.50	0.6	0.7	ns, max
CIN input to XB	T_{CINXB}	0.02	0.04	0.07	0.08	ns, max
CIN input to Y via XOR	T_{CINY}	0.26	0.45	0.7	0.7	ns, max
CIN input to YB	T_{CINYB}	0.16	0.28	0.38	0.43	ns, max
CIN input to COUT output	T_{BYP}	0.05	0.10	0.14	0.15	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.10	0.30	0.35	0.39	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.28	0.56	0.7	0.8	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.17	0.38	0.46	0.51	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.20	0.46	0.55	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.09	0.28	0.30	0.34	ns, max
Setup and Hold Times before/after Clock CLK						
CIN input to FFX	T_{CCKX}/T_{CKCX}	0.47 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}	0.49 / 0	0.92 / 0	1.2 / 0	1.3 / 0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Virtex-E Pin-to-Pin Output Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

Description[1]	Symbol	Device[3]	Speed Grade[2]				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.	$T_{ICKOFDLL}$	XCV405E	1.0	3.1	3.1	3.1	ns
		XCV812E	1.0	3.1	3.1	3.1	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 2 and Table 3.
3. DLL output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

Description[1]	Symbol	Device	Speed Grade[2]				Units
			Min	-8	-7	-6	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 8.	T_{ICKOF}	XCV405E	1.6	4.5	4.7	4.9	ns
		XCV812E	1.8	4.8	5.0	5.2	ns

Notes:
1. Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
2. Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 2 and Table 3.

Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

Description[1]	Symbol	Device[3]	Speed Grade[2]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.							
No Delay	T_{PSDLL}/T_{PHDLL}	XCV405E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
Global Clock and IFF, with DLL		XCV812E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description[1]	Symbol	Device[3]	Speed Grade[2]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.							
Full Delay	T_{PSFD}/T_{PHFD}	XCV405E	2.3 / 0	2.3 / 0	2.3 / 0	2.3 / 0	ns
Global Clock and IFF, without DLL		XCV812E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
2	IO_L61N_Y	N3
2	IO_L62P_Y	N2
2	IO_L62N_Y	P5
2	IO_VREF_L63P_YY	P4
2	IO_D3_L63N_YY	P3
2	IO_L64P_Y	P2
2	IO_L64N_Y	R5
2	IO_L65P_Y	R4
2	IO_L65N_Y	R3
2	IO_VREF_L66P_Y	R1
2	IO_L66N_Y	T4
2	IO_L67P_Y	T5
2	IO_L67N_Y	T3
2	IO_L68P_YY	T2
2	IO_L68N_YY	U3
3	IO	U4
3	IO	AE3
3	IO	AF3
3	IO	AH3
3	IO	AK3
3	IO_L69P_Y	U1
3	IO_L69N_Y	U2
3	IO_L70P_Y	V2
3	IO_VREF_L70N_Y	V4
3	IO_L71P_Y	V5
3	IO_L71N_Y	V3
3	IO_L72P	W1
3	IO_L72N	W3
3	IO_D4_L73P_YY	W4
3	IO_VREF_L73N_YY	W5
3	IO_L74P_Y	Y3
3	IO_L74N_Y	Y4
3	IO_L75P	AA1
3	IO_L75N	Y5
3	IO_L76P_Y	AA3
3	IO_VREF_L76N_Y	AA4[1]

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
3	IO_L77P	AB3
3	IO_L77N	AA5
3	IO_L78P	AC1
3	IO_L78N	AB4
3	IO_L79P_YY	AC3
3	IO_D5_L79N_YY	AB5
3	IO_D6_L80P_YY	AC4
3	IO_VREF_L80N_YY	AD3
3	IO_L81P_Y	AE1
3	IO_L81N_Y	AC5
3	IO_L82P_YY	AD4
3	IO_VREF_L82N_YY	AF1[1]
3	IO_L83P_Y	AF2
3	IO_L83N_Y	AD5
3	IO_L84P_Y	AG2
3	IO_L84N_Y	AE4
3	IO_L85P_YY	AH1
3	IO_VREF_L85N_YY	AE5
3	IO_L86P_Y	AF4
3	IO_L86N_Y	AJ1
3	IO_L87P_Y	AJ2
3	IO_L87N_Y	AF5
3	IO_L88P_Y	AG4
3	IO_VREF_L88N_Y	AK2
3	IO_L89P_Y	AJ3
3	IO_L89N_Y	AG5
3	IO_L90P_Y	AL1
3	IO_L90N_Y	AH4
3	IO_D7_L91P_YY	AJ4
3	IO_INIT_L91N_YY	AH5
4	GCK0	AL17
4	IO	AJ8
4	IO	AJ11
4	IO	AK6
4	IO	AK9
4	IO_L92P_YY	AL4

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
4	IO_L92N_YY	AJ6
4	IO_L93P	AK5
4	IO_L93N	AN3
4	IO_L94P_YY	AL5
4	IO_L94N_YY	AJ7
4	IO_VREF_L95P_YY	AM4
4	IO_L95N_YY	AM5
4	IO_L96P_Y	AK7
4	IO_L96N_Y	AL6
4	IO_L97P_YY	AM6
4	IO_L97N_YY	AN6
4	IO_VREF_L98P_YY	AL7
4	IO_L98N_YY	AJ9
4	IO_L99P	AN7
4	IO_L99N	AL8
4	IO_L100P_YY	AM8
4	IO_L100N_YY	AJ10
4	IO_VREF_L101P_YY	AL9[1]
4	IO_L101N_YY	AM9
4	IO_L102P_Y	AK10
4	IO_L102N_Y	AN9
4	IO_VREF_L103P_YY	AL10
4	IO_L103N_YY	AM10
4	IO_L104P_YY	AL11
4	IO_L104N_YY	AJ12
4	IO_L105P	AN11
4	IO_L105N	AK12
4	IO_L106P_YY	AL12
4	IO_L106N_YY	AM12
4	IO_VREF_L107P_YY	AK13[1]
4	IO_L107N_YY	AL13
4	IO_L108P_Y	AM13
4	IO_L108N_Y	AN13
4	IO_L109P_YY	AJ14
4	IO_L109N_YY	AK14
4	IO_VREF_L110P_YY	AM14
4	IO_L110N_YY	AN15
4	IO_L111P	AJ15
4	IO_L111N	AK15
4	IO_L112P_YY	AL15
4	IO_L112N_YY	AM16
4	IO_VREF_L113P_YY	AL16
4	IO_L113N_YY	AJ16
4	IO_L114P_Y	AK16
4	IO_L114N_Y	AN17
4	IO_LVDS_DLL_L115P	AM17
5	GCK1	AJ17
5	IO	AL18
5	IO	AL25
5	IO	AL28
5	IO	AL30
5	IO	AN28
5	IO_LVDS_DLL_L115N	AM18
5	IO_L116P_YY	AK18
5	IO_VREF_L116N_YY	AJ18
5	IO_L117P_YY	AN19
5	IO_L117N_YY	AL19
5	IO_L118P	AK19
5	IO_L118N	AM20
5	IO_L119P_YY	AJ19
5	IO_VREF_L119N_YY	AL20
5	IO_L120P_YY	AN21
5	IO_L120N_YY	AL21
5	IO_L121P_Y	AJ20
5	IO_L121N_Y	AM22
5	IO_L122P_YY	AK21
5	IO_VREF_L122N_YY	AN23[1]
5	IO_L123P_YY	AJ21
5	IO_L123N_YY	AM23
5	IO_L124P	AK22
5	IO_L124N	AM24
5	IO_L125P_YY	AL23
5	IO_L125N_YY	AJ22

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
NA	VCCINT	B18
NA	VCCINT	B28
NA	VCCINT	C22
NA	VCCINT	C24
NA	VCCINT	E9
NA	VCCINT	E12
NA	VCCINT	F2
NA	VCCINT	H30
NA	VCCINT	J1
NA	VCCINT	K32
NA	VCCINT	M3
NA	VCCINT	N1
NA	VCCINT	N29
NA	VCCINT	N33
NA	VCCINT	U5
NA	VCCINT	U30
NA	VCCINT	Y2
NA	VCCINT	Y31
NA	VCCINT	AB2
NA	VCCINT	AB32
NA	VCCINT	AD2
NA	VCCINT	AD32
NA	VCCINT	AG3
NA	VCCINT	AG31
NA	VCCINT	AJ13
NA	VCCINT	AK8
NA	VCCINT	AK11
NA	VCCINT	AK17
NA	VCCINT	AK20
NA	VCCINT	AL14
NA	VCCINT	AL22
NA	VCCINT	AL27
NA	VCCINT	AN25
0	VCCO	A22
0	VCCO	A26
0	VCCO	A30

Table 1: **BG560 BGA — XCV405E and XCV812E**

Bank	Pin Description	Pin#
0	VCCO	B19
0	VCCO	B32
1	VCCO	A10
1	VCCO	A16
1	VCCO	B13
1	VCCO	C3
1	VCCO	E5
2	VCCO	B2
2	VCCO	D1
2	VCCO	H1
2	VCCO	M1
2	VCCO	R2
3	VCCO	V1
3	VCCO	AA2
3	VCCO	AD1
3	VCCO	AK1
3	VCCO	AL2
4	VCCO	AN4
4	VCCO	AN8
4	VCCO	AN12
4	VCCO	AM2
4	VCCO	AM15
5	VCCO	AL31
5	VCCO	AM21
5	VCCO	AN18
5	VCCO	AN24
5	VCCO	AN30
6	VCCO	W32
6	VCCO	AB33
6	VCCO	AF33
6	VCCO	AK33
6	VCCO	AM32
7	VCCO	C32
7	VCCO	D33
7	VCCO	K33
7	VCCO	N32
7	VCCO	T33

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_L35P_Y	B19
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D26
2	IO	E26
2	IO	F26
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25
2	IO_L54P_Y	G26
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
50	2	F23	G23	√	-
51	2	H23	J20	√	VREF
52	2	G24	H22	√	-
53	2	J21	G25	2	-
54	2	G26	J22	1	-
55	2	H24	J23	√	-
56	2	J24	K20	√	VREF
57	2	K22	K21	√	D2
58	2	H25	K23	√	-
59	2	L20	J26	2	-
60	2	K25	L22	1	-
61	2	L21	L23	1	-
62	2	M20	L24	1	-
63	2	M23	M22	√	D3
64	2	L26	M21	√	-
65	2	N19	M24	2	-
66	2	M26	N20	1	VREF
67	2	N24	N21	√	-
68	2	N23	N22	√	-
69	3	P21	P23	√	-
70	3	P22	R25	1	VREF
71	3	P19	P20	2	-
72	3	R21	R22	√	-
73	3	R24	R23	√	VREF
74	3	T24	R20	1	-
75	3	T22	U24	1	-
76	3	T23	U25	1	-
77	3	T21	U20	2	-
78	3	U22	V26	√	-
79	3	T20	U23	√	D5
80	3	V24	U21	√	VREF
81	3	V23	W24	√	-
82	3	V22	W26	NA	-
83	3	Y25	V21	NA	-

Table 4: **FG676 Fine-Pitch BGA Differential Pin Pair Summary — XCV405E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
84	3	V20	AA26	√	-
85	3	Y24	W23	√	VREF
86	3	AA24	Y23	NA	-
87	3	AB26	W21	NA	-
88	3	Y22	W22	NA	VREF
89	3	AA23	AB24	NA	-
90	3	W20	AC24	√	-
91	3	AB23	Y21	√	INIT
92	4	AC22	AD26	√	-
93	4	AD23	AA20	NA1	-
94	4	Y19	AC21	√	-
95	4	AD22	AB20	√	VREF
96	4	AE22	Y18	NA	-
97	4	AF22	AA19	NA	-
98	4	AD21	AB19	√	VREF
99	4	AC20	AA18	√	-
100	4	AC19	AD20	NA	-
101	4	AF20	AB18	NA	-
102	4	AD19	Y17	NA	-
103	4	AE19	AD18	NA	VREF
104	4	AF19	AA17	√	-
105	4	AC17	AB17	NA	-
106	4	Y16	AE17	√	-
107	4	AF17	AA16	√	-
108	4	AD17	AB16	NA	-
109	4	AC16	AD16	√	-
110	4	AC15	Y15	√	VREF
111	4	AD15	AA15	√	-
112	4	W14	AB15	NA	-
113	4	AF15	Y14	NA	VREF
114	4	AD14	AB14	NA	-
115	5	AC14	AF13	NA	IO_LVDS_DLL
116	5	AA13	AF12	NA	VREF
117	5	AC13	W13	NA	-

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
2	IO_L97P	N25
2	IO_L97N	N27
2	IO_VREF_L98P_YY	N30
2	IO_D3_L98N_YY	P21
2	IO_L99P_YY	N26
2	IO_L99N_YY	P28
2	IO_L100P_Y	P29
2	IO_L100N_Y	N24
2	IO_L101P	P22
2	IO_L101N	R26
2	IO_VREF_2_L102P	P25
2	IO_L102N	R29
2	IO_L104P	R25
2	IO_L104N	T30
2	IO_L106P	R24
3	IO	T24
3	IO	V24
3	IO	Y21
3	IO	Y27
3	IO	AB27
3	IO	AF28
3	IO	AG30
3	IO_L106N	U29
3	IO_L107P	R22
3	IO_L107N	T27
3	IO_L108P	R23
3	IO_L108N	T28
3	IO_L109P	T21
3	IO_VREF_L109N	T25
3	IO_L110P	U28
3	IO_L110N	U30
3	IO_L111P_Y	T23
3	IO_L111N_Y	U27

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
3	IO_L112P_YY	U25
3	IO_L112N_YY	V27
3	IO_D4_L113P_YY	U24
3	IO_VREF_L113N_YY	V29
3	IO_L114P	W30
3	IO_L114N	U22
3	IO_L115P	U21
3	IO_L115N	W29
3	IO_L116P_YY	V26
3	IO_L116N_YY	W27
3	IO_L117P_Y	W26
3	IO_VREF_L117N_Y	Y29
3	IO_L118P	W25
3	IO_L118N	Y30
3	IO_L120P	AA30
3	IO_L120N	W24
3	IO_L121P_Y	AA29
3	IO_L121N_Y	V20
3	IO_L123P_YY	Y26
3	IO_D5_L123N_YY	AB30
3	IO_D6_L124P_YY	V21
3	IO_VREF_L124N_YY	AA28
3	IO_L125P	Y25
3	IO_L125N	AA27
3	IO_L126P	W22
3	IO_L126N	Y23
3	IO_L127P	Y24
3	IO_VREF_L127N	AB28
3	IO_L128P	AC30
3	IO_L128N	AA25
3	IO_L129P_Y	W21
3	IO_L129N_Y	AA24
3	IO_L130P_YY	AB26
3	IO_L130N_YY	AD30

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
201	5	AC11	AG8	-	-
202	5	AK8	AF7	√	VREF
203	5	AG7	AK7	√	-
204	5	AJ7	AD10	-	-
205	5	AH6	AC10	-	-
206	5	AD9	AG6	√	VREF
207	5	AB10	AJ5	√	-
209	5	AC9	AJ4	√	-
210	5	AG5	AK4	√	-
212	6	AC6	AF3	√	-
214	6	AE4	AB9	√	-
215	6	AH1	AE3	-	-
217	6	AA10	AG1	-	-
218	6	AD4	AA9	√	VREF
219	6	AD2	AD5	√	-
220	6	AF2	AD3	-	-
221	6	AA7	AA8	-	-
222	6	Y9	AF1	√	VREF
223	6	AC4	AB6	√	-
224	6	W8	AE1	√	-
225	6	AB4	Y8	-	-
226	6	W9	AB3	-	VREF
228	6	V10	AB1	-	-
230	6	AA3	V11	-	-
232	6	AA6	W7	√	-
233	6	Y4	Y6	-	-
235	6	Y2	Y3	-	-
236	6	W5	Y5	√	VREF
237	6	W6	W4	√	-
238	6	W2	V6	-	-
239	6	V4	U9	-	-
240	6	T8	AB2	√	VREF
241	6	W1	U5	√	-
242	6	T9	Y1	√	-
243	6	U3	T7	-	-
244	6	V2	T5	-	VREF
246	6	U2	T4	-	-

Table 6: **FG900 Differential Pin Pair Summary — XCV812E**

Pair	Bank	P Pin	N Pin	AO	Other Functions
247	7	R10	T1	-	IRDY
249	7	R4	R8	-	-
250	7	R3	R7	-	-
251	7	P6	P10	-	VREF
252	7	P2	P5	-	-
253	7	P4	P7	√	-
254	7	R2	N4	√	-
255	7	P1	N7	√	VREF
256	7	N6	M6	-	-
257	7	N1	N5	-	-
258	7	M5	M4	√	-
259	7	M1	M2	√	VREF
260	7	L2	L4	-	-
262	7	M8	L1	-	-
263	7	M9	K2	√	-
265	7	K1	K5	√	-
266	7	K3	L6	√	VREF
267	7	K4	L7	-	-
268	7	J5	L8	-	-
269	7	H4	K6	-	VREF
270	7	K7	H1	-	-
271	7	J2	J7	√	-
272	7	G2	H5	√	-
273	7	G5	L9	√	VREF
274	7	K8	F3	-	-
275	7	E1	G3	-	-
276	7	E2	H6	√	-
277	7	K9	E4	√	VREF
278	7	F4	J8	-	-
280	7	C2	G6	-	-
281	7	F5	D2	-	-