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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Obsolete
Number of LABs/CLBs	4704
Number of Logic Elements/Cells	21168
Total RAM Bits	1146880
Number of I/O	404
Number of Gates	254016
Voltage - Supply	1.71V ~ 1.89V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	560-LBGA Exposed Pad, Metal
Supplier Device Package	560-MBGA (42.5x42.5)
Purchase URL	https://www.e-xfl.com/product-detail/xilinx/xcv812e-8bg560c

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/23/00	1.0	Initial Xilinx release.
08/01/00	1.1	Accumulated edits and fixes. Upgrade to Preliminary. Preview -8 numbers added. Reformatted to adhere to corporate documentation style guidelines. Minor changes in BG560 pin-out table.
09/19/00	1.2	• In Table 3 (Module 4), **FG676 Fine-Pitch BGA — XCV405E**, the following pins are no longer labeled as VREF: B7, G16, G26, W26, AF20, AF8, Y1, H1. • Min values added to **Virtex-E Electrical Characteristics** tables.
11/20/00	1.3	• Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3). • Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2). • Added to note 2 of **Absolute Maximum Ratings** (Module 3). • Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3). • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters** (Module 3).
04/02/01	1.4	• In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF. • Updated values in **Virtex-E Switching Characteristics** tables. • Converted data sheet to modularized format. See **Virtex-E Extended Memory Data Sheet**, below.
07/17/02	1.5	• Data sheet designation upgraded from Preliminary to Production.

Virtex-E Extended Memory Data Sheet

The Virtex-E Extended Memory Data Sheet contains the following modules:

- DS025-1, Virtex-E 1.8V Extended Memory FPGAs: **Introduction and Ordering Information (Module 1)**
- DS025-2, Virtex-E 1.8V Extended Memory FPGAs: **Functional Description (Module 2)**
- DS025-3, Virtex-E 1.8V Extended Memory FPGAs: **DC and Switching Characteristics (Module 3)**
- DS025-4, Virtex-E 1.8V Extended Memory FPGAs: **Pinout Tables (Module 4)**

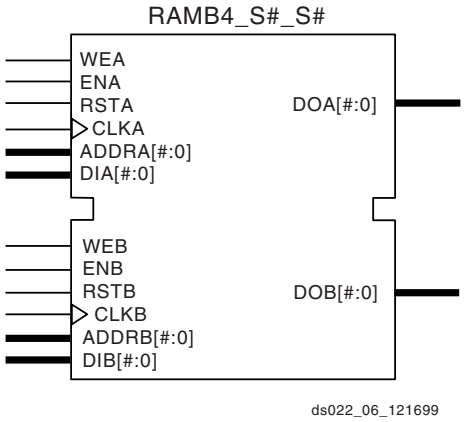


Figure 6: **Dual-Port Block SelectRAM**

Table 5 shows the depth and width aspect ratios for the block SelectRAM. The Virtex-E block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other block SelectRAM modules. Refer to XAPP130 for block SelectRAM timing waveforms.

Table 5: Block SelectRAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex-E routing architecture and its place-and-route software were defined in a joint optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock, shown in Figure 7, provides local routing resources with the following types of connections:

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM

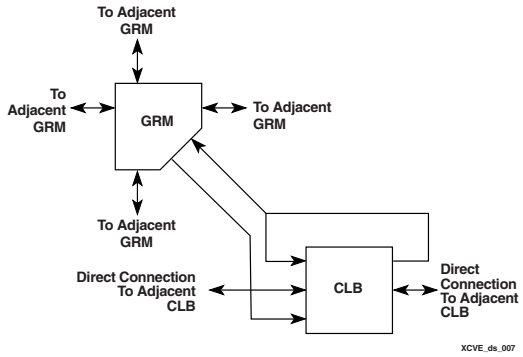


Figure 7: **Virtex-E Local Routing**

General Purpose Routing

Most Virtex-E signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the CLB rows and columns. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 72 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines are driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Virtex-E devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

either asserted or de-asserted. Otherwise an abort is initiated, as described below.

2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while $\overline{CS}$ is Low and $\overline{WRITE}$ is High. Similarly, while $\overline{WRITE}$ is High, no more that one $\overline{CS}$ should be asserted.
3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance instead occurs on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert $\overline{CS}$ and $\overline{WRITE}$.

Table 11: **SelectMAP Write Timing Characteristics**

	Description		Symbol	Values	Units
CCLK	D_{0-7} Setup/Hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0 / 1.7	ns, min
	$\overline{CS}$ Setup/Hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0 / 1.7	ns, min
	$\overline{WRITE}$ Setup/Hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0 / 1.7	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum Frequency		F_{CC}	66	MHz, max
	Maximum Frequency with no handshake		F_{CCNH}	50	MHz, max

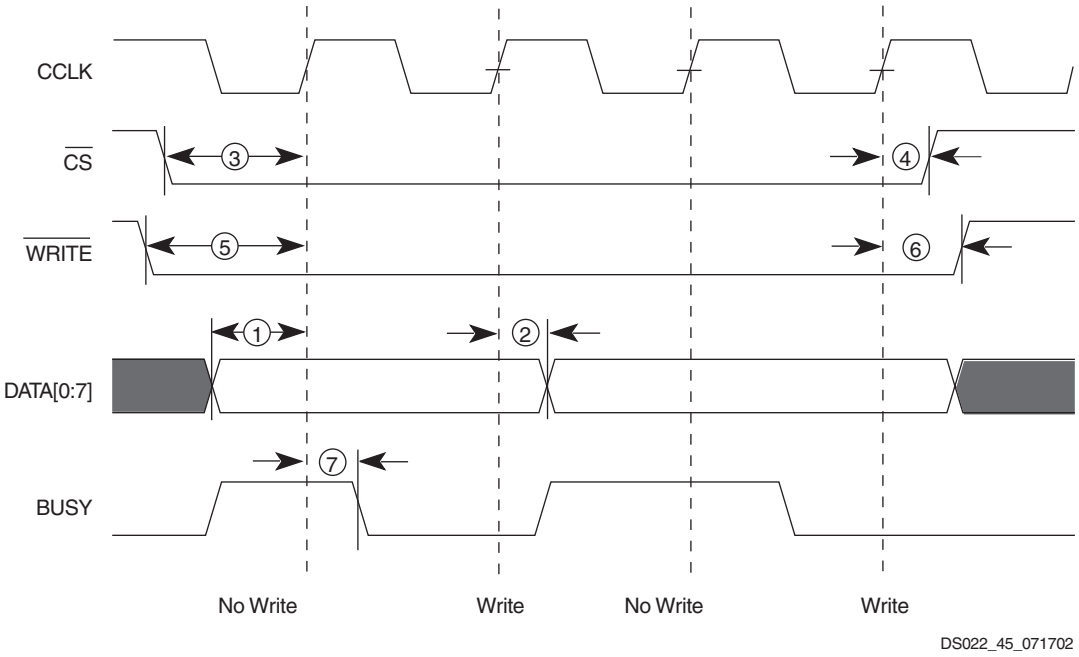


Figure 17: **Write Operations**

A flowchart for the write operation appears in Figure 18. Note that if CCLK is slower than f_{CCNH}, the FPGA never asserts BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device remains BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{WRITE}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 19.

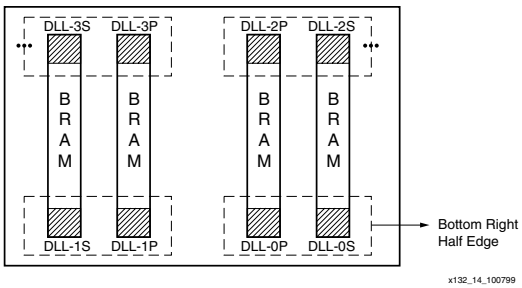


Figure 26: **Virtex Series DLLs**

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL produces an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 µs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED stays High and remains High when the clock is restored.

When the clock is stopped, one to four more clocks are still observed as the delay line is flushed. When the clock is restarted, the output clocks are not observed for one to four clocks as the delay line is filled. The most common case is two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift propagates one to four clocks to the output after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Useful Application Examples

The Virtex-E DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications. The Verilog and VHDL example files are available at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Standard Usage

The circuit shown in Figure 27 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

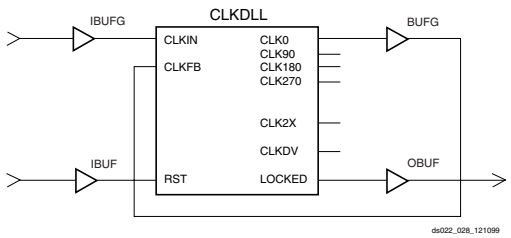


Figure 27: **Standard DLL Implementation**

Board Level De-Skew of Multiple Non-Virtex-E Devices

The circuit shown in Figure 28 can be used to de-skew a system clock between a Virtex-E chip and other non-Virtex-E chips on the same board. This application is commonly used when the Virtex-E device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

Port Signals

Each block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 15 describes the depth and width aspect ratios for the block SelectRAM+ memory.

Table 15: **Block SelectRAM+ Port Aspect Ratios**

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A/B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A/B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A/B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A/B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A/B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 15.

Data In Bus—DI[A/B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 15.

Data Output Bus—DO[A/B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 15.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$Start = ((ADDR_{port} + 1) * Width_{port}) - 1$$

$$End = ADDR_{port} * Width_{port}$$

Table 16 shows low order address mapping for each port width.

Table 16: **Port Address Mapping**

Port Width	Port Addresses																
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

Creating Larger RAM Structures

The block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

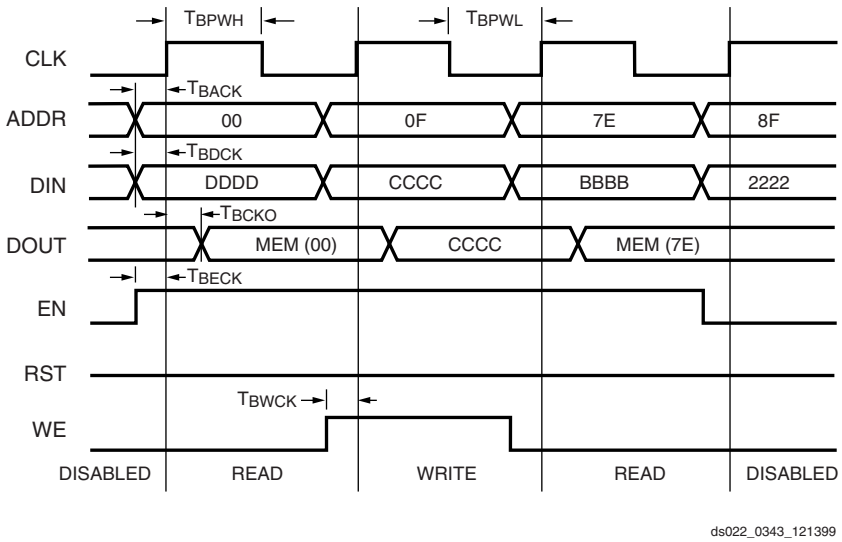


Figure 33: **Timing Diagram for Single Port Block SelectRAM+ Memory**

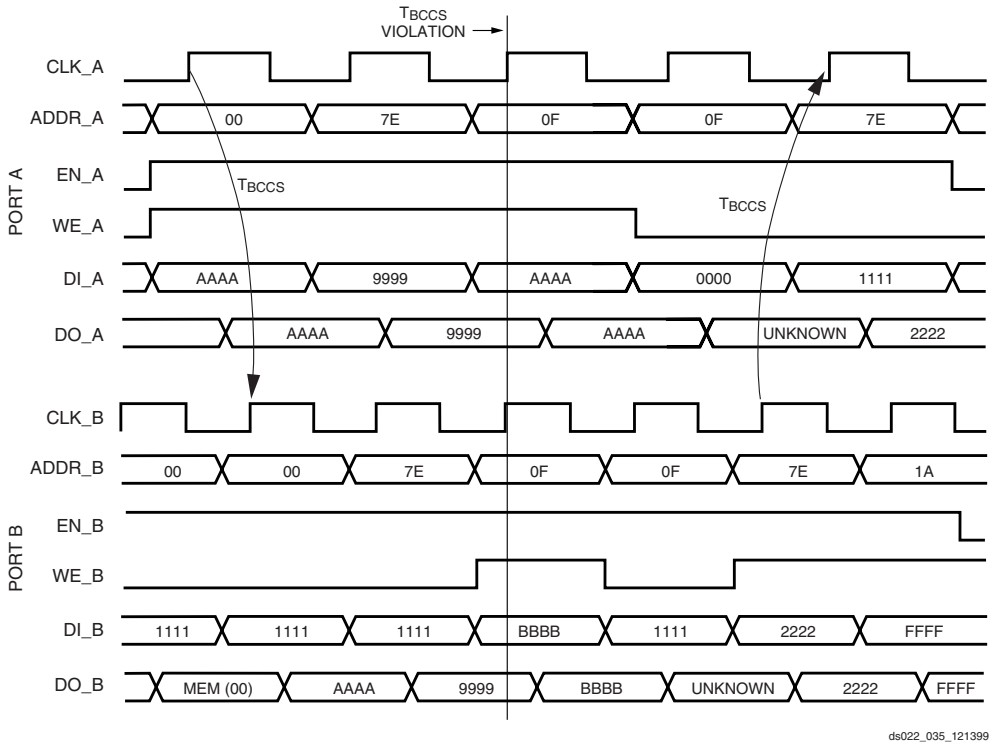


Figure 34: **Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory**

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x0F is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows.

```
OBUFT_<slew_rate>_<drive_strength>
```

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

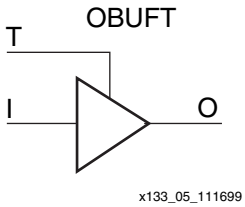


Figure 41: **3-State Output Buffer Symbol (OBUFT)**

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP
- OBUFT_LVCMOS18
- OBUFT_LVDS
- OBUFT_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

The SelectI/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak “keeper” circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak “keeper” circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak “keeper” typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 42.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows.

```
IOBUF_<slew_rate>_<drive_strength>
```

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

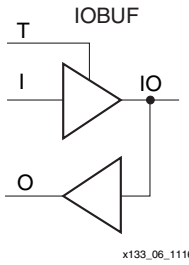


Figure 42: **Input/Output Buffer Symbol (IOBUF)**

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 38 on page 34 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

SelectI/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

Creating LVDS Output Buffers

LVDS output buffer can be placed in wide number of IOB locations. The exact location are dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Both output buffers are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other, and if output registers are used, the INIT states must be opposite values (one HIGH and one LOW). Failure to follow these rules leads to DRC errors in software.

VHDL Instantiation

```
data0_p  : OBUF_LVDS port map
(I=>data_int(0),   O=>data_p(0));

data0_inv: INV       port map
(I=>data_int(0),   O=>data_n_int(0));

data0_n  : OBUF_LVDS port map
(I=>data_n_int(0), O=>data_n(0));
```

Verilog Instantiation

```
OBUF_LVDS data0_p   (.I(data_int[0]),
.O(data_p[0]));

INV       data0_inv (.I(data_int[0],
.O(data_n_int[0]);

OBUF_LVDS data0_n   (.I(data_n_int[0]),
.O(data_n[0]));
```

Location Constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this can be done with the following constraint in the UCF or NCF file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Outputs

If the outputs are synchronous (registered in the IOB), then any IO_L#PIN pair can be used. If the outputs are asynchronous (no output register), then they must use one of the pairs that are part of the same IOB group at the end of a ROW or at the top/bottom of a COLUMN in the device.

The LVDS pairs that can be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous-capable for all devices in that package, and others are marked as available only for that device in the package. If the device size might change at some point in the product lifetime, then only the common pairs for all packages should be used.

Adding an Output Register

All LVDS buffers can have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements can be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The clock pin (C), clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this leads to a DRC error in the software.

The register elements can be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The output library macros are listed in Table 43. The O and OB inputs to the macros are the external net connections.

Table 43: **Output Library Macros**

Name	Inputs	Outputs
OBUFDS_FD_LVDS	D, C	O, OB
OBUFDS_FDE_LVDS	DD, CE, C	O, OB
OBUFDS_FDC_LVDS	D, C, CLR	O, OB
OBUFDS_FDCE_LVDS	D, CE, C, CLR	O, OB
OBUFDS_FDP_LVDS	D, C, PRE	O, OB
OBUFDS_FDPE_LVDS	D, CE, C, PRE	O, OB
OBUFDS_FDR_LVDS	D, C, R	O, OB
OBUFDS_FDRE_LVDS	D, CE, C, R	O, OB
OBUFDS_FDS_LVDS	D, C, S	O, OB
OBUFDS_FDSE_LVDS	D, CE, C, S	O, OB
OBUFDS_LD_LVDS	D, G	O, OB
OBUFDS_LDE_LVDS	D, GE, G	O, OB
OBUFDS_LDC_LVDS	D, G, CLR	O, OB
OBUFDS_LDCE_LVDS	D, GE, G, CLR	O, OB
OBUFDS_LDP_LVDS	D, G, PRE	O, OB
OBUFDS_LDPE_LVDS	D, GE, G, PRE	O, OB

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade(1)				Units
			Min	-8	-7	-6	
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0.0	0.0	0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2	–0.02	0.0	0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18	–0.02	+0.20	+0.20	+0.20	ns
	T_{ILVDS}	LVDS	0.00	+0.15	+0.15	+0.15	ns
	$T_{ILVPECL}$	LVPECL	0.00	+0.15	+0.15	+0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	–0.05	+0.08	+0.08	+0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	–0.05	–0.11	–0.11	–0.11	ns
	T_{IGTL}	GTL	+0.10	+0.14	+0.14	+0.14	ns
	$T_{IGTLPLUS}$	GTL+	+0.06	+0.14	+0.14	+0.14	ns
	T_{IHSTL}	HSTL	+0.02	+0.04	+0.04	+0.04	ns
	T_{ISSTL2}	SSTL2	–0.04	+0.04	+0.04	+0.04	ns
	T_{ISSTL3}	SSTL3	–0.02	+0.04	+0.04	+0.04	ns
	T_{ICTT}	CTT	+0.01	+0.10	+0.10	+0.10	ns
	T_{IAGP}	AGP	–0.03	+0.04	+0.04	+0.04	ns

Notes:
1. Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 3.

I

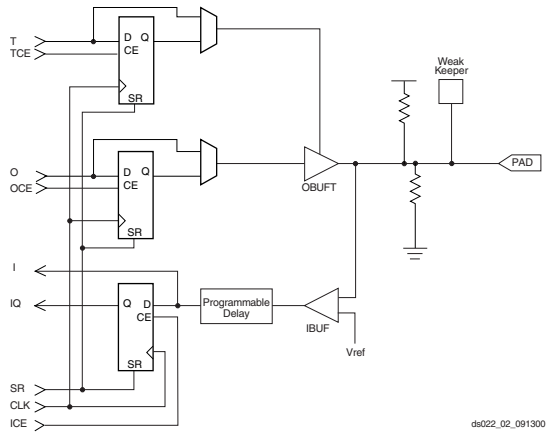


Figure 1: **Virtex-E Input/Output Block (IOB)**

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

			Speed Grade				
Description	**Symbol**	**Standard**	**Min**	**-8**	**-7**	**-6**	**Units**
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow, 2 mA	4.2	+14.7	+14.7	+14.7	ns
	T_{OLVTTL_S4}	4 mA	2.5	+7.5	+7.5	+7.5	ns
	T_{OLVTTL_S6}	6 mA	1.8	+4.8	+4.8	+4.8	ns
	T_{OLVTTL_S8}	8 mA	1.2	+3.0	+3.0	+3.0	ns
	T_{OLVTTL_S12}	12 mA	1.0	+1.9	+1.9	+1.9	ns
	T_{OLVTTL_S16}	16 mA	0.9	+1.7	+1.7	+1.7	ns
	T_{OLVTTL_S24}	24 mA	0.8	+1.3	+1.3	+1.3	ns
	T_{OLVTTL_F2}	LVTTL, Fast, 2 mA	1.9	+13.1	+13.1	+13.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	+5.3	+5.3	+5.3	ns
	T_{OLVTTL_F6}	6 mA	0.20	+3.1	+3.1	+3.1	ns
	T_{OLVTTL_F8}	8 mA	0.10	+1.0	+1.0	+1.0	ns
	T_{OLVTTL_F12}	12 mA	0.0	0.0	0.0	0.0	ns
	T_{OLVTTL_F16}	16 mA	–0.10	–0.05	–0.05	–0.05	ns
	T_{OLVTTL_F24}	24 mA	–0.10	–0.20	–0.20	–0.20	ns
	$T_{OLVCMOS\_2}$	LVCMOS2	0.10	+0.09	+0.09	+0.09	ns
	$T_{OLVCMOS\_18}$	LVCMOS18	0.10	+0.7	+0.7	+0.7	ns
	T_{OLVDS}	LVDS	–0.39	–1.2	–1.2	–1.2	ns
	$T_{OLVPECL}$	LVPECL	–0.20	–0.41	–0.41	–0.41	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	+2.3	+2.3	+2.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	–0.41	–0.41	–0.41	ns
	T_{OGTL}	GTL	0.6	+0.49	+0.49	+0.49	ns
	T_{OGTLP}	GTL+	0.7	+0.8	+0.8	+0.8	ns
	T_{OHSTL_I}	HSTL I	0.10	–0.51	–0.51	–0.51	ns
	T_{OHSTL_IIII}	HSTL III	–0.10	–0.91	–0.91	–0.91	ns
	T_{OHSTL_IV}	HSTL IV	–0.20	–1.01	–1.01	–1.01	ns
	T_{OSSTL2_I}	SSTL2 I	–0.10	–0.51	–0.51	–0.51	ns
	T_{OSSTL2_II}	SSTL2 II	–0.20	–0.91	–0.91	–0.91	ns
	T_{OSSTL3_I}	SSTL3 I	–0.20	–0.51	–0.51	–0.51	ns
	T_{OSSTL3_II}	SSTL3 II	–0.30	–1.01	–1.01	–1.01	ns
	T_{OCTT}	CTT	0.0	–0.61	–0.61	–0.61	ns
	T_{OAGP}	AGP	–0.1	–0.91	–0.91	–0.91	ns

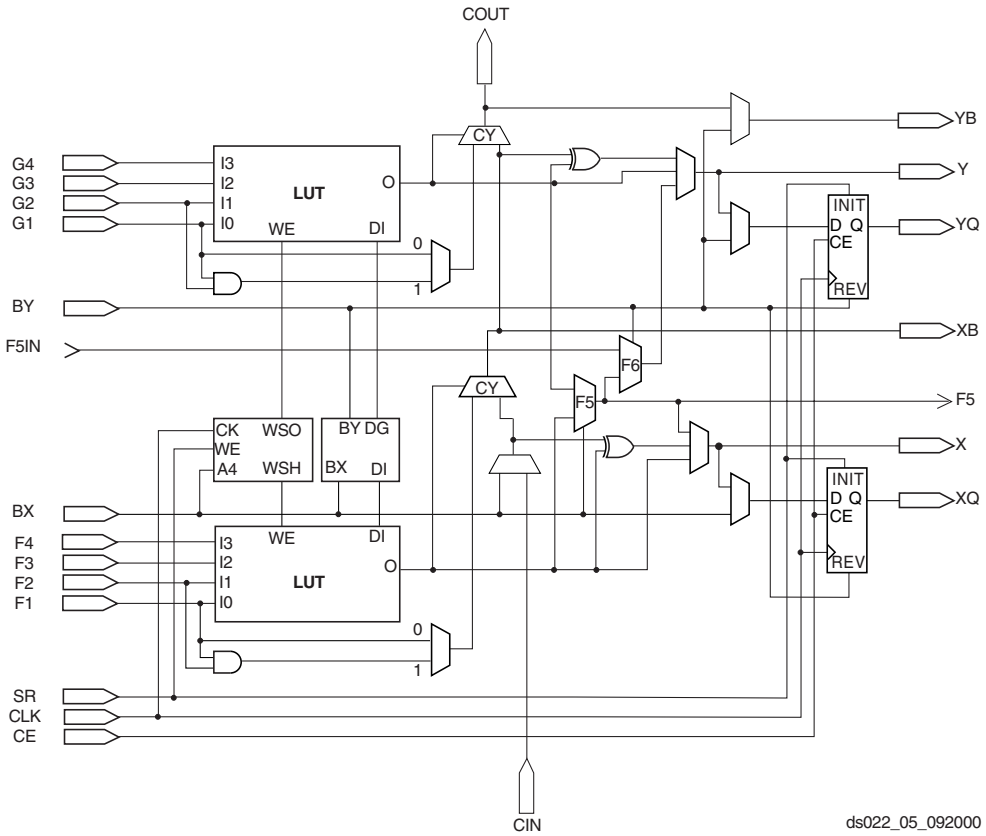


Figure 2: **Detailed View of Virtex-E Slice**

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

Description[1]	Symbol	Speed Grade				Units
		Min	-8	-7	-6	
Combinatorial Delays						
F operand inputs to X via XOR	T_{OPX}	0.32	0.68	0.8	0.8	ns, max
F operand input to XB output	T_{OPXB}	0.35	0.65	0.8	0.9	ns, max
F operand input to Y via XOR	T_{OPY}	0.59	1.07	1.4	1.5	ns, max
F operand input to YB output	T_{OPYB}	0.48	0.89	1.1	1.3	ns, max
F operand input to COUT output	T_{OPCYF}	0.37	0.71	0.9	1.0	ns, max
G operand inputs to Y via XOR	T_{OPGY}	0.34	0.72	0.8	0.9	ns, max
G operand input to YB output	T_{OPGYB}	0.47	0.78	1.2	1.3	ns, max
G operand input to COUT output	T_{OPCYG}	0.36	0.60	0.9	1.0	ns, max
BX initialization input to COUT	T_{BXCY}	0.19	0.36	0.51	0.57	ns, max
CIN input to X output via XOR	T_{CINX}	0.27	0.50	0.6	0.7	ns, max
CIN input to XB	T_{CINXB}	0.02	0.04	0.07	0.08	ns, max
CIN input to Y via XOR	T_{CINY}	0.26	0.45	0.7	0.7	ns, max
CIN input to YB	T_{CINYB}	0.16	0.28	0.38	0.43	ns, max
CIN input to COUT output	T_{BYP}	0.05	0.10	0.14	0.15	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.10	0.30	0.35	0.39	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.28	0.56	0.7	0.8	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.17	0.38	0.46	0.51	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.20	0.46	0.55	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.09	0.28	0.30	0.34	ns, max
Setup and Hold Times before/after Clock CLK						
CIN input to FFX	T_{CCKX}/T_{CKCX}	0.47 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}	0.49 / 0	0.92 / 0	1.2 / 0	1.3 / 0	ns, min

Notes:

1. A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Virtex-E Pin-to-Pin Input Parameter Guidelines

All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

Description[1]	Symbol	Device[3]	Speed Grade[2]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.							
No Delay	T_{PSDLL}/T_{PHDLL}	XCV405E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns
Global Clock and IFF, with DLL		XCV812E	1.5 / –0.4	1.5 / –0.4	1.6 / –0.4	1.7 / –0.4	ns

Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. DLL output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

Description[1]	Symbol	Device[3]	Speed Grade[2]				Units
			Min	-8	-7	-6	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 6.							
Full Delay	T_{PSFD}/T_{PHFD}	XCV405E	2.3 / 0	2.3 / 0	2.3 / 0	2.3 / 0	ns
Global Clock and IFF, without DLL		XCV812E	2.5 / 0	2.5 / 0	2.5 / 0	2.5 / 0	ns

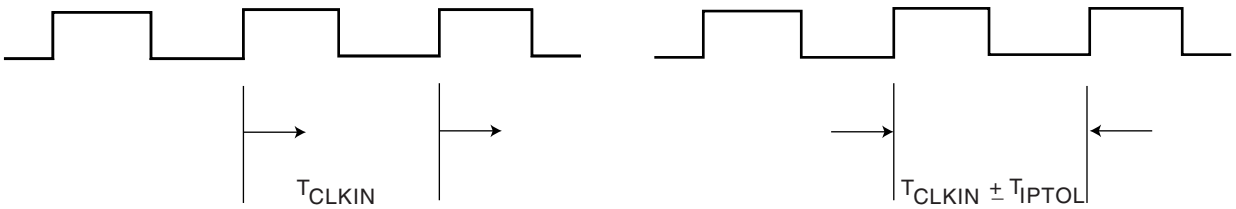
Notes:
1. IFF = Input Flip-Flop or Latch
2. Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.
3. A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

DLL Timing Parameters

All devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

Description	Symbol	F_{CLKIN}	Speed Grade						Units
			-8		-7		-6		
			Min	Max	Min	Max	Min	Max	
Input Clock Frequency (CLKDLLHF)	FCLKINHF		60	320	60	320	60	260	MHz
Input Clock Frequency (CLKDLL)	FCLKINLF		25	160	25	160	25	135	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥25 MHz	5.0		5.0		5.0		ns
		≥50 MHz	3.0		3.0		3.0		ns
		≥100 MHz	2.4		2.4		2.4		ns
		≥150 MHz	2.0		2.0		2.0		ns
		≥200 MHz	1.8		1.8		1.8		ns
		≥250 MHz	1.5		1.5		1.5		ns
		≥300 MHz	1.3		1.3		NA		ns

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

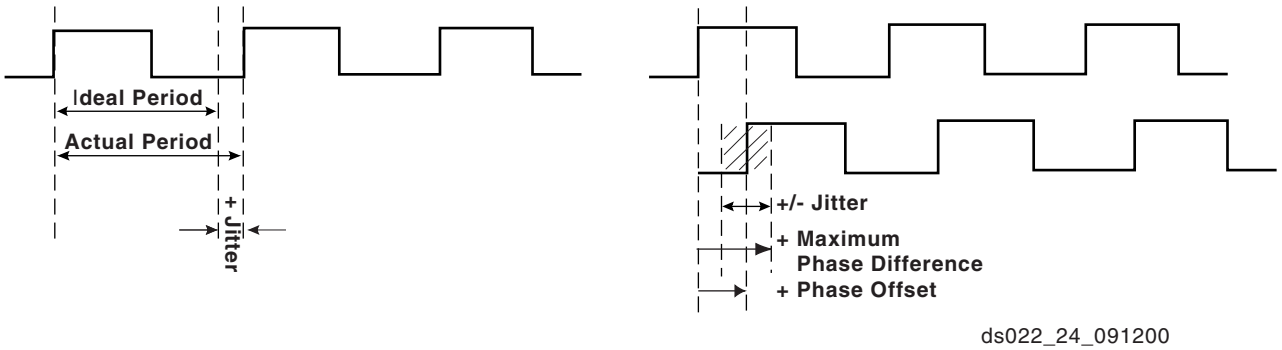


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Figure 4: **DLL Timing Waveforms**

Date	Version	Revision
11/20/00	1.3	• Updated speed grade -8 numbers in **Virtex-E Electrical Characteristics** tables (Module 3). • Updated minimums in Table 11 (Module 2), and added notes to Table 12 (Module 2). • Added to note 2 of **Absolute Maximum Ratings** (Module 3). • Changed all minimum hold times to –0.4 for **Global Clock Set-Up and Hold for LVTTL Standard, with DLL** (Module 3). • Revised maximum T_{DLLPW} in -6 speed grade for **DLL Timing Parameters** (Module 3).
04/02/01	1.4	• In Table 4, **FG676 Fine-Pitch BGA — XCV405E**, pin B19 is no longer labeled as VREF, and pin G16 is now labeled as VREF. • Updated values in Virtex-E Switching Characteristics tables. • Converted data sheet to modularized format. See the Virtex-E Extended Memory Data Sheet section.
04/19/01	1.5	• Updated values in Virtex-E Switching Characteristics tables.
07/23/01	1.6	• Under Absolute Maximum Ratings, changed (T_{SOL}) to 220 °C . • Changes made to SSTL symbol names in IOB Input Switching Characteristics Standard Adjustments table.
07/26/01	1.7	• Removed T_{SOL} parameter and added footnote to Absolute Maximum Ratings table.
09/18/01	1.8	• Reworded power supplies footnote to Absolute Maximum Ratings table.
10/25/01	1.9	• Updated the speed grade designations used in data sheets, and added Table 1, which shows the current speed grade designation for each device. • Updated Power-On Power Supply Requirements table.
11/09/01	2.0	• Updated the XCV405E device speed grade designation to Preliminary in Table 1. • Updated Power-On Power Supply Requirements table.
02/01/02	2.1	• Updated footnotes to the DC Input and Output Levels and DLL Clock Tolerance, Jitter, and Phase Information tables.
07/17/02	2.2	• Data sheet designation upgraded from Preliminary to Production. • Removed mention of MIL-M-38510/605 specification. • Added link to XAPP158 from the Power-On Power Supply Requirements section.
09/10/02	2.3	• Revised V_{IN} in Absolute Maximum Ratings Table. Added Clock CLK switching characteristics to "IOB Input Switching Characteristics" on page 5 and "IOB Output Switching Characteristics, Figure 1" on page 7.
12/22/02	2.3.1	• Added footnote regarding V_{IN} PCI compliance to Absolute Maximum Ratings table.
03/14/03	2.3.2	• Under Power-On Power Supply Requirements, the fastest ramp rate is no longer a "suggested" rate.

Virtex-E Extended Memory Data Sheet

The Virtex-E Extended Memory Data Sheet contains the following modules:

- DS025-1, Virtex-E 1.8V Extended Memory FPGAs: **Introduction and Ordering Information (Module 1)**
- DS025-2, Virtex-E 1.8V Extended Memory FPGAs: **Functional Description (Module 2)**
- DS025-3, Virtex-E 1.8V Extended Memory FPGAs: **DC and Switching Characteristics (Module 3)**
- DS025-4, Virtex-E 1.8V Extended Memory FPGAs: **Pinout Tables (Module 4)**

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

50	2	H5	E2	NA	-
51	2	H4	G3	√	VREF_2
52	2	J5	F1	NA	-
53	2	J4	H3	2	-
54	2	K5	H2	NA	VREF_2
55	2	J3	K4	NA	-
56	2	L5	K3	√	D1
57	2	L4	K2	√	D2
58	2	M5	L3	2	-
59	2	L1	M4	NA	-
60	2	N5	M2	1	VREF_2
61	2	N4	N3	1	-
62	2	N2	P5	NA	-
63	2	P4	P3	√	D3
64	2	P2	R5	2	-
65	2	R4	R3	NA	-
66	2	R1	T4	NA	VREF_2
67	2	T5	T3	NA	-
68	2	T2	U3	√	IRDY
69	3	U1	U2	NA	-
70	3	V2	V4	NA	VREF_3
71	3	V5	V3	NA	-
72	3	W1	W3	2	-
73	3	W4	W5	√	VREF_3
74	3	Y3	Y4	NA	-
75	3	AA1	Y5	1	-
76	3	AA3	AA4	1	VREF_3
77	3	AB3	AA5	NA	-
78	3	AC1	AB4	2	-
79	3	AC3	AB5	√	D5
80	3	AC4	AD3	√	VREF_3
81	3	AE1	AC5	1	-
82	3	AD4	AF1	NA	VREF_3
83	3	AF2	AD5	NA	-

Table 2: **BG560 Package Differential Pin Pair Summary XCV405E and XCV812E**

84	3	AG2	AE4	NA	-
85	3	AH1	AE5	√	VREF_3
86	3	AF4	AJ1	NA	-
87	3	AJ2	AF5	2	-
88	3	AG4	AK2	1	VREF_3
89	3	AJ3	AG5	NA	-
90	3	AL1	AH4	NA	-
91	3	AJ4	AH5	√	INIT
92	4	AL4	AJ6	√	-
93	4	AK5	AN3	NA	-
94	4	AL5	AJ7	√	-
95	4	AM4	AM5	√	VREF_4
96	4	AK7	AL6	1	-
97	4	AM6	AN6	√	-
98	4	AL7	AJ9	√	VREF_4
99	4	AN7	AL8	NA	-
100	4	AM8	AJ10	1	-
101	4	AL9	AM9	1	VREF_4
102	4	AK10	AN9	1	-
103	4	AL10	AM10	√	VREF_4
104	4	AL11	AJ12	√	-
105	4	AN11	AK12	NA	-
106	4	AL12	AM12	√	-
107	4	AK13	AL13	√	VREF_4
108	4	AM13	AN13	1	-
109	4	AJ14	AK14	√	-
110	4	AM14	AN15	√	VREF_4
111	4	AJ15	AK15	NA	-
112	4	AL15	AM16	1	-
113	4	AL16	AJ16	1	VREF_4
114	4	AK16	AN17	1	-
115	5	AM17	AM18	NA	GCLK LVDS 1/0
116	5	AK18	AJ18	1	VREF_5
117	5	AN19	AL19	1	-

Table 3: **FG676 Fine-Pitch BGA — XCV405E**

Bank	Pin Description	Pin #
1	IO_L25P_YY	C15
1	IO_L26N_YY	E15
1	IO_VREF_L26P_YY	D15
1	IO_L27N_YY	C16
1	IO_L27P_YY	F15
1	IO_L28N	G15
1	IO_L28P	D16
1	IO_L29N_YY	E16
1	IO_L29P_YY	A17
1	IO_L30N_YY	C17
1	IO_L30P_YY	E17
1	IO_L31N_Y	F16
1	IO_L31P_Y	D17
1	IO_L32N_YY	F17
1	IO_L32P_YY	C18
1	IO_L33N_YY	A18
1	IO_VREF_L33P_YY	G16
1	IO_L34N_YY	C19
1	IO_L34P_YY	G17
1	IO_L35N_Y	D18
1	IO_L35P_Y	B19
1	IO_L36N_Y	D19
1	IO_L36P_Y	E18
1	IO_L37N_YY	F18
1	IO_L37P_YY	B20
1	IO_L38N_YY	G19
1	IO_VREF_L38P_YY	C20
1	IO_L39N_YY	G18
1	IO_L39P_YY	E19
1	IO_L40N_YY	A21
1	IO_L40P_YY	D20
1	IO_L41N_YY	F19
1	IO_VREF_L41P_YY	C21
1	IO_L42N_YY	B22
1	IO_L42P_YY	E20
1	IO_L43N_Y	A23
1	IO_L43P_Y	D21
1	IO_WRITE_L44N_YY	C22
1	IO_CS_L44P_YY	E21
2	IO	D26
2	IO	E26
2	IO	F26
2	IO_D1	K24
2	IO_DOUT_BUSY_L45P_YY	E23
2	IO_DIN_D0_L45N_YY	F22
2	IO_L46P_YY	E24
2	IO_L46N_YY	F20
2	IO_L47P_Y	G21
2	IO_L47N_Y	G22
2	IO_VREF_L48P_Y	F24
2	IO_L48N_Y	H20
2	IO_L49P_Y	E25
2	IO_L49N_Y	H21
2	IO_L50P_YY	F23
2	IO_L50N_YY	G23
2	IO_VREF_L51P_YY	H23
2	IO_L51N_YY	J20
2	IO_L52P_YY	G24
2	IO_L52N_YY	H22
2	IO_L53P_Y	J21
2	IO_L53N_Y	G25
2	IO_L54P_Y	G26
2	IO_L54N_Y	J22
2	IO_L55P_YY	H24
2	IO_L55N_YY	J23
2	IO_L56P_YY	J24
2	IO_VREF_L56N_YY	K20
2	IO_D2_L57P_YY	K22
2	IO_L57N_YY	K21

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
0	IO_L29N	D14
0	IO_L29P	B14
0	IO_L30N_YY	A14
0	IO_L30P_YY	J14
0	IO_VREF_L31N_YY	K14
0	IO_L31P_YY	J15
0	IO_LVDS_DLL_L34N	A15
1	GCk2	E15
1	IO	B18
1	IO	B21
1	IO	B28
1	IO	C23
1	IO	C26
1	IO	D20
1	IO	D23
1	IO_LVDS_DLL_L34P	E16
1	IO_L35N	B16
1	IO_L35P	F16
1	IO_L36N	A16
1	IO_L36P	H16
1	IO_L37N_YY	C16
1	IO_VREF_L37P_YY	K15
1	IO_L38N_YY	K16
1	IO_L38P_YY	G16
1	IO_L39N	A17
1	IO_L39P	E17
1	IO_L40N	F17
1	IO_L40P	C17
1	IO_L41N_YY	E18
1	IO_VREF_L41P_YY	A18
1	IO_L42N_YY	D18
1	IO_L42P_YY	A19
1	IO_L43N	B19

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
1	IO_L43P	G18
1	IO_L44N	D19
1	IO_L44P	H18
1	IO_L45N_YY	F18
1	IO_VREF_L45P_YY	F19
1	IO_L46N_YY	B20
1	IO_L46P_YY	K17
1	IO_L48N_Y	G19
1	IO_L48P_Y	C20
1	IO_L49N_Y	K18
1	IO_L49P_Y	E20
1	IO_L51N_YY	F20
1	IO_L51P_YY	A21
1	IO_L52N_YY	C21
1	IO_VREF_L52P_YY	A22
1	IO_L53N	H19
1	IO_L53P	B22
1	IO_L54N	E21
1	IO_L54P	D22
1	IO_L55N_YY	F21
1	IO_VREF_L55P_YY	C22
1	IO_L56N_YY	H20
1	IO_L56P_YY	E22
1	IO_L57N	G21
1	IO_L57P	A23
1	IO_L58N	A24
1	IO_L58P	K19
1	IO_L59N_YY	C24
1	IO_VREF_L59P_YY	B24
1	IO_L60N_YY	H21
1	IO_L60P_YY	G22
1	IO_L61N	E23
1	IO_L61P	C25
1	IO_L62N	D24

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
6	IO_L232P_Y	AA6
6	IO_L233N	Y6
6	IO_L233P	Y4
6	IO_L235N	Y3
6	IO_L235P	Y2
6	IO_VREF_L236N_Y	Y5
6	IO_L236P_Y	W5
6	IO_L237N_YY	W4
6	IO_L237P_YY	W6
6	IO_L238N	V6
6	IO_L238P	W2
6	IO_L239N	U9
6	IO_L239P	V4
6	IO_VREF_L240N_YY	AB2
6	IO_L240P_YY	T8
6	IO_L241N_YY	U5
6	IO_L241P_YY	W1
6	IO_L242N_Y	Y1
6	IO_L242P_Y	T9
6	IO_L243N	T7
6	IO_L243P	U3
6	IO_VREF_L244N	T5
6	IO_L244P	V2
6	IO_L246N	T4
6	IO_L246P	U2
6	IO_L247N	T1
7	IO	D1
7	IO	E3
7	IO	J4
7	IO	J6
7	IO	K10
7	IO	L3
7	IO	M7

Table 5: **FG900 Fine-Pitch BGA Package — XCV812E**

Bank	Description	Pin
7	IO	N8
7	IO	R5
7	IO_L247P	R10
7	IO_L249N	R8
7	IO_L249P	R4
7	IO_L250N	R7
7	IO_L250P	R3
7	IO_L251N	P10
7	IO_VREF_L251P	P6
7	IO_L252N	P5
7	IO_L252P	P2
7	IO_L253N_Y	P7
7	IO_L253P_Y	P4
7	IO_L254N_YY	N4
7	IO_L254P_YY	R2
7	IO_L255N_YY	N7
7	IO_VREF_L255P_YY	P1
7	IO_L256N	M6
7	IO_L256P	N6
7	IO_L257N	N5
7	IO_L257P	N1
7	IO_L258N_YY	M4
7	IO_L258P_YY	M5
7	IO_L259N_Y	M2
7	IO_VREF_L259P_Y	M1
7	IO_L260N	L4
7	IO_L260P	L2
7	IO_L262N	L1
7	IO_L262P	M8
7	IO_L263N_Y	K2
7	IO_L263P_Y	M9
7	IO_L265N_YY	K5
7	IO_L265P_YY	K1
7	IO_L266N_YY	L6