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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	100MHz
Connectivity	EBI/EMI, Ethernet, I²C, IrDA, SD, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I ² S, LCD, LVD, POR, PWM, WDT
Number of I/O	94
Program Memory Size	256КВ (256К х 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 41x16b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LBGA
Supplier Device Package	144-MAPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk53dx256cmd10

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Terminology and guidelines





3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.



4 Ratings

4.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free		260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level		3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

4.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

2. Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.

4.4 Voltage and current operating ratings



Symbol	Description	Min.	Max.	Unit
V _{DD}	Digital supply voltage	-0.3	3.8	V
I _{DD}	Digital supply current	—	185	mA
V _{DIO}	Digital input voltage (except RESET, EXTAL, and XTAL)	-0.3	5.5	V
V _{AIO}	Analog ¹ , RESET, EXTAL, and XTAL input voltage	-0.3	V _{DD} + 0.3	V
I _D	Maximum current single pin limit (applies to all digital pins)	-25	25	mA
V _{DDA}	Analog supply voltage	V _{DD} – 0.3	V _{DD} + 0.3	V
$V_{USB_{DP}}$	USB_DP input voltage	-0.3	3.63	V
V _{USB_DM}	USB_DM input voltage	-0.3	3.63	V
VREGIN	USB regulator input	-0.3	6.0	V
V _{BAT}	RTC battery supply voltage	-0.3	3.8	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

5 General

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + $(V_{IH} - V_{IL})/2$.

Figure 1. Input signal measurement reference

All digital I/O switching characteristics assume:

- 1. output pins
 - have C_L=30pF loads,
 - are configured for fast slew rate (PORTx_PCRn[SRE]=0), and
 - are configured for high drive strength (PORTx_PCRn[DSE]=1)
- 2. input pins
 - have their passive filter disabled (PORTx_PCRn[PFE]=0)

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5.2.3 Voltage and current operating behaviors Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
V _{OH}	Output high voltage — high drive strength					
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -9mA	V _{DD} – 0.5	_	_	V	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OH} = -3mA	V _{DD} – 0.5	—	—	V	
	Output high voltage — low drive strength					
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -2mA	V _{DD} – 0.5		_	V	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OH} = -0.6mA	V _{DD} – 0.5	_	_	V	
I _{OHT}	Output high current total for all ports	_		100	mA	
V _{OL}	Output low voltage — high drive strength					2
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 10mA	_	_	0.5	V	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OL} = 5mA	_	_	0.5	V	
	Output low voltage — low drive strength					-
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 2mA	_	—	0.5	v	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OL} = 1mA	_	—	0.5	v	
I _{OLT}	Output low current total for all ports	_		100	mA	
I _{INA}	Input leakage current, analog pins and digital pins configured as analog inputs					3, 4
	• $V_{SS} \le V_{IN} \le V_{DD}$					
	All pins except EXTAL32, XTAL32, EXTAL, XTAL	_	0.002	0.5	μA	
	• EXTAL (PTA18) and XTAL (PTA19)	_	0.004	1.5	μA	
	• EXTAL32, XTAL32	_	0.075	10	μA	
I _{IND}	Input leakage current, digital pins					4, 5
	• $V_{SS} \le V_{IN} \le V_{IL}$					
	All digital pins	_	0.002	0.5	μA	
	• V _{IN} = V _{DD}					
	All digital pins except PTD7	_	0.002	0.5	μA	
	• PTD7	_	0.004	1	μA	
I _{IND}	Input leakage current, digital pins					4, 5, 6
	• $V_{IL} < V_{IN} < V_{DD}$					
	• V _{DD} = 3.6 V	_	18	26	μA	
	• V _{DD} = 3.0 V	_	12	49	μA	
	• V _{DD} = 2.5 V	_	8	13	μA	
	• V _{DD} = 1.7 V	-	3	6	μA	

Table continues on the next page ...

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6.1.1 Debug trace timing specifications

Table 12. Debu	g trace operating	behaviors
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Symbol	Description	Min.	Max.	Unit	
T _{cyc}	Clock period	Frequency	Frequency dependent		
T _{wl}	Low pulse width	2	—	ns	
T _{wh}	High pulse width	2	_	ns	
Tr	Clock and data rise time	—	3	ns	
T _f	Clock and data fall time	—	3	ns	
Ts	Data setup	3	—	ns	
T _h	Data hold	2	—	ns	



Figure 3. TRACE_CLKOUT specifications



Figure 4. Trace data specifications

6.1.2 JTAG electricals



Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	Boundary Scan	0	10	
	JTAG and CJTAG	0	25	
	Serial Wire Debug	0	50	
J2	TCLK cycle period	1/J1		ns

Table continues on the next page ...

6.4.1.5 Write endurance to FlexRAM for EEPROM

When the FlexNVM partition code is not set to full data flash, the EEPROM data set size can be set to any of several non-zero values.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

 $Writes_subsystem = \frac{EEPROM - 2 \times EEESPLIT \times EEESIZE}{EEESPLIT \times EEESIZE} \times Write_efficiency \times n_{nvmcycd}$

where

- Writes_subsystem minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency
 - 0.25 for 8-bit writes to FlexRAM
 - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} data flash cycling endurance (the following graph assumes 10,000 cycles)



rempheral operating requirements and behaviors

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
C _{rate}	ADC conversion	≤ 13 bit modes	18.484	—	450	Ksps	7
ra	rate	No ADC hardware averaging					
		Continuous conversions enabled					
		Peripheral clock = 50 MHz					
		16 bit modes	37.037	_	250	Ksps	8
		No ADC hardware averaging					
		Continuous conversions enabled					
		Peripheral clock = 50 MHz					

Table 29. 16-bit ADC with PGA operating conditions (continued)

- 1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{ADCK} = 6 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
- 2. ADC must be configured to use the internal voltage reference (VREF_OUT)
- 3. PGA reference is internally connected to the VREF_OUT pin. If the user wishes to drive VREF_OUT with a voltage other than the output of the VREF module, the VREF module must be disabled.
- 4. For single ended configurations the input impedance of the driven input is R_{PGAD}/2
- 5. The analog source resistance (R_{AS}), external to MCU, should be kept as minimum as possible. Increased R_{AS} causes drop in PGA gain without affecting other performances. This is not dependent on ADC clock frequency.
- 6. The minimum sampling time is dependent on input signal frequency and ADC mode of operation. A minimum of 1.25µs time should be allowed for Fin=4 kHz at 16-bit differential mode. Recommended ADC setting is: ADLSMP=1, ADLSTS=2 at 8 MHz ADC clock.
- 7. ADC clock = 18 MHz, ADLSMP = 1, ADLST = 00, ADHSC = 1
- 8. ADC clock = 12 MHz, ADLSMP = 1, ADLST = 01, ADHSC = 1

6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC PGA[PGACHPb] =0)

Table 30. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ. ¹	Max.	Unit	Notes
I _{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	_	420	644	μA	2
I _{DC_PGA}	Input DC current		$\frac{2}{R_{\text{PGAD}}} \left(\frac{1}{2}\right)$	V _{REFPGA} ×0.5 (Gain+	$\frac{83}{1} - V_{CM}$	A	3
		Gain =1, V_{REFPGA} =1.2V, V_{CM} =0.5V	_	1.54		μA	
		Gain =64, V_{REFPGA} =1.2V, V_{CM} =0.1V		0.57		μA	

Table continues on the next page ...



Symbol	Description	Min.	Тур.	Max.	Unit
V _H	Analog comparator hysteresis ¹				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	 CR0[HYSTCTR] = 01 	—	10	—	mV
	• CR0[HYSTCTR] = 10	_	20	—	mV
	 CR0[HYSTCTR] = 11 	—	30	—	mV
V _{CMPOh}	Output high	V _{DD} – 0.5	_	—	V
V _{CMPOI}	Output low		_	0.5	V
t _{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t _{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay ²	_	_	40	μs
I _{DAC6b}	6-bit DAC current adder (enabled)	_	7	—	μA
INL	6-bit DAC integral non-linearity	-0.5	_	0.5	LSB ³
DNL	6-bit DAC differential non-linearity	-0.3	_	0.3	LSB

Table 31. Comparator and 6-bit DAC electrical specifications (continued)

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD} -0.6 V.

2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.

3. 1 LSB = $V_{reference}/64$



Peripheral operating requirements and behaviors



Figure 17. Typical hysteresis vs. Vin level (VDD=3.3V, PMODE=1)

6.6.3 12-bit DAC electrical characteristics

6.6.3.1 12-bit DAC operating requirements Table 32. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	1.71 3.6		V	
V _{DACR}	Reference voltage	1.13	3.6	V	1
T _A	Temperature	Operating t range of t	emperature he device	°C	
CL	Output load capacitance	_	100	pF	2
١L	Output load current		1	mA	

1. The DAC reference can be selected to be V_{DDA} or the voltage output of the VREF module (VREF_OUT)

2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC



rempheral	operating	requirements	and	behaviors
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Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{SUPPLY}	Supply current (I _{OUT} =0mA, CL=0) — Low-power mode	—	60	80	μA	
I _{SUPPLY}	Supply current (I _{OUT} =0mA, CL=0) — High-speed mode	_	280	450	μA	
V _{OS}	Input offset voltage	-20	—	20	mV	
α _{VOS}	Input offset voltage temperature coefficient	—	4.8	—	µV/C	
I _{OS}	Input offset current	—	±0.3	±5	nA	
I _{BIAS}	Input bias current	—	±0.3	±5	nA	
R _{IN}	Input resistance	500	—	—	MΩ	
C _{IN}	Input capacitance	—	17	—	pF	
R _{OUT}	Output AC impedance		_	1500	Ω	@ 100kHz,High speedmode
X _{IN}	AC input impedance (f _{IN} =100kHz)	—	159	—	kΩ	
CMRR	Input common mode rejection ratio	60	—	—	dB	
PSRR	Power supply rejection ratio	60	_	—	dB	
SR	Slew rate (ΔV_{IN} =100mV) — Low-power mode	0.1	—	—	V/µs	
SR	Slew rate (ΔV_{IN} =100mV) — High speed mode	1	—	—	V/µs	
GBW	Unity gain bandwidth — Low-power mode 50pF	0.15	—	—	MHz	
GBW	Unity gain bandwidth — High speed mode 50pF	1	_	—	MHz	
A _V	DC open-loop voltage gain	80	—	—	dB	
VOUT	Output voltage range	0.15	_	V _{DD} -0.15	V	
I _{OUT}	Output load current	—	±0.5	—	mA	
GM	Gain margin	—	20	—	dB	
PM	Phase margin	50	60	—	deg	
Vn	Voltage noise density (noise floor) 1kHz	—	280	—	nV/√Hz	
Vn	Voltage noise density (noise floor) 10kHz	—	100	—	nV/√Hz	

Table 36. TRIAMP full range operating behaviors

6.6.6 Transimpedance amplifier electrical specifications — limited range

Table 37. TRIAMP limited range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DDA}	Supply voltage	2.4	3.3	V	
V _{IN}	Input voltage range	0.1	V _{DDA} -1.4	V	
T _A	Temperature	0	50	С	
CL	Output load capacitance	—	100	pf	



6.8.1.1 MII signal switching specifications

The following timing specs meet the requirements for MII style interfaces for a range of transceiver devices.

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK
				period
MII2	RXCLK pulse width low	35%	65%	RXCLK
				period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5		ns
_	TXCLK frequency	_	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK
				period
MII6	TXCLK pulse width low	35%	65%	TXCLK
				period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2		ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

Table 43. MII signal switching specifications



Figure 20. MII transmit signal timing diagram



6.8.3 USB DCD electrical specifications

 Table 45.
 USB DCD electrical specifications

Symbol	Description	Min.	Тур.	Max.	Unit
V _{DP_SRC}	USB_DP source voltage (up to 250 µA)	0.5	—	0.7	V
V _{LGC}	Threshold voltage for logic high	0.8	—	2.0	V
I _{DP_SRC}	USB_DP source current	7	10	13	μA
I _{DM_SINK}	USB_DM sink current	50	100	150	μA
R _{DM_DWN}	D- pulldown resistance for data pin contact detect	14.25	_	24.8	kΩ
V _{DAT_REF}	Data detect voltage	0.25	0.33	0.4	V

6.8.4 USB VREG electrical specifications

Table 46. USB VREG electrical specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I _{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	_	120	186	μA	
I _{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	μA	
I _{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C	_	650	_	nA	
	Across operating voltage and temperature	—	_	4	μΑ	
I _{LOADrun}	Maximum load current — Run mode	—		120	mA	
I _{LOADstby}	Maximum load current — Standby mode	_	—	1	mA	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) > 3.6 V					
	Run mode	3	3.3	3.6	v	
	Standby mode	2.1	2.8	3.6	V	
V _{Reg33out}	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	_	3.6	V	2
C _{OUT}	External output capacitor	1.76	2.2	8.16	μF	
ESR	External output capacitor equivalent series resistance	1	_	100	mΩ	
I _{LIM}	Short circuit current	_	290	_	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 $^\circ\text{C}$ unless otherwise stated.

2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to ILoad.



rempheral operating requirements and behaviors

6. C_b = total capacitance of the one bus line in pF.



Figure 26. Timing definition for fast and standard mode devices on the I²C bus

6.8.8 UART switching specifications

See General switching specifications.

6.8.9 SDHC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

Num	Symbol	Description	Min.	Max.	Unit
		Operating voltage	1.71	3.6	V
		Card input clock	•	•	
SD1	fpp	Clock frequency (low speed)	0	400	kHz
	fpp	Clock frequency (SD\SDIO full speed\high speed)	0	25\50	MHz
	fpp	Clock frequency (MMC full speed\high speed)	0	20\50	MHz
	f _{OD}	Clock frequency (identification mode)	0	400	kHz
SD2	t _{WL}	Clock low time	7	—	ns
SD3	t _{WH}	Clock high time	7	—	ns
SD4	t _{TLH}	Clock rise time	—	3	ns
SD5	t _{THL}	Clock fall time	—	3	ns
		SDHC output / card inputs SDHC_CMD, SDHC_DAT	(reference to	SDHC_CLK)	•
SD6	t _{OD}	SDHC output delay (output valid)	-5	8.3	ns
	SDHC input / card inputs SDHC_CMD, SDHC_DAT (reference to SDHC_CLK)				
SD7	t _{ISU}	SDHC input setup time	5	_	ns
SD8	t _{IH}	SDHC input hold time	0	—	ns

Table 52. SDHC switching specifications



Table 54. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (limited voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	4.5	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	_	25	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



Figure 29. I2S/SAI timing — slave modes

6.8.10.2 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 55.I2S/SAI master mode timing in Normal Run, Wait and Stop modes
(full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	-1.0	—	ns

Table continues on the next page...



Table 55. I2S/SAI master mode timing in Normal Run, Wait and Stop modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S7	I2S_TX_BCLK to I2S_TXD valid	—	15	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	_	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	20.5	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



Figure 30. I2S/SAI timing — master modes

Table 56. I2S/SAI slave mode timing in Normal Run, Wait and Stop modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	5.8	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid			ns
	Multiple SAI Synchronous mode	-	24	
	All other modes	_	20.6	
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	_	ns

Table continues on the next page ...

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Table 57. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	45	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns



Figure 32. I2S/SAI timing — master modes

Table 58.I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full
voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	_	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	3	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	63	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid ¹	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear



144 LQFP	144 Map Bga	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
39	L4	TRI0_DM	TRIO_DM	TRI0_DM								
40	M4	TRI0_DP	TRI0_DP	TRI0_DP								
41	L5	TRI1_DM	TRI1_DM	TRI1_DM								
42	M5	TRI1_DP	TRI1_DP	TRI1_DP								
43	K5	TRI1_OUT/ CMP2_IN5/ ADC1_SE22	TRI1_OUT/ CMP2_IN5/ ADC1_SE22	TRI1_OUT/ CMP2_IN5/ ADC1_SE22								
44	K4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4								
45	J4	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	DAC1_OUT/ CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5								
46	M7	XTAL32	XTAL32	XTAL32								
47	M6	EXTAL32	EXTAL32	EXTAL32								
48	L6	VBAT	VBAT	VBAT								
49	H4	PTE28	DISABLED		PTE28				FB_AD20			
50	J5	PTA0	JTAG_TCLK/ SWD_CLK/ EZP_CLK	TSI0_CH1	PTAO	UARTO_CTS_ b/ UARTO_COL_ b	FTM0_CH5				JTAG_TCLK/ SWD_CLK	ezp_clk
51	J6	PTA1	JTAG_TDI/ EZP_DI	TSI0_CH2	PTA1	UART0_RX	FTM0_CH6				JTAG_TDI	EZP_DI
52	K6	PTA2	JTAG_TDO/ TRACE_SWO/ EZP_DO	TSI0_CH3	PTA2	UARTO_TX	FTM0_CH7				JTAG_TDO/ TRACE_SWO	EZP_DO
53	K7	PTA3	JTAG_TMS/ SWD_DIO	TSI0_CH4	PTA3	UARTO_RTS_ b	FTM0_CH0				JTAG_TMS/ SWD_DIO	
54	L7	PTA4/ LLWU_P3	NMI_b/ EZP_CS_b	TSI0_CH5	PTA4/ LLWU_P3		FTM0_CH1				NMI_b	EZP_CS_b
55	M8	PTA5	DISABLED		PTA5	USB_CLKIN	FTM0_CH2	RMII0_RXER/ MII0_RXER	CMP2_OUT	I2S0_TX_ BCLK	JTAG_TRST_ b	
56	E7	VDD	VDD	VDD								
57	G7	VSS	VSS	VSS								
58	J7	PTA6	DISABLED		PTA6		FTM0_CH3		CLKOUT		TRACE_ CLKOUT	
59	J8	PTA7	ADC0_SE10	ADC0_SE10	PTA7		FTM0_CH4		FB_AD18		TRACE_D3	
60	K8	PTA8	ADC0_SE11	ADC0_SE11	PTA8		FTM1_CH0		FB_AD17	FTM1_QD_ PHA	TRACE_D2	
61	L8	PTA9	DISABLED		PTA9		FTM1_CH1	MII0_RXD3	FB_AD16	FTM1_QD_ PHB	TRACE_D1	



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144	144	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
LQFP	MAP BGA											
84	G11	PTB3	LCD_P3/ ADC0_SE13/ TSI0_CH8	LCD_P3/ ADC0_SE13/ TSI0_CH8	PTB3	I2C0_SDA	UARTO_CTS_ b/ UARTO_COL	ENET0_1588_ TMR1		FTM0_FLT0	LCD_P3	
							b					
85	G10	PTB4	LCD_P4/ ADC1_SE10	LCD_P4/ ADC1_SE10	PTB4			ENET0_1588_ TMR2		FTM1_FLT0	LCD_P4	
86	G9	PTB5	LCD_P5/ ADC1_SE11	LCD_P5/ ADC1_SE11	PTB5			ENET0_1588_ TMR3		FTM2_FLT0	LCD_P5	
87	F12	PTB6	LCD_P6/ ADC1_SE12	LCD_P6/ ADC1_SE12	PTB6						LCD_P6	
88	F11	PTB7	LCD_P7/ ADC1_SE13	LCD_P7/ ADC1_SE13	PTB7						LCD_P7	
89	F10	PTB8	LCD_P8	LCD_P8	PTB8		UART3_RTS_ b				LCD_P8	
90	F9	PTB9	LCD_P9	LCD_P9	PTB9	SPI1_PCS1	UART3_CTS_ b				LCD_P9	
91	E12	PTB10	LCD_P10/ ADC1_SE14	LCD_P10/ ADC1_SE14	PTB10	SPI1_PCS0	UART3_RX			FTM0_FLT1	LCD_P10	
92	E11	PTB11	LCD_P11/ ADC1_SE15	LCD_P11/ ADC1_SE15	PTB11	SPI1_SCK	UART3_TX			FTM0_FLT2	LCD_P11	
93	H7	VSS	VSS	VSS								
94	F5	VDD	VDD	VDD								
95	E10	PTB16	LCD_P12/ TSI0_CH9	LCD_P12/ TSI0_CH9	PTB16	SPI1_SOUT	UART0_RX			EWM_IN	LCD_P12	
96	E9	PTB17	LCD_P13/ TSI0_CH10	LCD_P13/ TSI0_CH10	PTB17	SPI1_SIN	UART0_TX			EWM_OUT_b	LCD_P13	
97	D12	PTB18	LCD_P14/ TSI0_CH11	LCD_P14/ TSI0_CH11	PTB18		FTM2_CH0	I2S0_TX_ BCLK		FTM2_QD_ PHA	LCD_P14	
98	D11	PTB19	LCD_P15/ TSI0_CH12	LCD_P15/ TSI0_CH12	PTB19		FTM2_CH1	I2S0_TX_FS		FTM2_QD_ PHB	LCD_P15	
99	D10	PTB20	LCD_P16	LCD_P16	PTB20	SPI2_PCS0				CMP0_OUT	LCD_P16	
100	D9	PTB21	LCD_P17	LCD_P17	PTB21	SPI2_SCK				CMP1_OUT	LCD_P17	
101	C12	PTB22	LCD_P18	LCD_P18	PTB22	SPI2_SOUT				CMP2_OUT	LCD_P18	
102	C11	PTB23	LCD_P19	LCD_P19	PTB23	SPI2_SIN	SPI0_PCS5				LCD_P19	
103	B12	PTC0	LCD_P20/ ADC0_SE14/ TSI0_CH13	LCD_P20/ ADC0_SE14/ TSI0_CH13	PTC0	SPI0_PCS4	PDB0_EXTRG			I2S0_TXD1	LCD_P20	
104	B11	PTC1/ LLWU_P6	LCD_P21/ ADC0_SE15/ TSI0_CH14	LCD_P21/ ADC0_SE15/ TSI0_CH14	PTC1/ LLWU_P6	SPI0_PCS3	UART1_RTS_ b	FTM0_CH0		I2S0_TXD0	LCD_P21	
105	A12	PTC2	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	LCD_P22/ ADC0_SE4b/ CMP1_IN0/ TSI0_CH15	PTC2	SPI0_PCS2	UART1_CTS_ b	FTM0_CH1		12S0_TX_FS	LCD_P22	
106	A11	PTC3/ LLWU_P7	LCD_P23/ CMP1_IN1	LCD_P23/ CMP1_IN1	PTC3/ LLWU_P7	SPI0_PCS1	UART1_RX	FTM0_CH2	CLKOUT	I2S0_TX_ BCLK	LCD_P23	
107	H8	VSS	VSS	VSS								

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144 LQFP	144 Map	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
	BGA											
108	C10	VLL3	VLL3	VLL3								
109	C9	VLL2	VLL2	VLL2								
110	B9	VLL1	VLL1	VLL1								
111	B10	VCAP2	VCAP2	VCAP2								
112	A10	VCAP1	VCAP1	VCAP1								
113	A9	PTC4/ LLWU_P8	LCD_P24	LCD_P24	PTC4/ LLWU_P8	SPI0_PCS0	UART1_TX	FTM0_CH3		CMP1_OUT	LCD_P24	
114	D8	PTC5/ LLWU_P9	LCD_P25	LCD_P25	PTC5/ LLWU_P9	SPI0_SCK	LPTMR0_ ALT2	12S0_RXD0		CMP0_OUT	LCD_P25	
115	C8	PTC6/ LLWU_P10	LCD_P26/ CMP0_IN0	LCD_P26/ CMP0_IN0	PTC6/ LLWU_P10	SPI0_SOUT	PDB0_EXTRG	12S0_RX_ BCLK		I2S0_MCLK	LCD_P26	
116	B8	PTC7	LCD_P27/ CMP0_IN1	LCD_P27/ CMP0_IN1	PTC7	SPI0_SIN	USB_SOF_ OUT	I2S0_RX_FS			LCD_P27	
117	A8	PTC8	LCD_P28/ ADC1_SE4b/ CMP0_IN2	LCD_P28/ ADC1_SE4b/ CMP0_IN2	PTC8			I2S0_MCLK			LCD_P28	
118	D7	PTC9	LCD_P29/ ADC1_SE5b/ CMP0_IN3	LCD_P29/ ADC1_SE5b/ CMP0_IN3	PTC9			I2S0_RX_ BCLK		FTM2_FLT0	LCD_P29	
119	C7	PTC10	LCD_P30/ ADC1_SE6b	LCD_P30/ ADC1_SE6b	PTC10	I2C1_SCL		I2S0_RX_FS			LCD_P30	
120	B7	PTC11/ LLWU_P11	LCD_P31/ ADC1_SE7b	LCD_P31/ ADC1_SE7b	PTC11/ LLWU_P11	I2C1_SDA		12S0_RXD1			LCD_P31	
121	A7	PTC12	LCD_P32	LCD_P32	PTC12		UART4_RTS_ b				LCD_P32	
122	D6	PTC13	LCD_P33	LCD_P33	PTC13		UART4_CTS_ b				LCD_P33	
123	C6	PTC14	LCD_P34	LCD_P34	PTC14		UART4_RX				LCD_P34	
124	B6	PTC15	LCD_P35	LCD_P35	PTC15		UART4_TX				LCD_P35	
125	A6	PTC16	LCD_P36	LCD_P36	PTC16		UART3_RX	ENET0_1588_ TMR0			LCD_P36	
126	D5	PTC17	LCD_P37	LCD_P37	PTC17		UART3_TX	ENET0_1588_ TMR1			LCD_P37	
127	C5	PTC18	LCD_P38	LCD_P38	PTC18		UART3_RTS_ b	ENET0_1588_ TMR2			LCD_P38	
128	B5	PTC19	LCD_P39	LCD_P39	PTC19		UART3_CTS_ b	ENET0_1588_ TMR3			LCD_P39	
129	A5	PTD0/ LLWU_P12	LCD_P40	LCD_P40	PTD0/ LLWU_P12	SPI0_PCS0	UART2_RTS_ b				LCD_P40	
130	D4	PTD1	LCD_P41/ ADC0_SE5b	LCD_P41/ ADC0_SE5b	PTD1	SPI0_SCK	UART2_CTS_ b				LCD_P41	
131	C4	PTD2/ LLWU_P13	LCD_P42	LCD_P42	PTD2/ LLWU_P13	SPI0_SOUT	UART2_RX				LCD_P42	
132	B4	PTD3	LCD_P43	LCD_P43	PTD3	SPI0_SIN	UART2_TX				LCD_P43	1
133	A4	PTD4/ LLWU_P14	LCD_P44	LCD_P44	PTD4/ LLWU_P14	SPI0_PCS1	UART0_RTS_ b	FTM0_CH4		EWM_IN	LCD_P44	



Pinout



Figure 34. K53 144 LQFP Pinout Diagram