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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkm34z256vll7

Ordering Information

Part Number [1]	Memory		ADC Channels	Maximum number of GPIOs
	Flash (KB)	SRAM (KB)		
MKM34Z256VLL7	256	32	12	72
MKM34Z256VLQ7	256	32	16	99

1. To confirm current availability of orderable part numbers, go to http://www.freescale.com and perform a part number search.

Related Resources

Type	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KM3xPB [1]
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KM34P144M75SF0RM [1]
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document: KM34P144M75SF0
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_M_0N32P [1]
Package Drawing	Package dimensions are provided in package drawings.	100-LQFP: 98ASS23308W [1] 144-LQFP: 98ASS23177W [1]

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model (All pins except RESET pin)	-4000	+4000	V	
	Electrostatic discharge voltage, human body model (RESET pin only)	-2500	+2500	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model (for corner pins)	-750	+750	V	
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
V_{PESD}	Powered ESD voltage	-6000	+6000	V	
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage when AFE is operational	2.7	3.6	V	
	Supply voltage when AFE is NOT operational	1.71	3.6	V	
V_{DDA}	Analog supply voltage	2.7	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin • V_{IN} < V_{SS}–0.3V	–5	—	mA	
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • V_{IN} < V_{SS}–0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 –3 —	 — +3	mA	
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 –25 —	 — +25	mA	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. V_{BAT} always needs to be there for the chip to be operational.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• –40 °C • 105 °C	—	6.05	15	µA	
I_{DD_VBAT}	Average current when VDD is OFF and LFSR and Tamper clocks set to 2 Hz.					7, 8

	• @ 3.0 V
	  • 25 °C
	  • –40 °C
	  • 105 °C
		—	1.42
			1.24
			8.04
				3
				2.5
				16
					µA
					µA
					µA	

1. See AFE specification for I_{DDA}.
2. 75 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FBE mode. All peripheral clocks disabled.
3. Should be reduced by 500 µA.
4. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing while (1) loop from flash.
5. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing while (1) loop from flash.
6. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. No flash accesses; some activity on DMA & RAM assumed.
7. Includes 32 kHz oscillator current and RTC operation.
8. An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBµV	
V_{RE2}	Radiated emissions voltage, band 2	50–150	16	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	1

1. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time • Slew disabled • 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V • Slew enabled • 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V	 — — — —	 8 5 27 16	 ns ns ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.[1]	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

1. Maximum T_A can be exceeded ***only if*** the user ensures that T_J does ***not*** exceed maximum T_J . The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	144 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient	62	55	°C/W	1

Table continues on the next page...

3.1 Core modules

3.1.1 Single Wire Debug (SWD)

Table 12. SWD switching characteristics at 2.7 V (2.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	
Inputs, t_{SUI}	Data setup time	5	ns	1
inputs, t_{HI}	Data hold time	0	ns	1
after clock edge, t_{DVO}	Data valid Time	32	ns	1
t_{HO}	Data Valid Hold	0	ns	1

1. Input transition assumed = 1 ns. Output transition assumed = 50 pF.

Table 13. Switching characteristics at 1.7 V (1.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, t_{SUI}	Data setup time	4.7	ns	1
inputs, t_{HI}	Data hold time	0	ns	1
after clock edge, t_{DVO}	Data valid Time	49.4	ns	2
t_{HO}	Data Valid Hold	0	ns	1

1. Input transition assumed = 1 ns. Output transition assumed = 50 pF.
2. Frequency of SWD clock (18 MHz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

3.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V-3.6 V)

Case 1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad PTB7, PTE3, and PTK4).

Table 14. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	
Inputs, t_{SUI}	Data setup time	5	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at the XBAR out ports).

Table 15. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, t_{SUI}	Data setup time	36	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

AFE switching characteristics at (1.7 V-3.6 V)

Case 1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad PTB7, PTE3, and PTK4).

Table 16. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	13	MHz	
Inputs, t_{SUI}	Data setup time	30	ns	1
inputs, t_{HI}	Data hold time	5	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at XBAR out ports).

Table 17. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.5	MHz	
Inputs, t_{SUI}	Data setup time	36	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

3.2 Clock modules

Table 19. Oscillator DC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)					
	• 1 MHz resonator	—	6.6	—	kΩ	
	• 2 MHz resonator	—	3.3	—	kΩ	
	• 4 MHz resonator	—	0	—	kΩ	
	• 8 MHz resonator	—	0	—	kΩ	
	• 16 MHz resonator	—	0	—	kΩ	
	• 20 MHz resonator	—	0	—	kΩ	
	• 32 MHz resonator	—	0	—	kΩ	
V_{pp}[5]	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — low-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, low-power mode (HGO=0)	—	0.6	—	V	
	Peak-to-peak amplitude of oscillation (oscillator mode) — high-frequency, high-gain mode (HGO=1)	—	V_{DD}	—	V	

1. V_{DD}=3.3 V, Temperature =25 °C
2. See crystal or resonator manufacturer's recommendation
3. C_x and C_y can be provided by using either integrated capacitors or external components.
4. When low-power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other device.

3.2.2.2 Oscillator frequency specifications

Table 20. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	1	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	

Table continues on the next page...

Table 21. 32kHz oscillator absolute maximum ratings (continued)

Num	Symbol	Description	Min.	Max.	Unit
3	V_{XTAL}	XTAL Input Voltage	–0.3	3.6	V
4	T_A	Operating Temperature Range (Packaged)	–40	135	°C
5	T_J	Operating Temperature Range (Junction)	–40	135	°C
6	T_{stg}	Storage Temperature Range	–65	150	°C

3.2.3.2 32 kHz oscillator DC electrical specifications

Table 22. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.3.3 32 kHz oscillator frequency specifications

Table 23. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

3.3.1.3 Flash high voltage current behaviors

Table 26. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.3.1.4 Reliability specifications

Table 27. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 105 °C.

3.4 Analog

3.4.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

3.4.1.1 16-bit ADC operating conditions

Table 28. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4

Table continues on the next page...

Table 29. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• <12-bit modes			–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • 12-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

3. The ADC supply current depends on the ADC conversion clock speed, conversion rate and ADC_CFG1[ADLPC] (low power). For lowest power operation, ADC_CFG1[ADLPC] must be set, the ADC_CFG2[ADHSC] bit must be clear with 1 MHz ADC conversion clock speed.
4. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
5. ADC conversion clock < 16 MHz, Max hardware averaging (AVGE = %1, AVGS = %11)
6. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
7. Input data is 1 kHz sine wave. ADC conversion clock < 12 MHz.
8. ADC conversion clock < 3 MHz

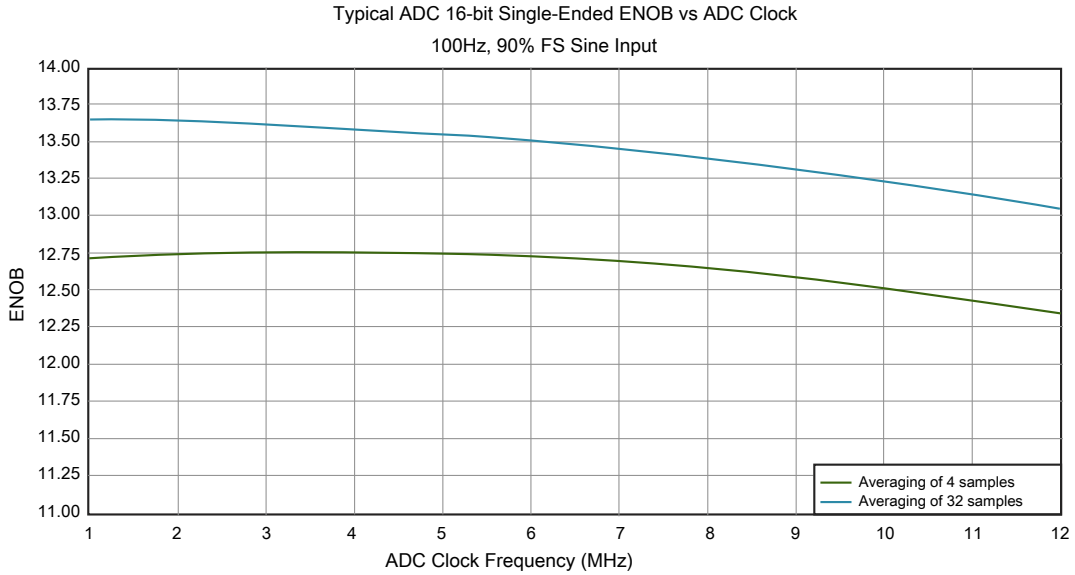


Figure 4. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

3.4.2 CMP and 6-bit DAC electrical specifications

Table 30. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	µA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V

Table continues on the next page...

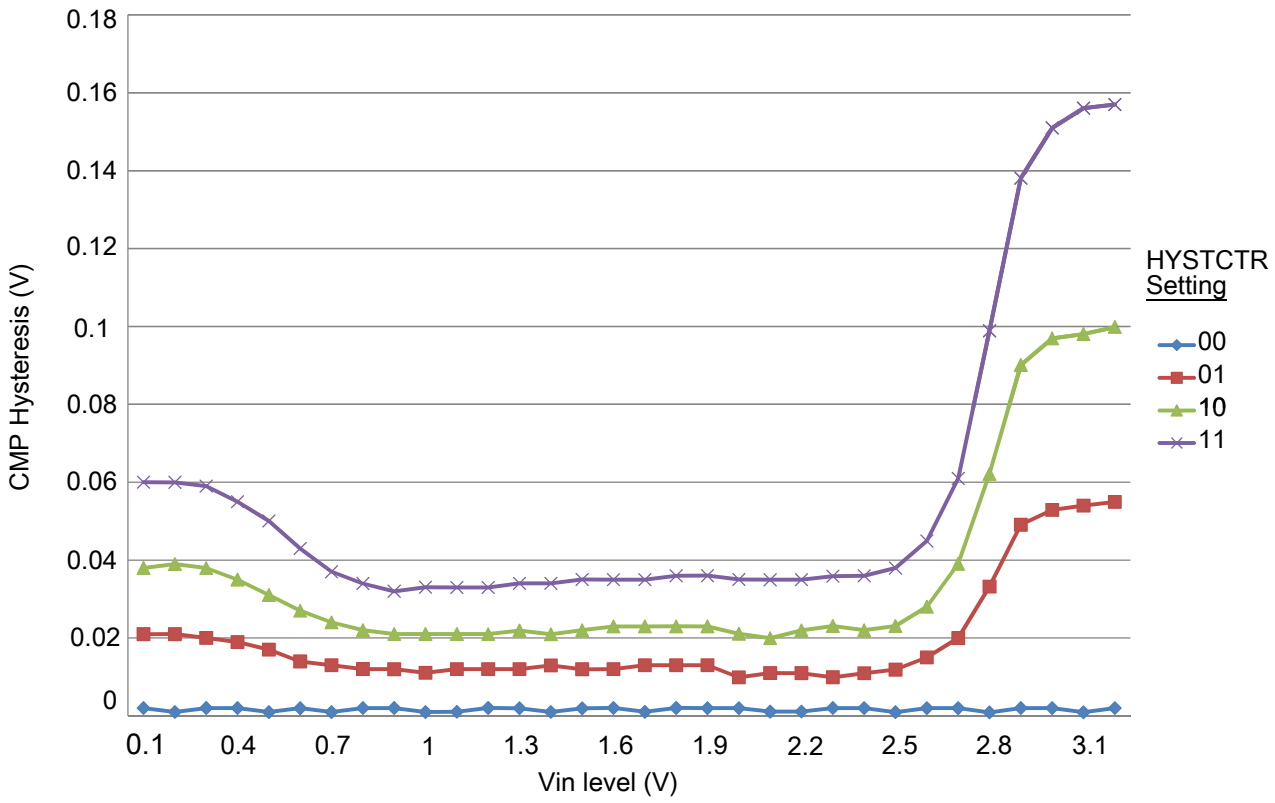


Figure 6. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.4.3 Voltage reference electrical specifications

Table 31. 1.2 VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	2.7 [1]	3.6	V	
T_A	Temperature	–40	105	°C	
C_L	Output load capacitance	100		nF	2, 3

1. AFE is enabled.
2. C_L must be connected between VREFH and VREFL.
3. The load capacitance should not exceed ±25% of the nominal specified C_L value over the operating temperature range of the device.

Table 32. VREF full-range operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with factory trim at nominal V_{DDA} and temperature = 25 °C	1.1915	1.195	1.2027	V	

Table continues on the next page...

Table 32. VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with — factory trim	1.1584	—	1.2376	V	
VREFH	Voltage reference output — user trim	1.178	—	1.202	V	
VREFL	Voltage reference output	0.38	0.4	0.42	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift when ICOMP = 0 across full temperature range	—	18	—	ppm/ºC	
	Temperature drift when ICOMP = 1 across full temperature range	—	6	—	ppm/°C	1
	Temperature drift when ICOMP = 1 across -40 ºC to 70 ºC	—	5	—	ppm/°C	1, 2
	Temperature drift when ICOMP = 1 across 0 ºC to 50 ºC	—	3	—	ppm/°C	1, 2
Ac	Aging coefficient	—	—	400	uV/yr	
I_{bg}	Bandgap only current	—	—	80	µA	2
I_{lp}	Low-power buffer current	—	—	0.19	mA	2
I_{hp}	High-power buffer current	—	—	0.5	mA	2
I_{LOAD}	VREF buffer current	–2	—	2	mA	3, 4
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	— —	 200	 —	µV	2, 5
T_{stup}	Buffer startup time	—	—	20	ms	
V_{vdrift}	Voltage drift (VREFHmax -VREFHmin across the full voltage range)	—	0.5	—	mV	2

1. ICOMP=1 is recommended to get best temperature drift. CHOPEN bit = 1 is also recommended.
2. See the chip's Reference Manual for the appropriate settings of VREF Status and Control register.
3. 2 mA I_{LOAD} is only achievable for above 2.7 V V_{DDA} condition.
4. See the chip's Reference Manual for the appropriate settings of SIM Miscellaneous Control Register.
5. Load regulation voltage is the difference between VREFH voltage with no load vs. voltage with defined load.

NOTE

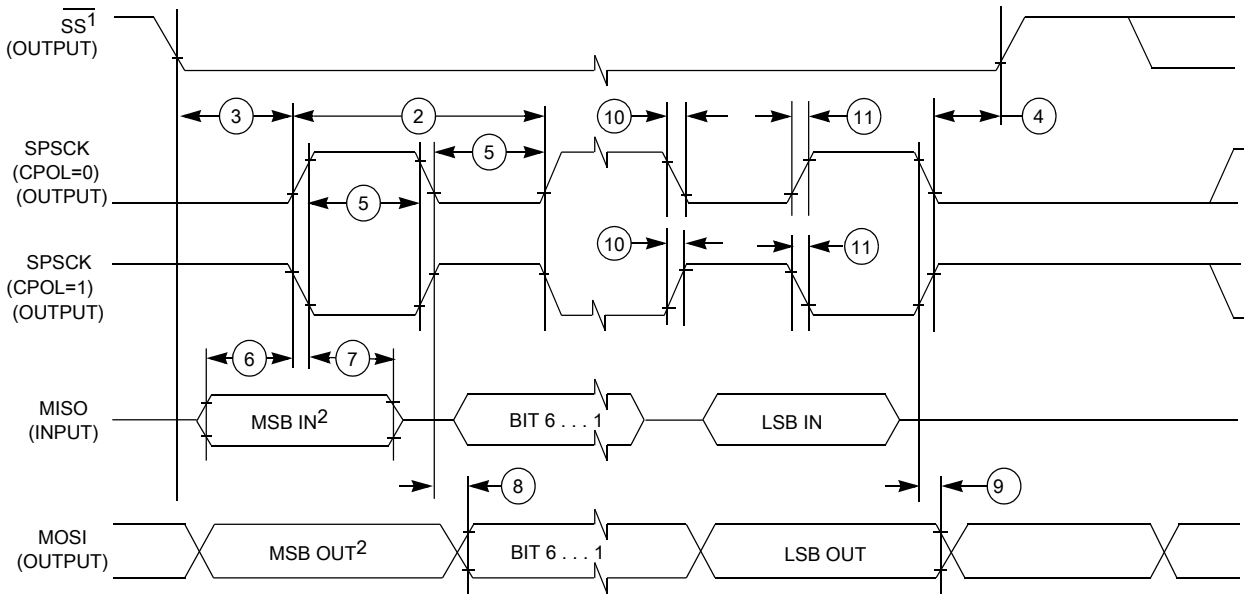
Temperature drift per degree is ((VREFHmax-VREFHmin)/ (temperature range)/VREFHmin) in ppm/ºC

3.4.4 AFE electrical specifications

Table 36. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 7. SPI master mode timing (CPHA = 0)

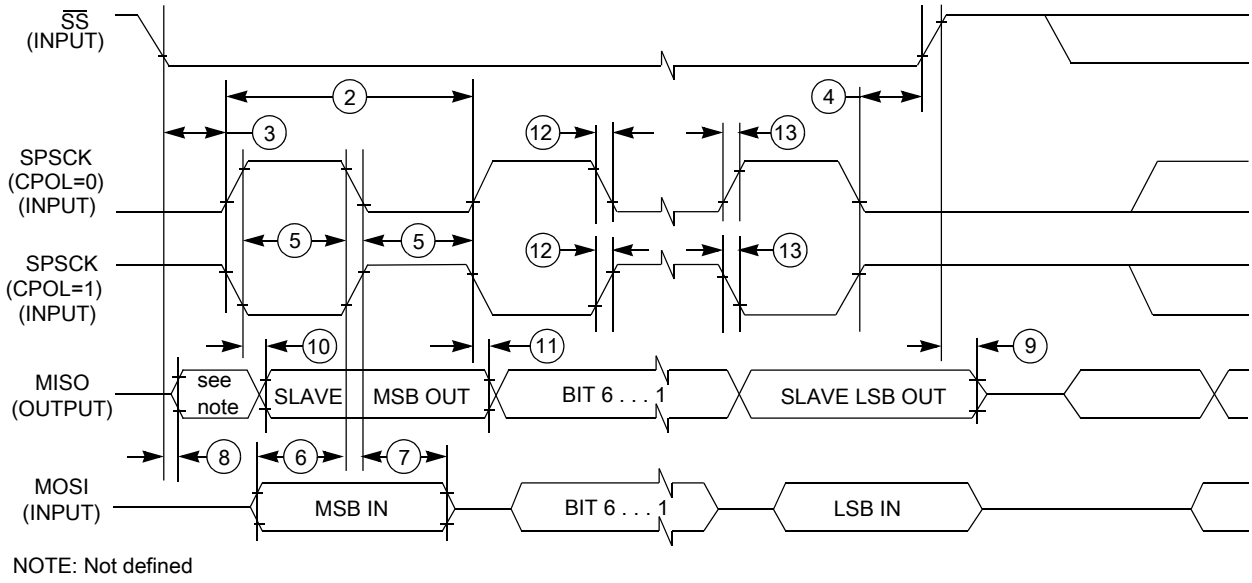


Figure 10. SPI slave mode timing (CPHA = 1)

3.7 Human-Machine Interfaces (HMI)

3.7.1 LCD electrical characteristics

Table 39. LCD electricals

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{Frame}	LCD frame frequency					
	• GCR[FFR]=0	23.3	—	73.1	Hz	
	• GCR[FFR]=1	46.6	—	146.2	Hz	
C_{LCD}	LCD charge pump capacitance — nominal value	—	100	—	nF	
C_{BYLCD}	LCD bypass capacitance — nominal value	—	100	—	nF	1
C_{Glass}	LCD glass capacitance	—	2000	8000	pF	2
V_{IREG}	V_{IREG}				V	3
	• RVTRIM=0000	—	0.91	—		
	• RVTRIM=1000	—	0.92	—		
	• RVTRIM=0100	—	0.93	—		
	• RVTRIM=1100	—	0.94	—		
	• RVTRIM=0010	—	0.96	—		
	• RVTRIM=1010	—	0.97	—		
	• RVTRIM=0110	—	0.98	—		

Table continues on the next page...

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
144-pin LQFP	98ASS23177W

5 Pinout

5.1 KM3x_256 Signal multiplexing and pin assignments

144 QFP	100 QFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	—	NC	NC								
2	—	NC	NC								
3	—	PTI5	Disabled	LCD_P45	PTI5						LCD_P45
4	1	PTA0/ LLWU_P16	Disabled	LCD_P23	PTA0/ LLWU_P16						LCD_P23
5	2	PTA1	Disabled	LCD_P24	PTA1						LCD_P24
6	—	PTI6	Disabled	LCD_P46	PTI6	UART2_RX					LCD_P46
7	—	PTI7	Disabled	LCD_P47	PTI7	UART2_TX					LCD_P47
8	3	PTA2	Disabled	LCD_P25	PTA2						LCD_P25
9	4	PTA3	Disabled	LCD_P26	PTA3						LCD_P26
10	5	PTA4/ LLWU_P15	NMI_b	LCD_P27	PTA4/ LLWU_P15					LCD_P27	NMI_b
11	6	PTA5	Disabled	LCD_P28	PTA5	CMP0_OUT					LCD_P28
12	7	PTA6/ LLWU_P14	Disabled	LCD_P29	PTA6/ LLWU_P14	XBAR_IN0					LCD_P29
13	8	PTA7	Disabled	LCD_P30	PTA7	XBAR_OUT0					LCD_P30
14	—	PTJ0	Disabled	LCD_P48	PTJ0	I2C1_SDA					LCD_P48
15	—	PTJ1	Disabled	LCD_P49	PTJ1	I2C1_SCL					LCD_P49

144 QFP	100 QFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
51	39	AFE_ SDADP2/ CMP1_IN2	AFE_ SDADP2/ CMP1_IN2	AFE_ SDADP2/ CMP1_IN2							
52	40	AFE_ SDADM2/ CMP1_IN3	AFE_ SDADM2/ CMP1_IN3	AFE_ SDADM2/ CMP1_IN3							
53	41	VREF	VREF	VREF							
54	42	AFE_ SDADP3/ CMP1_IN4	AFE_ SDADP3/ CMP1_IN4	AFE_ SDADP3/ CMP1_IN4							
55	43	AFE_ SDADM3/ CMP1_IN5	AFE_ SDADM3/ CMP1_IN5	AFE_ SDADM3/ CMP1_IN5							
56	—	NC	NC								
57	—	NC	NC								
58	44	PTC5/ LLWU_P12	Disabled	ADC0_SE0/ CMP2_IN0	PTC5/ LLWU_P12	UART0_RTS_ b					
59	45	PTC6	Disabled	ADC0_SE1/ CMP2_IN1	PTC6	UART0_CTS_ b	QTMR0_ TMR1	PDB0_EXTRG			
60	46	PTC7	Disabled	ADC0_SE2/ CMP2_IN2	PTC7	UART0_TX	XBAR_OUT2				
61	47	PTD0/ LLWU_P11	Disabled	CMP0_IN0	PTD0/ LLWU_P11	UART0_RX	XBAR_IN2				
62	—	PTJ3	Disabled		PTJ3	LPUART0_ RTS_b	CMP2_OUT				
63	—	PTJ4	Disabled		PTJ4	LPUART0_ CTS_b					
64	48	PTD1	Disabled		PTD1	UART1_TX	SPI0_PCS0	XBAR_OUT3	QTMR0_ TMR3		
65	49	PTD2/ LLWU_P10	Disabled	CMP0_IN1	PTD2/ LLWU_P10	UART1_RX	SPI0_SCK	XBAR_IN3			
66	—	PTJ5	Disabled		PTJ5	LPUART0_TX					
67	—	PTJ6/ LLWU_P18	Disabled		PTJ6/ LLWU_P18	LPUART0_RX					
68	—	PTJ7	Disabled		PTJ7						
69	50	PTD3	Disabled		PTD3	UART1_CTS_ b	SPI0_MOSI				
70	—	PTK0	Disabled	ADC0_SE12	PTK0						
71	—	NC	NC								
72	—	NC	NC								
73	—	NC	NC								
74	—	NC	NC								
75	—	PTK1	Disabled	ADC0_SE13	PTK1						
76	51	PTD4/ LLWU_P9	Disabled	ADC0_SE3	PTD4/ LLWU_P9	UART1_RTS_ b	SPI0_MISO				

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

- MKM34Z256VLL7
- MKM34Z256VLQ7

7 Part identification

7.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

7.2 Format

Part numbers for this device have the following format:

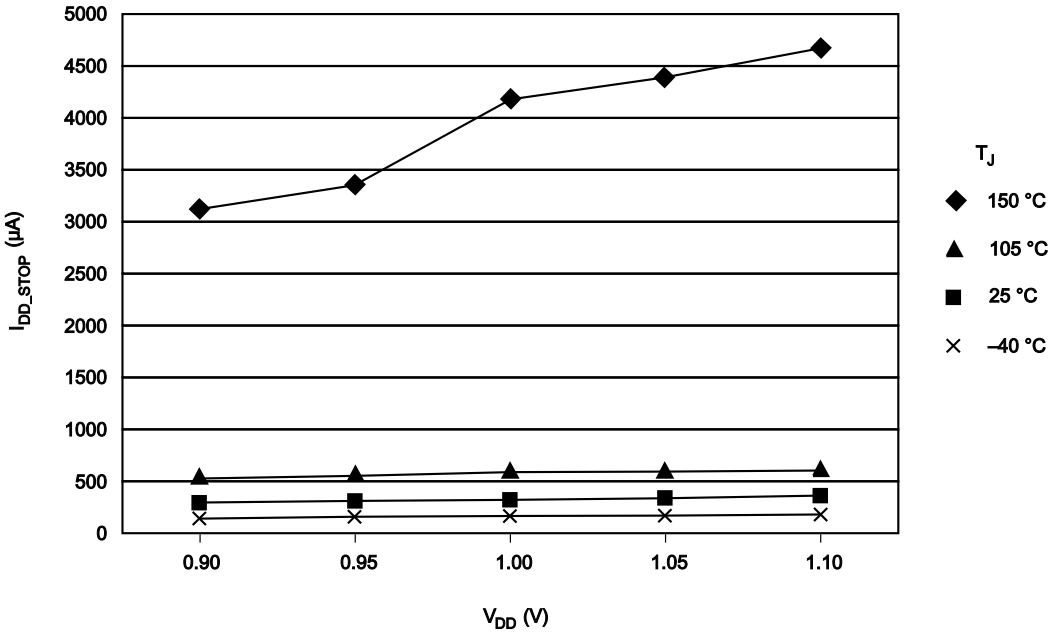
Q KM## A FFF R T PP CC N

7.3 Fields

Following table lists the possible values for each field in the part number (not all combinations are valid):

Field	Description	Values
Q	Qualification status	• M = Fully qualified, general market flow • P = Pre-qualification
KM##	Kinetis family	• KM34
A	Key attribute	• Z = Cortex®-M0+
FFF	Program flash memory size	• 256 = 256 KB
R	Silicon revision	• (Blank) = Main • A = Revision after main
T	Temperature range (°C)	• V = –40 to 105
PP	Package identifier	• LL = 100 LQFP (14 mm x 14 mm) • LQ = 144 LQFP (20 mm × 20 mm)

Table continues on the next page...



8.9 Typical value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DD}	3.3 V supply voltage	3.3	V

9 Revision History

The following table provides a revision history for this document.

Table 40. Revision History

Rev. No.	Date	Substantial Changes
2	05/2015	Initial public release