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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	72
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 12x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkm34z256vll7r

Timers

- Quad Timer (QTMR)
- Periodic Interrupt Timer (PIT)
- Low Power Timer (LPTMR)
- Programmable Delay Block (PDB)
- Independent Real Time Clock (iRTC)

Human-machine interface

- Up to 4×60 (8×56, 6×58) segment LCD controller operating in all low-power modes
- General purpose input/output (GPIO)

Security and integrity modules

- Memory Mapped Cryptographic Acceleration Unit (MMCAU) for AES encryption
- Random Number Generator (RNGA), complying with NIST: SP800-90
- Programmable Cyclic Redundancy Check (PCRC)
- 80-bit unique identification number per chip

The following figure shows the functional modules in the chip.

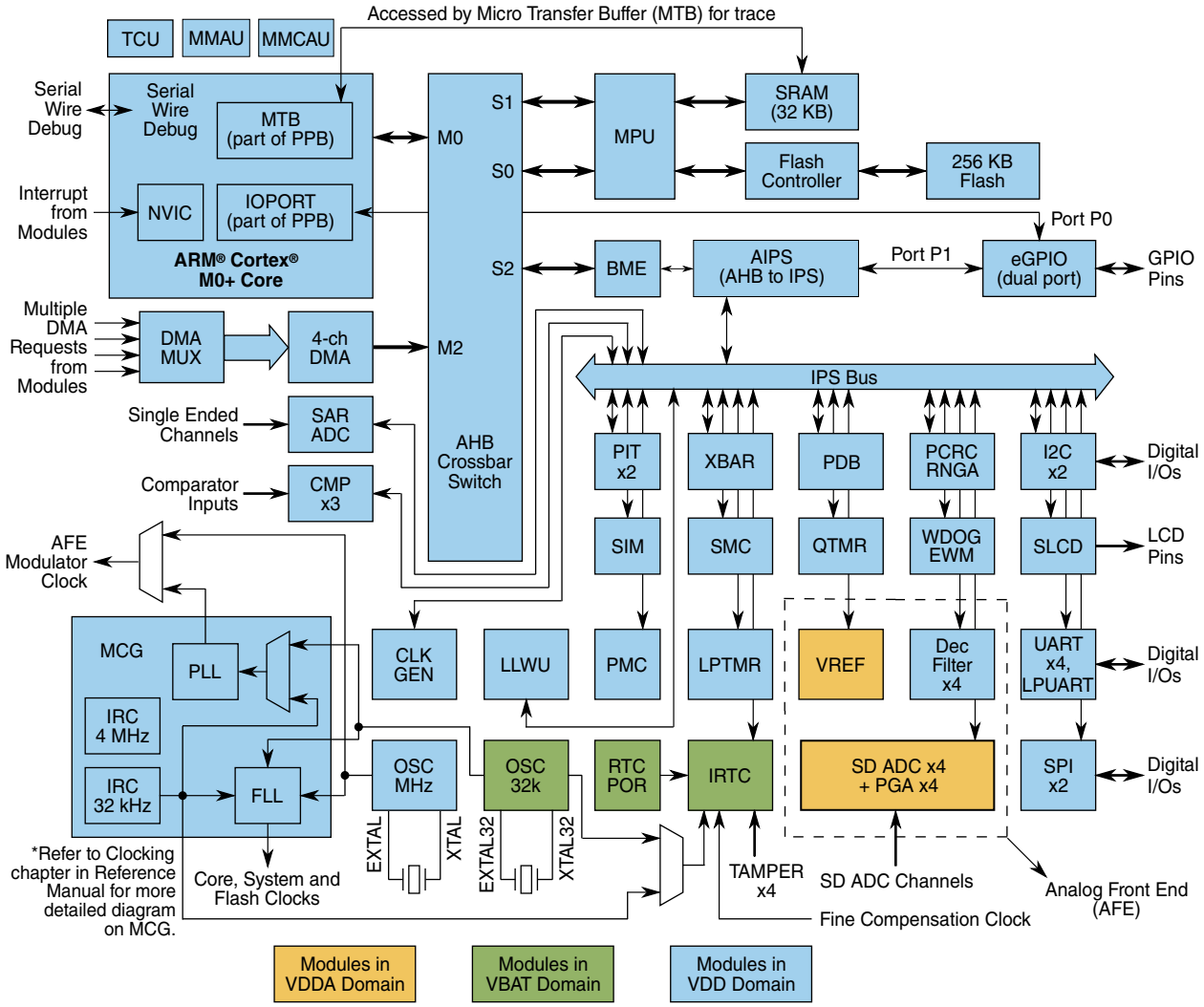


Figure 1. Functional block diagram

1.4 Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit
V_{DD}	Digital supply voltage	–0.3	3.6	V
V_{DIO}	Digital input voltage (except $\overline{RESET}$, EXTAL, and XTAL)	–0.3	V_{DD} + 0.3	V
$V_{DTamper}$	Tamper input voltage	–0.3	V_{BAT} + 0.3	V
V_{AIO}	Analog[1], $\overline{RESET}$, EXTAL, and XTAL input voltage	–0.3	V_{DD} + 0.3	V
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	–25	25	mA
V_{DDA}	Analog supply voltage	V_{DD} – 0.3	V_{DD} + 0.3	V
V_{BAT}	RTC battery supply voltage	–0.3	3.6	V

1. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2 General

2.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

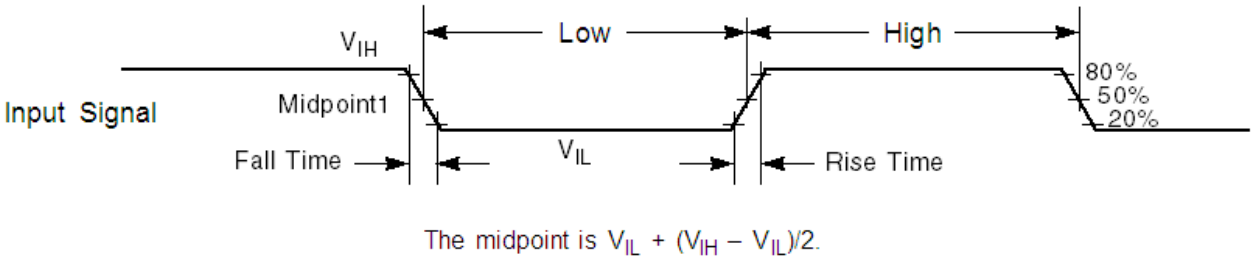


Figure 2. Input signal measurement reference

2.2 Nonswitching electrical specifications

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• –40 °C • 105 °C	—	6.05	15	µA	
I_{DD_VBAT}	Average current when VDD is OFF and LFSR and Tamper clocks set to 2 Hz.					7, 8

	• @ 3.0 V
	  • 25 °C
	  • –40 °C
	  • 105 °C
		—	1.42
			1.24
			8.04
				3
				2.5
				16
					µA
					µA
					µA	

1. See AFE specification for I_{DDA}.
2. 75 MHz core and system clock, 25 MHz bus clock, and 25 MHz flash clock. MCG configured for FBE mode. All peripheral clocks disabled.
3. Should be reduced by 500 µA.
4. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. Code executing while (1) loop from flash.
5. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks enabled but peripherals are not in active operation. Code executing while (1) loop from flash.
6. 2 MHz core/system clock, and 1 MHz bus/flash clock. MCG configured for BLPE mode. All peripheral clocks disabled. No flash accesses; some activity on DMA & RAM assumed.
7. Includes 32 kHz oscillator current and RTC operation.
8. An external power switch for VBAT should be present on board to have better battery life and keep VBAT pin powered in all conditions. There is no internal power switch in RTC.

2.2.6 EMC radiated emissions operating behaviors

Table 7. EMC radiated emissions operating behaviors

Symbol	Description	Frequency band (MHz)	Typ.	Unit	Notes
V_{RE1}	Radiated emissions voltage, band 1	0.15–50	14	dBµV	
V_{RE2}	Radiated emissions voltage, band 2	50–150	16	dBµV	
V_{RE3}	Radiated emissions voltage, band 3	150–500	12	dBµV	
V_{RE4}	Radiated emissions voltage, band 4	500–1000	5	dBµV	
V_{RE_IEC}	IEC level	0.15–1000	M	—	1

1. V_{DD} = 3.3 V, T_A = 25 °C, f_{OSC} = 10 MHz (crystal), f_{SYS} = 75 MHz, f_{BUS} = 25 MHz

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for “EMC design.”

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time • Slew disabled • 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V • Slew enabled • 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V	 — — — —	 8 5 27 16	 ns ns ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.[1]	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

1. Maximum T_A can be exceeded ***only if*** the user ensures that T_J does ***not*** exceed maximum T_J . The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	144 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient	62	55	°C/W	1

Table continues on the next page...

3.1 Core modules

3.1.1 Single Wire Debug (SWD)

Table 12. SWD switching characteristics at 2.7 V (2.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	20	MHz	
Inputs, t_{SUI}	Data setup time	5	ns	1
inputs, t_{HI}	Data hold time	0	ns	1
after clock edge, t_{DVO}	Data valid Time	32	ns	1
t_{HO}	Data Valid Hold	0	ns	1

1. Input transition assumed = 1 ns. Output transition assumed = 50 pF.

Table 13. Switching characteristics at 1.7 V (1.7-3.6 V)

Symbol	Description	Value	Unit	Notes
SWD CLK	Frequency of SWD operation	18	MHz	
Inputs, t_{SUI}	Data setup time	4.7	ns	1
inputs, t_{HI}	Data hold time	0	ns	1
after clock edge, t_{DVO}	Data valid Time	49.4	ns	2
t_{HO}	Data Valid Hold	0	ns	1

1. Input transition assumed = 1 ns. Output transition assumed = 50 pF.
2. Frequency of SWD clock (18 MHz) is applicable only in case the input setup time of the device outside is not more than 6.15 ns, else the frequency of SWD clock would need to be lowered.

3.1.2 Analog Front End (AFE)

AFE switching characteristics at (2.7 V-3.6 V)

Case 1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad PTB7, PTE3, and PTK4).

Table 14. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	10	MHz	
Inputs, t_{SUI}	Data setup time	5	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

3.2.2.1 Oscillator DC electrical specifications

Table 19. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 1 MHz	—	200	—	µA	
	• 4 MHz	—	200	—	µA	
	• 8 MHz (RANGE=01)	—	300	—	µA	
	• 16 MHz	—	950	—	µA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high-gain mode (HGO=1)					1
	• 32 kHz	—	25	—	µA	
	• 1 MHz	—	300	—	µA	
	• 4 MHz	—	400	—	µA	
	• 8 MHz (RANGE=01)	—	500	—	µA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
	Capacitance of EXTAL • Die level (100 LQFP) • Package level (100 LQFP)	247 0.495	—	—	ff pF	
	Capacitance of XTAL • Die level (100 LQFP) • Package level (100 LQFP)	265 0.495	—	—	ff pF	
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	

Table continues on the next page...

Table 21. 32kHz oscillator absolute maximum ratings (continued)

Num	Symbol	Description	Min.	Max.	Unit
3	V_{XTAL}	XTAL Input Voltage	–0.3	3.6	V
4	T_A	Operating Temperature Range (Packaged)	–40	135	°C
5	T_J	Operating Temperature Range (Junction)	–40	135	°C
6	T_{stg}	Storage Temperature Range	–65	150	°C

3.2.3.2 32 kHz oscillator DC electrical specifications

Table 22. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

3.2.3.3 32 kHz oscillator frequency specifications

Table 23. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

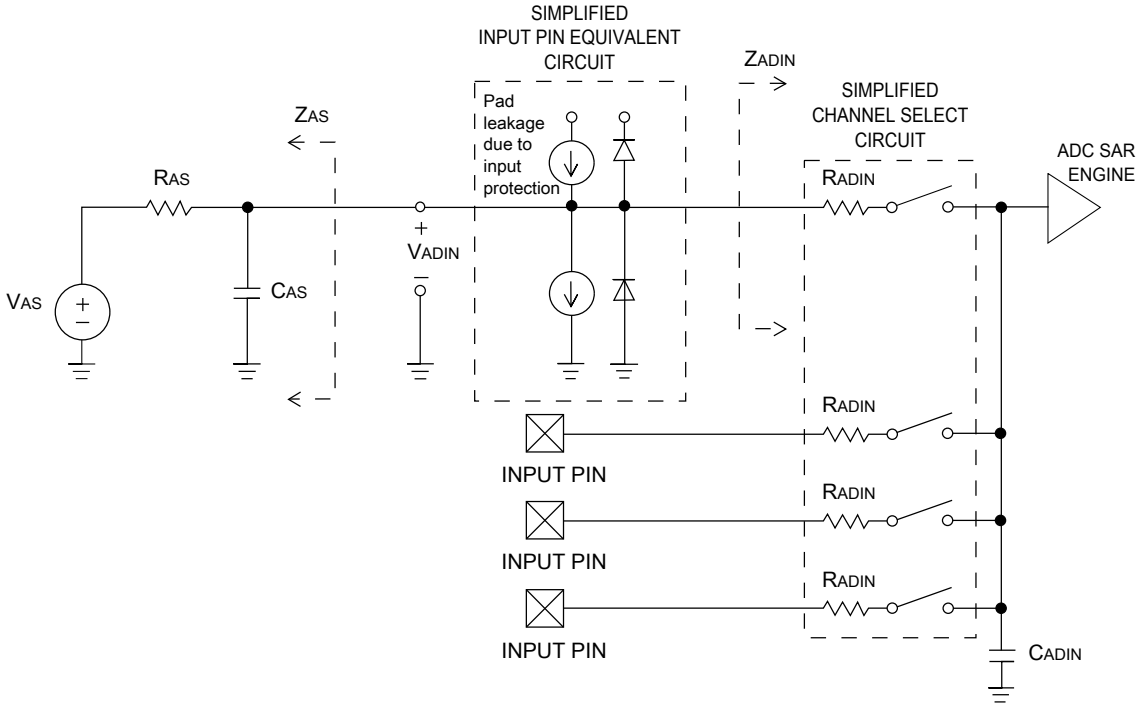


Figure 3. ADC input impedance equivalency diagram

3.4.1.2 16-bit ADC electrical characteristics

Table 29. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = $1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to +0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

Table 32. VREF full-range operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
VREFH	Voltage reference output with — factory trim	1.1584	—	1.2376	V	
VREFH	Voltage reference output — user trim	1.178	—	1.202	V	
VREFL	Voltage reference output	0.38	0.4	0.42	V	
V_{step}	Voltage reference trim step	—	0.5	—	mV	
V_{tdrift}	Temperature drift when ICOMP = 0 across full temperature range	—	18	—	ppm/ºC	
	Temperature drift when ICOMP = 1 across full temperature range	—	6	—	ppm/°C	1
	Temperature drift when ICOMP = 1 across -40 ºC to 70 ºC	—	5	—	ppm/°C	1, 2
	Temperature drift when ICOMP = 1 across 0 ºC to 50 ºC	—	3	—	ppm/°C	1, 2
Ac	Aging coefficient	—	—	400	uV/yr	
I_{bg}	Bandgap only current	—	—	80	µA	2
I_{lp}	Low-power buffer current	—	—	0.19	mA	2
I_{hp}	High-power buffer current	—	—	0.5	mA	2
I_{LOAD}	VREF buffer current	–2	—	2	mA	3, 4
ΔV_{LOAD}	Load regulation • current = ± 1.0 mA	— —	 200	 —	µV	2, 5
T_{stup}	Buffer startup time	—	—	20	ms	
V_{vdrift}	Voltage drift (VREFHmax -VREFHmin across the full voltage range)	—	0.5	—	mV	2

1. ICOMP=1 is recommended to get best temperature drift. CHOPEN bit = 1 is also recommended.
2. See the chip's Reference Manual for the appropriate settings of VREF Status and Control register.
3. 2 mA I_{LOAD} is only achievable for above 2.7 V V_{DDA} condition.
4. See the chip's Reference Manual for the appropriate settings of SIM Miscellaneous Control Register.
5. Load regulation voltage is the difference between VREFH voltage with no load vs. voltage with defined load.

NOTE

Temperature drift per degree is ((VREFHmax-VREFHmin)/ (temperature range)/VREFHmin) in ppm/ºC

3.4.4 AFE electrical specifications

3.4.4.1 ΣΔ ADC + PGA specifications

Table 33. ΣΔ ADC + PGA specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Differential input range	Gain = 1 (PGA ON/OFF)[2]		± 500		mV	
		Gain = 2		± 250		mV	
		Gain = 4		± 125		mV	
		Gain = 8		± 62		mV	
		Gain = 16		± 31		mV	
		Gain = 32		± 15		mV	
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50 Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50 Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50 Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50 Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended) • f_{IN}=50 Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended) • f_{IN}=50 Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	90 88 82 76 70 64	92 90 86 82 78 74		dB	
		Low-Power Mode • f_{IN}=50 Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50 Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50 Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50 Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended)	82 76 70 64 58	82 78 74 70 66		dB	

Table continues on the next page...

Table 33. ΣΔ ADC + PGA specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
		• f_{IN}=50 Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended) • f_{IN}=50 Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	52	62			
SINAD	Signal-to-Noise + Distortion Ratio	Normal Mode • f_{IN}=50 Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		78		dB	
		Low-Power Mode • f_{IN}=50 Hz; gain=01, common mode=0V, V_{pp}=500mV (differential ended)		74		dB	
CMMR	Common Mode Rejection Ratio	• f_{IN}=50 Hz; gain=01, common mode=0V, Vid=100 mV • f_{IN}=50 Hz; gain=32, common mode=0V, V_{id}=100 mV		70 70		dB	
E_{offset}	Offset Error	Gain=01, V_{pp}=1000 mV (full range diff.)			± 5	mV	
$\Delta Offset_{Temp}$	Offset Temperature Drift [3]	Gain=01, V_{pp}=1000 mV (full range diff.)			± 25	ppm/°C	
$\Delta Gain_{Temp}$	Gain Temperature Drift - Gain error caused by temperature drifts [4]	• Gain=01, V_{pp}=500 mV (differential ended) • Gain=32, V_{pp}=15 mV (differential ended)			± 75	ppm/°C	
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3 V ± 100 mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk (with the input of the affected channel grounded)	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_PGA}	Current consumption by PGA (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768 MHz, OSR= 256)			2.6 0	mA	5
I_{DDA_ADC}	Current Consumption by ADC (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768 MHz, OSR= 256)			1.4 0.5	mA	

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. The full-scale input range in single-ended mode is 0.5V_{pp}.

Table 34. ΣΔ ADC standalone specifications (continued)

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
$PSRR_{AC}$	AC Power Supply Rejection Ratio	Gain=01, VCC = 3 V ± 100 mV, f_{IN} = 50 Hz		60		dB	
XT	Crosstalk	Gain=01, V_{id} = 500 mV, f_{IN} = 50 Hz			-100	dB	
f_{MCLK}	Modulator Clock Frequency Range	Normal Mode Low-Power Mode	0.03 0.03		6.5 1.6	MHz	
I_{DDA_ADC}	Current Consumption by ADC (each channel)	Normal Mode (f_{MCLK} = 6.144 MHz, OSR= 2048) Low-Power Mode (f_{MCLK} = 0.768 MHz, OSR= 256)			1.4 0.5	mA	

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25°C, f_{MCLK} = 6.144 MHz, OSR = 2048 for Normal mode and f_{MCLK} = 768 kHz, OSR = 256 for Low-Power Mode unless otherwise stated. Typical values are for reference only and are not tested in production.
2. Represent combined gain temperature drift of the SD ADC, and Internal 1.2 VREF blocks.
3. Represent combined offset temperature drift of the SD ADC, and Internal 1.2 VREF blocks; Defined by shorting both differential inputs to ground.

3.4.4.3 External modulator interface

The external modulator interface on this device comprises of a Clock signal and 1-bit data signal. Depending on the modulator device being used the interface works as follows:

- Clock supplied to external modulator which drives data on rising edge and the KM device captures it on falling edge or next rising edge.
- Clock and data are supplied by external modulator and KM device can sample it on falling edge or next rising edge.

Depending on control bit in AFE, the sampling edge is changed.

3.5 Timers

See General switching specifications.

3.6 Communication interfaces

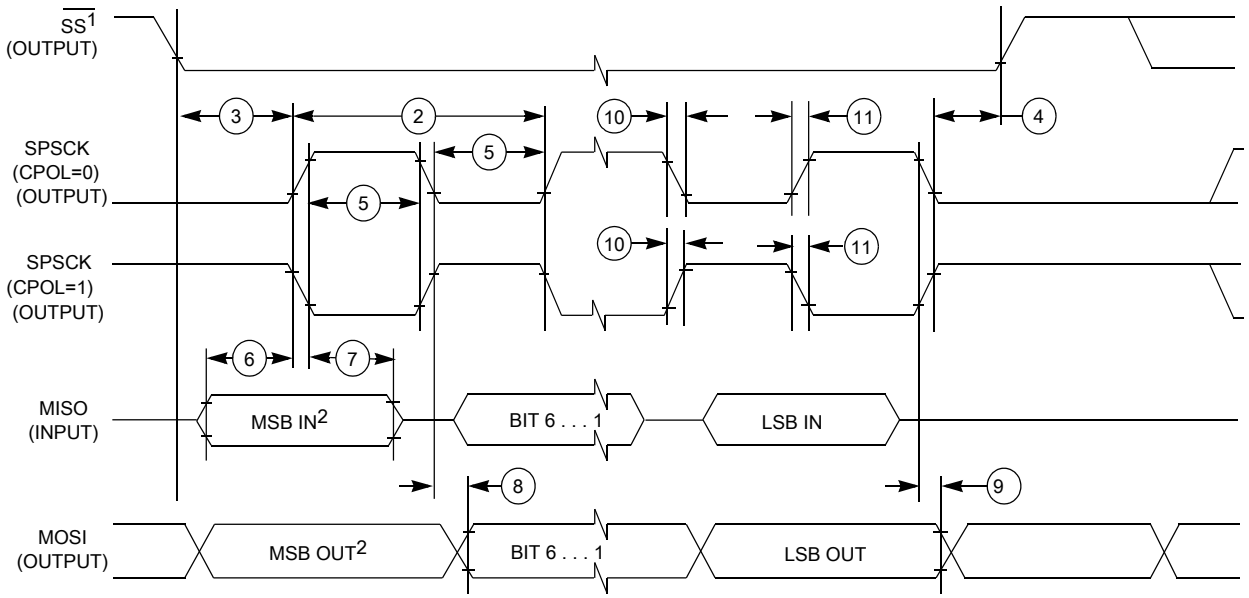
3.6.1 I2C switching specifications

See General switching specifications.

Table 36. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 7. SPI master mode timing (CPHA = 0)

Table 39. LCD electricals (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• RVTRIM=1110	—	0.99	—		
	• RVTRIM=0001	—	1.01	—		
	• RVTRIM=1001	—	1.02	—		
	• RVTRIM=0101	—	1.03	—		
	• RVTRIM=1101	—	1.05	—		
	• RVTRIM=0011	—	1.06	—		
	• RVTRIM=1011	—	1.07	—		
	• RVTRIM=0111	—	1.08	—		
	• RVTRIM=1111	—	1.09	—		
Δ_{RTRIM}	V_{IREG} TRIM resolution	—	—	3.0	% V_{IREG}	
I_{VIREG}	V_{IREG} current adder — RVEN = 1	—	1	—	µA	
I_{RBIAS}	RBIAS current adder					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	10	—	µA	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	1	—	µA	
R_{RBIAS}	RBIAS resistor values					
	• LADJ = 10 or 11 — High load (LCD glass capacitance ≤ 8000 pF)	—	0.28	—	MΩ	
	• LADJ = 00 or 01 — Low load (LCD glass capacitance ≤ 2000 pF)	—	2.98	—	MΩ	
VLL1	VLL1 voltage	—	—	V_{IREG}	V	4
VLL2	VLL2 voltage	—	—	2 x V_{IREG}	V	4
VLL3	VLL3 voltage	—	—	3 x V_{IREG}	V	4
VLL1	VLL1 voltage	—	—	V_{DDA} / 3	V	5
VLL2	VLL2 voltage	—	—	V_{DDA} / 1.5	V	5
VLL3	VLL3 voltage	—	—	V_{DDA}	V	5

1. The actual value used could vary with tolerance.
2. For highest glass capacitance values, LCD_GCR[LADJ] should be configured as specified in the LCD Controller chapter within the device's reference manual.
3. V_{IREG} maximum should never be externally driven to any level other than V_{DD} - 0.15 V
4. VLL1, VLL2 and VLL3 are a function of V_{IREG} only when the regulator is enabled (GCR[RVEN]=1) and the charge pump is enabled (GCR[CPSEL]=1).
5. VLL1, VLL2 and VLL3 are a function of V_{DDA} only under either of the following conditions:
   - The charge pump is enabled (GCR[CPSEL]=1), the regulator is disabled (GCR[RVEN]=0), and VLL3 = V_{DDA} through the internal power switch (GCR[VSUPPLY]=0).
   - The resistor bias string is enabled (GCR[CPSEL]=0), the regulator is disabled (GCR[RVEN]=0), and VLL3 is connected to V_{DDA} externally (GCR[VSUPPLY]=1).

144 QFP	100 QFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
77	52	PTD5	Disabled	ADC0_SE4a	PTD5	LPTMR0_ ALT3	QTMR0_ TMR0	UART3_CTS_ b			
78	53	PTD6/ LLWU_P8	Disabled	ADC0_SE5a	PTD6/ LLWU_P8	LPTMR0_ ALT2	CMP1_OUT	UART3_RTS_ b			
79	54	PTD7/ LLWU_P7	Disabled	CMP0_IN4	PTD7/ LLWU_P7	I2C0_SCL	XBAR_IN4	UART3_RX			
80	55	PTE0	Disabled		PTE0	I2C0_SDA	XBAR_OUT4	UART3_TX	CLKOUT		
81	—	PTK2	Disabled	ADC0_SE14	PTK2	UART0_TX					
82	—	PTK3/ LLWU_P19	Disabled	ADC0_SE15	PTK3/ LLWU_P19	UART0_RX					
83	56	PTE1	RESET_b		PTE1						RESET_b
84	57	PTE2	EXTAL0	EXTAL0	PTE2	EWM_IN	XBAR_IN6	I2C1_SDA			
85	58	PTE3	XTAL0	XTAL0	PTE3	EWM_OUT_b	AFE_CLK	I2C1_SCL			
86	59	VSS	VSS	VSS							
87	60	VSSA	VSSA	VSSA							
88	61	VDDA	VDDA	VDDA							
89	62	VDD	VDD	VDD							
90	63	PTE4	Disabled		PTE4	LPTMR0_ ALT1	UART2_CTS_ b	EWM_IN			
91	64	PTE5/ LLWU_P6	Disabled		PTE5/ LLWU_P6	QTMR0_ TMR3	UART2_RTS_ b	EWM_OUT_b			
92	65	PTE6/ LLWU_P5	SWD_DIO	CMP0_IN2	PTE6/ LLWU_P5	XBAR_IN5	UART2_RX		I2C0_SCL		SWD_DIO
93	66	PTE7	SWD_CLK	ADC0_SE6a	PTE7	XBAR_OUT5	UART2_TX		I2C0_SDA		SWD_CLK
94	67	PTF0/ LLWU_P4	Disabled	ADC0_SE7a/ CMP2_IN3	PTF0/ LLWU_P4	RTC_CLKOUT	QTMR0_ TMR2	CMP0_OUT			
95	68	PTF1	Disabled	LCD_P0/ ADC0_SE8/ CMP2_IN4	PTF1	QTMR0_ TMR0	XBAR_OUT6				LCD_P0
96	69	PTF2	Disabled	LCD_P1/ ADC0_SE9/ CMP2_IN5	PTF2	CMP1_OUT	RTC_CLKOUT				LCD_P1
97	—	PTK4	Disabled	LCD_P51	PTK4	XBAR_IN9	AFE_CLK				LCD_P51
98	—	PTK5	Disabled		PTK5	UART1_RX					
99	—	PTK6	Disabled		PTK6	UART1_TX					
100	70	PTF3/ LLWU_P20	Disabled	LCD_P2	PTF3/ LLWU_P20	SPI1_PCS0	LPTMR0_ ALT2	UART0_RX			LCD_P2
101	71	PTF4	Disabled	LCD_P3	PTF4	SPI1_SCK	LPTMR0_ ALT1	UART0_TX			LCD_P3
102	72	PTF5	Disabled	LCD_P4	PTF5	SPI1_MISO	I2C1_SCL				LCD_P4
103	73	PTF6/ LLWU_P3	Disabled	LCD_P5	PTF6/ LLWU_P3	SPI1_MOSI	I2C1_SDA				LCD_P5
104	74	PTF7	Disabled	LCD_P6	PTF7	QTMR0_ TMR2	CLKOUT	CMP2_OUT			LCD_P6

144 QFP	100 QFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
105	—	PTK7	Disabled	LCD_P52	PTK7	I2C0_SCL	XBAR_OUT9				LCD_P52
106	—	PTL0	Disabled	LCD_P53	PTL0	I2C0_SDA					LCD_P53
107	—	NC	NC								
108	—	NC	NC								
109	—	NC	NC								
110	75	PTG0	Disabled	LCD_P7	PTG0	QTMR0_ TMR1	LPTMR0_ ALT3				LCD_P7
111	76	PTG1/ LLWU_P2	Disabled	LCD_P8/ ADC0_SE10	PTG1/ LLWU_P2		LPTMR0_ ALT1				LCD_P8
112	77	PTG2/ LLWU_P1	Disabled	LCD_P9/ ADC0_SE11	PTG2/ LLWU_P1	SPI0_PCS0					LCD_P9
113	78	PTG3	Disabled	LCD_P10	PTG3	SPI0_SCK	I2C0_SCL				LCD_P10
114	79	PTG4	Disabled	LCD_P11	PTG4	SPI0_MOSI	I2C0_SDA				LCD_P11
115	80	PTG5	Disabled	LCD_P12	PTG5	SPI0_MISO	LPTMR0_ ALT2				LCD_P12
116	81	PTG6/ LLWU_P0	Disabled	LCD_P13	PTG6/ LLWU_P0		LPTMR0_ ALT3				LCD_P13
117	82	PTG7	Disabled	LCD_P14	PTG7						LCD_P14
118	83	PTH0	Disabled	LCD_P15	PTH0	LPUART0_ CTS_b					LCD_P15
119	84	PTH1	Disabled	LCD_P16	PTH1	LPUART0_ RTS_b					LCD_P16
120	85	PTH2	Disabled	LCD_P17	PTH2	LPUART0_RX					LCD_P17
121	86	PTH3	Disabled	LCD_P18	PTH3	LPUART0_TX					LCD_P18
122	87	PTH4	Disabled	LCD_P19	PTH4						LCD_P19
123	88	PTH5	Disabled	LCD_P20	PTH5						LCD_P20
124	89	PTH6	Disabled		PTH6	UART1_CTS_ b	SPI1_PCS0	XBAR_IN7			
125	90	PTH7	Disabled		PTH7	UART1_RTS_ b	SPI1_SCK	XBAR_OUT7			
126	91	PTI0/ LLWU_P21	Disabled	CMP0_IN5	PTI0/ LLWU_P21	UART1_RX	XBAR_IN8	SPI1_MISO	SPI1_MOSI		
127	92	PTI1 (This pin is true open drain pad. External pull-up resistor should be added.)	Disabled		PTI1	UART1_TX	XBAR_OUT8	SPI1_MOSI	SPI1_MISO		
128	—	PTL1	Disabled	LCD_P54	PTL1	XBAR_IN10					LCD_P54
129	—	PTL2	Disabled	LCD_P55	PTL2	XBAR_OUT10					LCD_P55
130	93	PTI2/ LLWU_P22	Disabled	LCD_P21	PTI2/ LLWU_P22	LPUART0_RX					LCD_P21
131	94	PTI3	Disabled	LCD_P22	PTI3	LPUART0_TX	CMP2_OUT				LCD_P22
132	95	VSS	VSS	VSS							

8.2.1 Example

This is an example of an operating behavior:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

8.3 Definition: Attribute

An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

8.3.1 Example

This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

8.4 Definition: Rating

A *rating* is a minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:

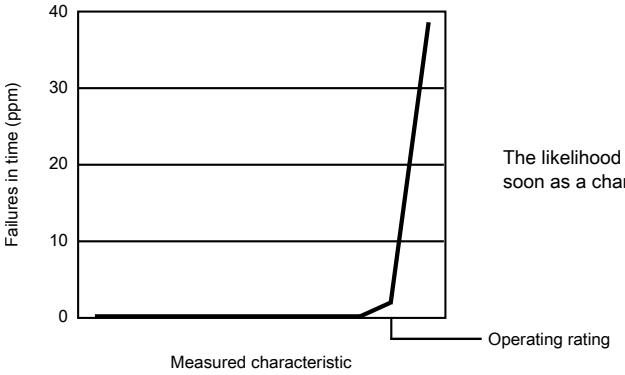
- *Operating ratings* apply during operation of the chip.
- *Handling ratings* apply when the chip is not powered.

8.4.1 Example

This is an example of an operating rating:

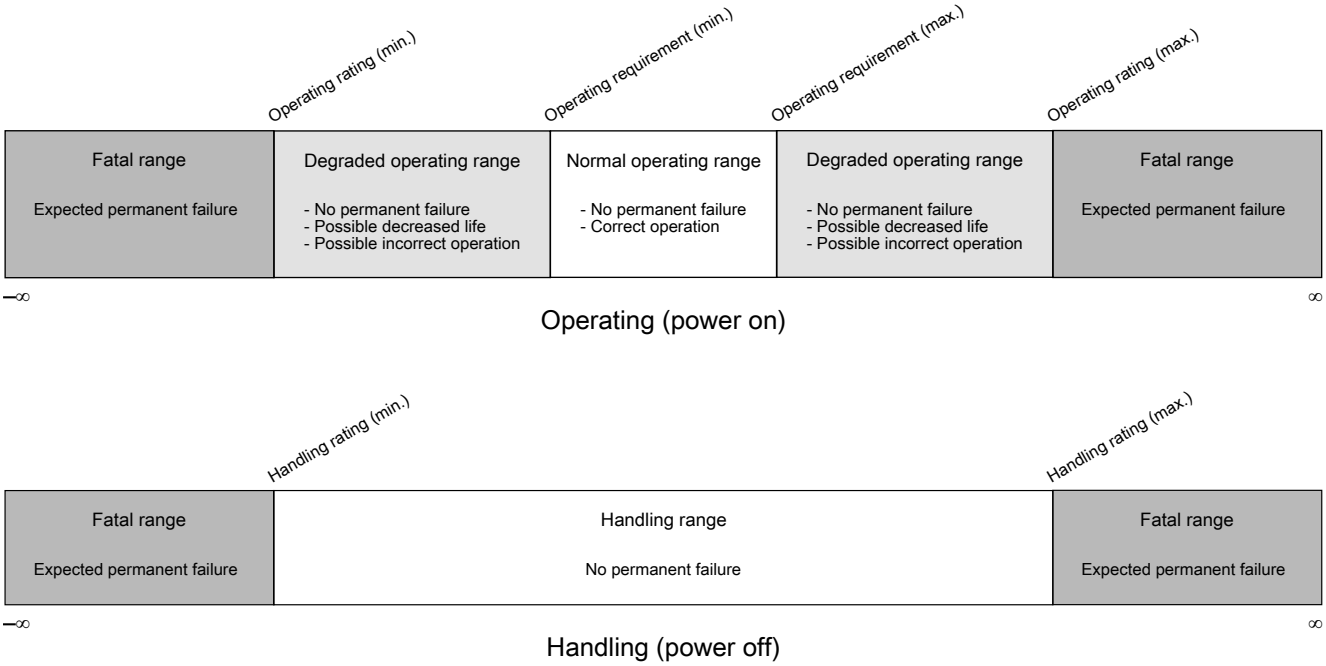
Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

8.5 Result of exceeding a rating



The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.

8.6 Relationship between ratings and operating requirements



8.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.

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