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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	75MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	DMA, LCD, WDT
Number of I/O	99
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x16b, 4x24b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkm34z256vlq7

Timers

- Quad Timer (QTMR)
- Periodic Interrupt Timer (PIT)
- Low Power Timer (LPTMR)
- Programmable Delay Block (PDB)
- Independent Real Time Clock (iRTC)

Human-machine interface

- Up to 4×60 (8×56, 6×58) segment LCD controller operating in all low-power modes
- General purpose input/output (GPIO)

Security and integrity modules

- Memory Mapped Cryptographic Acceleration Unit (MMCAU) for AES encryption
- Random Number Generator (RNGA), complying with NIST: SP800-90
- Programmable Cyclic Redundancy Check (PCRC)
- 80-bit unique identification number per chip

The following figure shows the functional modules in the chip.

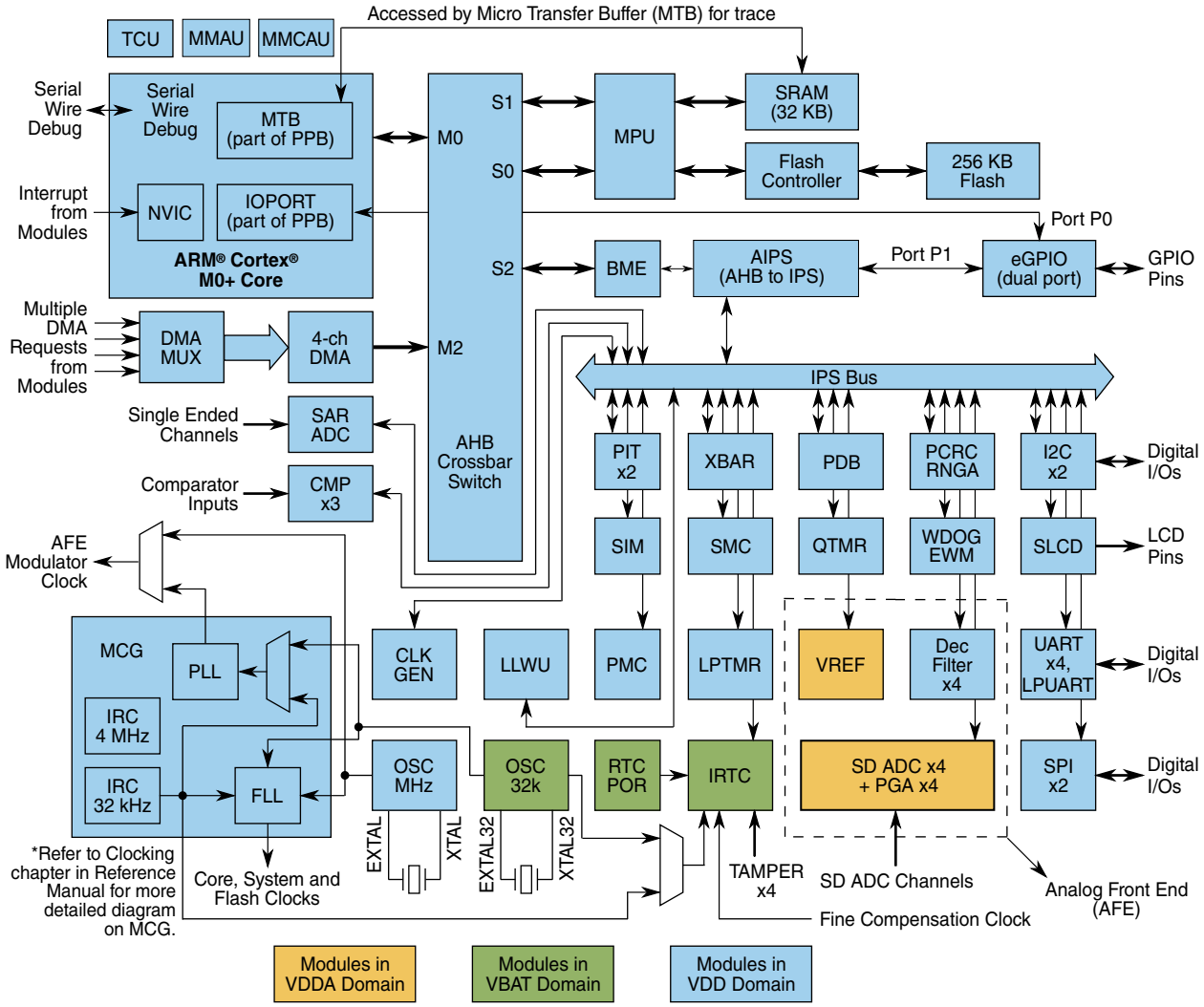


Figure 1. Functional block diagram

1 Ratings

1.1 Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.
2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.2 Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

1.3 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model (All pins except RESET pin)	-4000	+4000	V	
	Electrostatic discharge voltage, human body model (RESET pin only)	-2500	+2500	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model (for corner pins)	-750	+750	V	
V_{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
V_{PESD}	Powered ESD voltage	-6000	+6000	V	
I_{LAT}	Latch-up current at ambient temperature of 105°C	-100	+100	mA	

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.

2.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage when AFE is operational	2.7	3.6	V	
	Supply voltage when AFE is NOT operational	1.71	3.6	V	
V_{DDA}	Analog supply voltage	2.7	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	1
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin • V_{IN} < V_{SS}–0.3V	–5	—	mA	
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • V_{IN} < V_{SS}–0.3V (Negative current injection) • V_{IN} > V_{DD}+0.3V (Positive current injection)	 –3 —	 — +3	mA	
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 –25 —	 — +25	mA	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. V_{BAT} always needs to be there for the chip to be operational.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.

2.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	

Table continues on the next page...

Table 2. V_{DD} supply LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising threshold is the sum of falling threshold and hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

2.2.3 Voltage and current operating behaviors

Table 4. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V_{OH}	Output high voltage — low-drive strength				
	• 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OH} = 5 mA	V_{DD} – 0.5	—	V	
	• 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OH} = 2.5 mA	V_{DD} – 0.5	—	V	
I_{OHT}	Output high current total for all ports	—	100	mA	

Table continues on the next page...

Table 4. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{OL}	Output low voltage — low-drive strength • 2.7 V ≤ V_{DD} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DD} ≤ 2.7 V, I_{OL} = 2.5 mA	 — —	 0.5 0.5	 V V	
I_{OLT}	Output low current total for all ports	—	100	mA	
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	µA	
R_{PU}	Internal pull-up resistors	30	60	kΩ	1
R_{PD}	Internal pull-down resistors	30	60	kΩ	2

1. Measured at V_{input} = V_{SS}.
2. Measured at V_{input} = V_{DD}.

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR}, and VLLSx→RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 75 MHz
- Bus clock = 25 MHz
- Flash clock = 25 MHz
- Temperature: –40 °C, 25 °C, and 105 °C
- V_{DD}: 1.71 V, 3.3 V, and 3.6 V

Table 5. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.71 V to execute the first instruction across the operating temperature range of the chip.	563		659	µs	1
	• VLLS0 → RUN	—	370	382	µs	
	• VLLS1 → RUN	—	370	382	µs	
	• VLLS2 → RUN	—	270	275	µs	
	• VLLS3 → RUN	—	270	275	µs	
	• VLPS → RUN	—	5	6	µs	
	• STOP → RUN	—	5	6	µs	

Table 6. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• –40 °C • 105 °C	— —	456 1000	1000 —	µA µA	
I_{DD_VLPW}	Very-low-power wait mode current at 3.0 V — all peripheral clocks disabled • 25 °C • –40 °C • 105 °C	— — —	112 114 226	350 330 800	µA µA µA	6
I_{DD_STOP}	Stop mode current at 3.0 V • 25 °C • –40 °C • 105 °C	— — —	404 386 569	730 700 800	µA µA µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • 25 °C • –40 °C • 105 °C	— — —	6.05 2.63 145	46 44 700	µA µA µA	
I_{DD_VLLS3}	Very low-leakage stop mode 3 current at 3.0 V • 25 °C • –40 °C • 105 °C	— — —	2.49 1.97 20.1	3.5 3.3 85	µA µA µA	
I_{DD_VLLS2}	Very low-leakage stop mode 2 current at 3.0 V • 25 °C • –40 °C • 105 °C	— — —	2.31 1.94 14.5	2.6 2.5 59.5	µA µA µA	
I_{DD_VLLS1}	Very low-leakage stop mode 1 current at 3.0 V • 25 °C • –40 °C • 105 °C	— — —	1.16 0.937 10.7	1.7 1.6 38.8	µA µA µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit disabled • 25 °C • –40 °C • 105 °C	— — —	0.22 0.068 7.72	0.67 0.64 38	µA µA µA	
I_{DD_VLLS0}	Very low-leakage stop mode 0 current at 3.0 V with POR detect circuit enabled • 25 °C • –40 °C • 105 °C	— — —	0.502 0.349 9.07	0.76 0.72 38.4	µA µA µA	
I_{DD_VBAT}	Average current with RTC and 32 kHz disabled at 3.0 V and VDD is OFF • 25 °C	— —	0.243 0.143	1 0.95	µA µA	

Table continues on the next page...

Table 10. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Asynchronous path	16	—	ns	
	External reset pulse width (digital glitch filter disabled)	100	—	ns	2
	Port rise and fall time • Slew disabled • 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V • Slew enabled • 1.71 ≤ V_{DD} ≤ 2.7 V • 2.7 ≤ V_{DD} ≤ 3.6 V	 — — — —	 8 5 27 16	 ns ns ns ns	

1. The greater synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.

2.4 Thermal specifications

2.4.1 Thermal operating requirements

Table 11. Thermal operating requirements

Symbol	Description	Min.	Max.[1]	Unit
T_J	Die junction temperature	–40	125	°C
T_A	Ambient temperature	–40	105	°C

1. Maximum T_A can be exceeded ***only if*** the user ensures that T_J does ***not*** exceed maximum T_J . The simplest method to determine T_J is:

   $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Board type	Symbol	Description	100 LQFP	144 LQFP	Unit	Notes
Single-layer (1s)	$R_{\theta JA}$	Thermal resistance, junction to ambient	62	55	°C/W	1

Table continues on the next page...

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at the XBAR out ports).

Table 15. AFE switching characteristics (2.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.2	MHz	
Inputs, t_{SUI}	Data setup time	36	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

AFE switching characteristics at (1.7 V-3.6 V)

Case 1: Clock is coming In and Data is also coming In (XBAR ports timed with respect to AFE clock defined at pad PTB7, PTE3, and PTK4).

Table 16. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	13	MHz	
Inputs, t_{SUI}	Data setup time	30	ns	1
inputs, t_{HI}	Data hold time	5	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

Case 2: Clock is going Out and Data is coming In (XBAR ports timed with respect to generated clock defined at XBAR out ports).

Table 17. AFE switching characteristics (1.7 V-3.6 V)

Symbol	Description	Value	Unit	Notes
AFE CLK	Frequency of operation	6.5	MHz	
Inputs, t_{SUI}	Data setup time	36	ns	1
inputs, t_{HI}	Data hold time	0	ns	1

1. Input Transition: 1 ns. Output Load: 50 pF.

3.2 Clock modules

3.2.1 MCG specifications

Table 18. MCG specifications

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
f_{ints_ft}	Internal reference frequency (slow clock) — factory trimmed at nominal V_{DD} and 25 °C		—	32.768	—	kHz	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over voltage and temperature		—	+0.5/-0.7	—	%	
Δf_{ints_t}	Total deviation of internal reference frequency (slow clock) over fixed voltage and full operating temperature range		-2	—	+2	%	
f_{ints_t}	Internal reference frequency (slow clock) — user trimmed		31.25	—	39.0625	kHz	
$\Delta_{fdco\_res\_t}$	Resolution of trimmed average DCO output frequency at fixed voltage and temperature — using SCTRIM and SCFTRIM		—	± 0.3	± 0.6	$\%f_{dco}$	
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over voltage and temperature		—	+0.5/-0.7		$\%f_{dco}$	1
Δf_{dco_t}	Total deviation of trimmed average DCO output frequency over fixed voltage and temperature range of 0–70°C		—	± 0.4	—	$\%f_{dco}$	1
f_{intf_ft}	Internal reference frequency (fast clock) — factory trimmed at nominal V_{DD} and 25°C		—	4	—	MHz	
Δf_{intf_t}	Total deviation of internal reference frequency (fast clock) over voltage and temperature — factory trimmed at nominal V_{DD} and 25°C		—	+1/-2	—	%	
f_{intf_t}	Internal reference frequency (fast clock) — user trimmed at nominal V_{DD} and 25 °C		3	—	5	MHz	
f_{loc_low}	Loss of external clock minimum frequency — RANGE = 00		(3/5) x f_{ints_t}	—	—	kHz	
f_{loc_high}	Loss of external clock minimum frequency — RANGE = 01, 10, or 11		(16/5) x f_{ints_t}	—	—	kHz	
		FLL					
f_{dco}	DCO output frequency range	Low-range (DRS=00) 640 × f_{ints_t}	20	20.97	22	MHz	2, 3
		Mid-range (DRS=01) 1280 × f_{ints_t}	40	41.94	45	MHz	
		Mid-high range (DRS=10) 1920 × f_{ints_t}	60	62.91	67	MHz	
		High-range (DRS=11) 2560 × f_{ints_t}	80	83.89	90	MHz	
$f_{dco\_t\_DMX32}$	DCO output frequency	Low-range (DRS=00) 732 × f_{ints_t}	—	23.99	—	MHz	4, 5, 6

Table continues on the next page...

3.3.1.3 Flash high voltage current behaviors

Table 26. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	2.5	6.0	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

3.3.1.4 Reliability specifications

Table 27. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
Program Flash						
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	—
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	—
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at –40 °C ≤ T_j ≤ 105 °C.

3.4 Analog

3.4.1 ADC electrical specifications

All ADC channels meet the 12-bit single-ended accuracy specifications.

3.4.1.1 16-bit ADC operating conditions

Table 28. 16-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage	Absolute	1.71	—	3.6	V	—
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-100	0	+100	mV	2
ΔV_{SSA}	Ground voltage	Delta to V_{SS} (V_{SS} – V_{SSA})	-100	0	+100	mV	2
V_{REFH}	ADC reference voltage high	Absolute	V_{DDA}	V_{DDA}	V_{DDA}	V	3
V_{REFL}	ADC reference voltage low	Absolute	V_{SSA}	V_{SSA}	V_{SSA}	V	4

Table continues on the next page...

Table 28. 16-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{ADIN}	Input voltage		V_{SSA}	—	V_{DDA}	V	—
C_{ADIN}	Input capacitance	• 16-bit mode • 8-bit / 10-bit / 12-bit modes	— —	8 4	10 5	pF	—
R_{ADIN}	Input series resistance		—	2	5	kΩ	—
R_{AS}	Analog source resistance (external)	12-bit modes f_{ADCK} < 4 MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	≤ 12-bit mode	1.0	—	18.0	MHz	6
f_{ADCK}	ADC conversion clock frequency	16-bit mode	2.0	—	12.0	MHz	6
C_{rate}	ADC conversion rate	≤ 12-bit modes No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	20.000	—	818.330	ksps	7
C_{rate}	ADC conversion rate	16-bit mode No ADC hardware averaging Continuous conversions enabled, subsequent conversion time	37.037	—	461.467	ksps	7

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. V_{REFH} is internally tied to V_{DDA}.
4. V_{REFL} is internally tied to V_{SSA}.
5. This resistance is external to MCU. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The R_{AS}/C_{AS} time constant should be kept to < 1 ns.
6. To use the maximum ADC conversion clock frequency, CFG2[ADHSC] must be set and CFG1[ADLPC] must be clear.
7. For guidelines and examples of conversion rate calculation, download the ADC calculator tool.

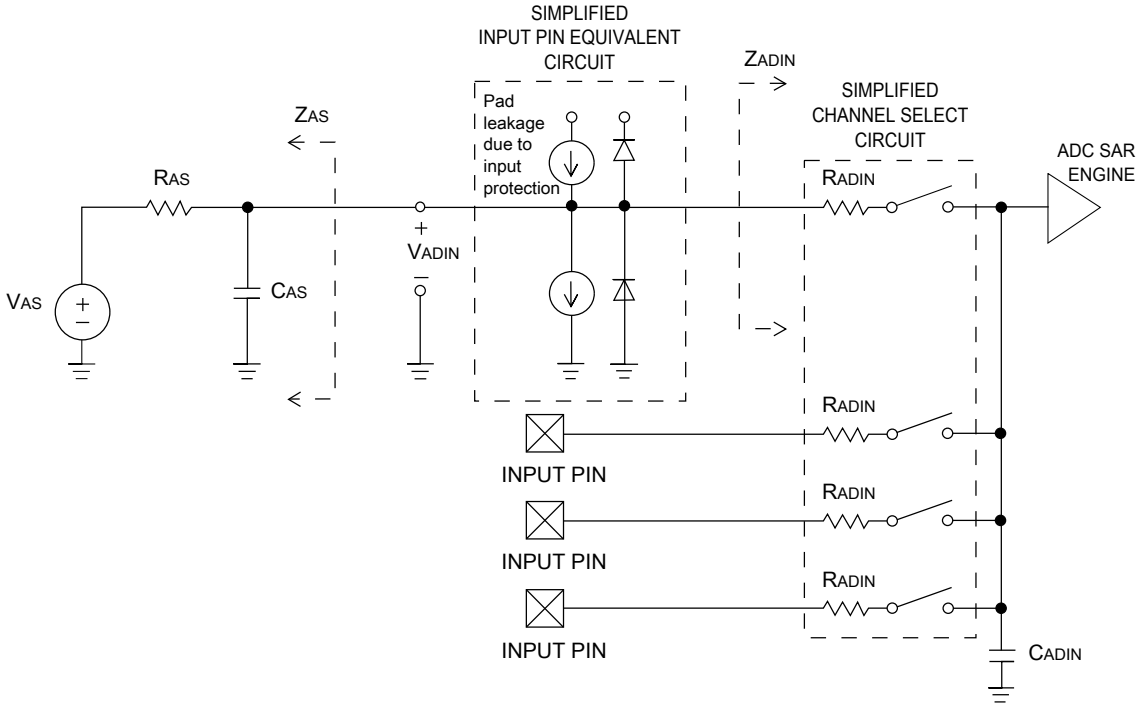


Figure 3. ADC input impedance equivalency diagram

3.4.1.2 16-bit ADC electrical characteristics

Table 29. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0 • ADLPC = 1, ADHSC = 1 • ADLPC = 0, ADHSC = 0 • ADLPC = 0, ADHSC = 1	1.2 2.4 3.0 4.4	2.4 4.0 5.2 6.2	3.9 6.1 7.3 9.5	MHz MHz MHz MHz	t_{ADACK} = $1/f_{ADACK}$
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes • <12-bit modes	— —	±4 ±1.4	±6.8 ±2.1	LSB[4]	5
DNL	Differential non-linearity	• 12-bit modes • <12-bit modes	— —	±0.7 ±0.2	–1.1 to +1.9 –0.3 to +0.5	LSB[4]	5
INL	Integral non-linearity	• 12-bit modes	— —	±1.0 ±0.5	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

Table 29. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
		• <12-bit modes			–0.7 to +0.5		
E_{FS}	Full-scale error	• 12-bit modes • <12-bit modes	— —	–4 –1.4	–5.4 –1.8	LSB[4]	V_{ADIN} = V_{DDA}[5]
E_Q	Quantization error	• 16-bit modes • 12-bit modes	— —	–1 to 0 —	— ±0.5	LSB[4]	
ENOB	Effective number of bits	16-bit single-ended mode • Avg = 32 • Avg = 4	 12.8 11.9 12.2 11.4	 14.5 13.8 13.9 13.1	 — — — —	 bits bits bits bits	6
SINAD	Signal-to-noise plus distortion	See ENOB	6.02 × ENOB + 1.76			dB	
THD	Total harmonic distortion	16-bit single-ended mode • Avg = 32	 — —	 -94 -85	 — —	dB dB	7
SFDR	Spurious free dynamic range	16-bit single-ended mode • Avg = 32	 82 78	 95 90	 — —	dB dB	7
E_{IL}	Input leakage error		I_{In} × R_{AS}			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)
	Temp sensor slope	Across the full temperature range of the device	1.55	1.62	1.69	mV/°C	8
V_{TEMP25}	Temp sensor voltage	25 °C	706	716	726	mV	8

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = V_{DDA}
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

Table 30. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{CMPOI}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}$/64

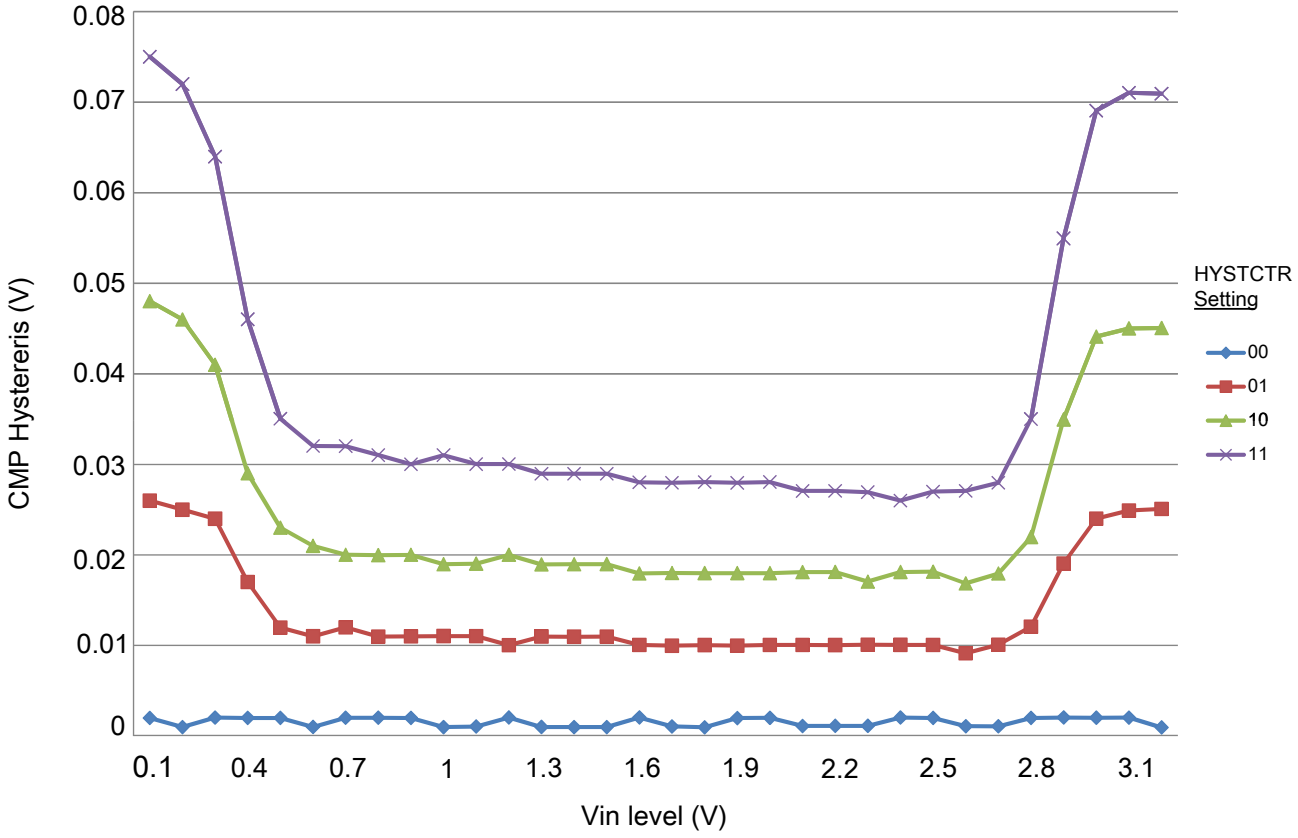


Figure 5. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

3.4.4.1 ΣΔ ADC + PGA specifications

Table 33. ΣΔ ADC + PGA specifications

Symbol	Description	Conditions	Min	Typ[1]	Max	Unit	Notes
f_{Nyq}	Input bandwidth	Normal Mode	1.5	1.5	1.5	kHz	
		Low-Power Mode	1.5	1.5	1.5		
V_{CM}	Input Common Mode Reference		0		0.8	V	
VIN_{diff}	Differential input range	Gain = 1 (PGA ON/OFF)[2]		± 500		mV	
		Gain = 2		± 250		mV	
		Gain = 4		± 125		mV	
		Gain = 8		± 62		mV	
		Gain = 16		± 31		mV	
		Gain = 32		± 15		mV	
SNR	Signal to Noise Ratio	Normal Mode • f_{IN}=50 Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50 Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50 Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50 Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended) • f_{IN}=50 Hz; gain=16, common mode=0V, V_{pp}= 62mV (differential ended) • f_{IN}=50 Hz; gain=32, common mode=0V, V_{pp}= 31mV (differential ended)	90 88 82 76 70 64	92 90 86 82 78 74		dB	
		Low-Power Mode • f_{IN}=50 Hz; gain=01, common mode=0V, V_{pp}=1000mV (full range diff.) • f_{IN}=50 Hz; gain=02, common mode=0V, V_{pp}= 500mV (differential ended) • f_{IN}=50 Hz; gain=04, common mode=0V, V_{pp}= 250mV (differential ended) • f_{IN}=50 Hz; gain=08, common mode=0V, V_{pp}= 125mV (differential ended)	82 76 70 64 58	82 78 74 70 66		dB	

Table continues on the next page...

3.6.2 UART switching specifications

See General switching specifications.

3.6.3 SPI switching specifications

The Serial Peripheral Interface (SPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes. See the SPI chapter of the chip's Reference Manual for information about the modified transfer formats used for communicating with slower peripheral devices.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all SPI pins.

Table 35. SPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$

Table 36. SPI master mode timing on slew rate enabled pads

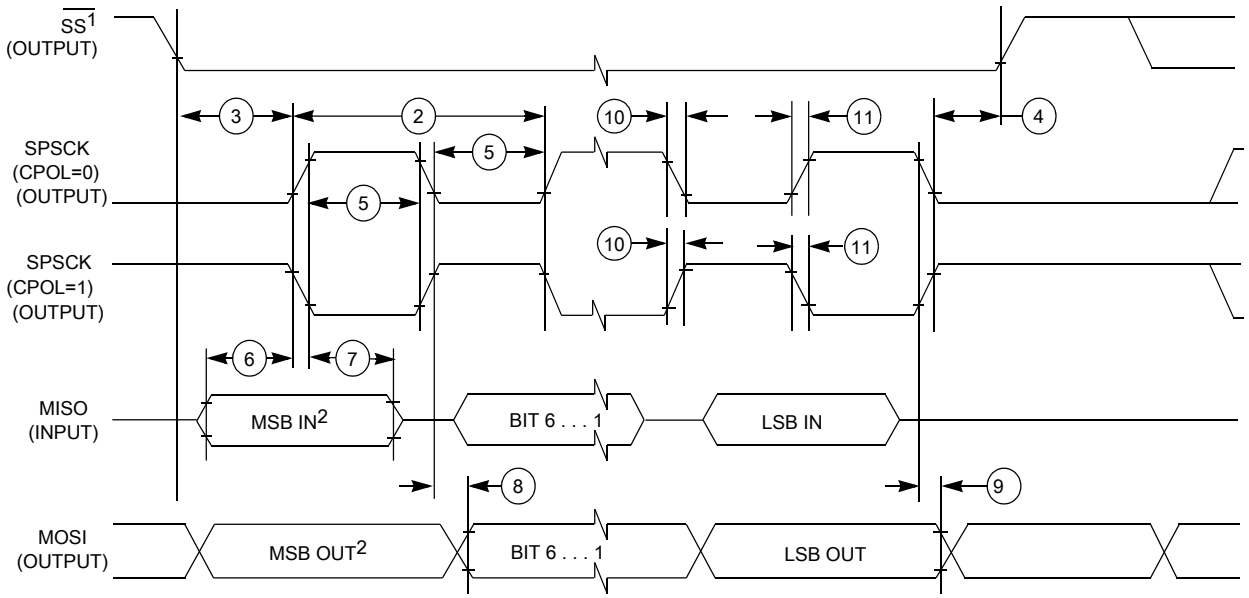
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1

Table continues on the next page...

Table 36. SPI master mode timing on slew rate enabled pads (continued)

Num.	Symbol	Description	Min.	Max.	Unit	Note
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For both SPI0 and SPI1, f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 7. SPI master mode timing (CPHA = 0)

4 Dimensions

4.1 Obtaining package dimensions

Package dimensions are provided in package drawings.

To find a package drawing, go to freescale.com and perform a keyword search for the drawing's document number:

If you want the drawing for this package	Then use this document number
100-pin LQFP	98ASS23308W
144-pin LQFP	98ASS23177W

5 Pinout

5.1 KM3x_256 Signal multiplexing and pin assignments

144 QFP	100 QFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
1	—	NC	NC								
2	—	NC	NC								
3	—	PTI5	Disabled	LCD_P45	PTI5						LCD_P45
4	1	PTA0/ LLWU_P16	Disabled	LCD_P23	PTA0/ LLWU_P16						LCD_P23
5	2	PTA1	Disabled	LCD_P24	PTA1						LCD_P24
6	—	PTI6	Disabled	LCD_P46	PTI6	UART2_RX					LCD_P46
7	—	PTI7	Disabled	LCD_P47	PTI7	UART2_TX					LCD_P47
8	3	PTA2	Disabled	LCD_P25	PTA2						LCD_P25
9	4	PTA3	Disabled	LCD_P26	PTA3						LCD_P26
10	5	PTA4/ LLWU_P15	NMI_b	LCD_P27	PTA4/ LLWU_P15					LCD_P27	NMI_b
11	6	PTA5	Disabled	LCD_P28	PTA5	CMP0_OUT					LCD_P28
12	7	PTA6/ LLWU_P14	Disabled	LCD_P29	PTA6/ LLWU_P14	XBAR_IN0					LCD_P29
13	8	PTA7	Disabled	LCD_P30	PTA7	XBAR_OUT0					LCD_P30
14	—	PTJ0	Disabled	LCD_P48	PTJ0	I2C1_SDA					LCD_P48
15	—	PTJ1	Disabled	LCD_P49	PTJ1	I2C1_SCL					LCD_P49

144 QFP	100 QFP	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
77	52	PTD5	Disabled	ADC0_SE4a	PTD5	LPTMR0_ ALT3	QTMR0_ TMR0	UART3_CTS_ b			
78	53	PTD6/ LLWU_P8	Disabled	ADC0_SE5a	PTD6/ LLWU_P8	LPTMR0_ ALT2	CMP1_OUT	UART3_RTS_ b			
79	54	PTD7/ LLWU_P7	Disabled	CMP0_IN4	PTD7/ LLWU_P7	I2C0_SCL	XBAR_IN4	UART3_RX			
80	55	PTE0	Disabled		PTE0	I2C0_SDA	XBAR_OUT4	UART3_TX	CLKOUT		
81	—	PTK2	Disabled	ADC0_SE14	PTK2	UART0_TX					
82	—	PTK3/ LLWU_P19	Disabled	ADC0_SE15	PTK3/ LLWU_P19	UART0_RX					
83	56	PTE1	RESET_b		PTE1						RESET_b
84	57	PTE2	EXTAL0	EXTAL0	PTE2	EWM_IN	XBAR_IN6	I2C1_SDA			
85	58	PTE3	XTAL0	XTAL0	PTE3	EWM_OUT_b	AFE_CLK	I2C1_SCL			
86	59	VSS	VSS	VSS							
87	60	VSSA	VSSA	VSSA							
88	61	VDDA	VDDA	VDDA							
89	62	VDD	VDD	VDD							
90	63	PTE4	Disabled		PTE4	LPTMR0_ ALT1	UART2_CTS_ b	EWM_IN			
91	64	PTE5/ LLWU_P6	Disabled		PTE5/ LLWU_P6	QTMR0_ TMR3	UART2_RTS_ b	EWM_OUT_b			
92	65	PTE6/ LLWU_P5	SWD_DIO	CMP0_IN2	PTE6/ LLWU_P5	XBAR_IN5	UART2_RX		I2C0_SCL		SWD_DIO
93	66	PTE7	SWD_CLK	ADC0_SE6a	PTE7	XBAR_OUT5	UART2_TX		I2C0_SDA		SWD_CLK
94	67	PTF0/ LLWU_P4	Disabled	ADC0_SE7a/ CMP2_IN3	PTF0/ LLWU_P4	RTC_CLKOUT	QTMR0_ TMR2	CMP0_OUT			
95	68	PTF1	Disabled	LCD_P0/ ADC0_SE8/ CMP2_IN4	PTF1	QTMR0_ TMR0	XBAR_OUT6				LCD_P0
96	69	PTF2	Disabled	LCD_P1/ ADC0_SE9/ CMP2_IN5	PTF2	CMP1_OUT	RTC_CLKOUT				LCD_P1
97	—	PTK4	Disabled	LCD_P51	PTK4	XBAR_IN9	AFE_CLK				LCD_P51
98	—	PTK5	Disabled		PTK5	UART1_RX					
99	—	PTK6	Disabled		PTK6	UART1_TX					
100	70	PTF3/ LLWU_P20	Disabled	LCD_P2	PTF3/ LLWU_P20	SPI1_PCS0	LPTMR0_ ALT2	UART0_RX			LCD_P2
101	71	PTF4	Disabled	LCD_P3	PTF4	SPI1_SCK	LPTMR0_ ALT1	UART0_TX			LCD_P3
102	72	PTF5	Disabled	LCD_P4	PTF5	SPI1_MISO	I2C1_SCL				LCD_P4
103	73	PTF6/ LLWU_P3	Disabled	LCD_P5	PTF6/ LLWU_P3	SPI1_MOSI	I2C1_SDA				LCD_P5
104	74	PTF7	Disabled	LCD_P6	PTF7	QTMR0_ TMR2	CLKOUT	CMP2_OUT			LCD_P6

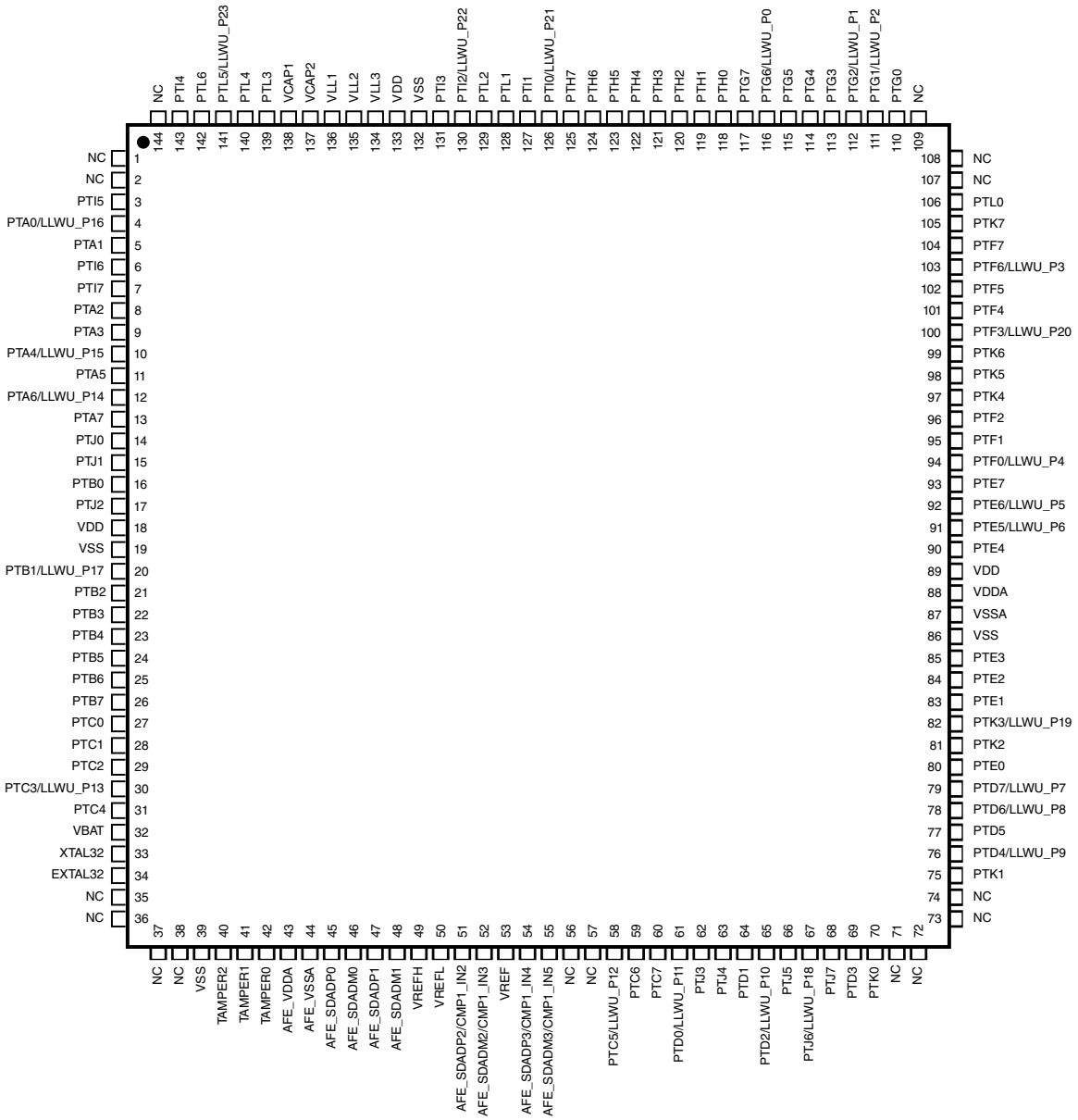


Figure 12. 144-pin LQFP Pinout Diagram

6 Ordering parts