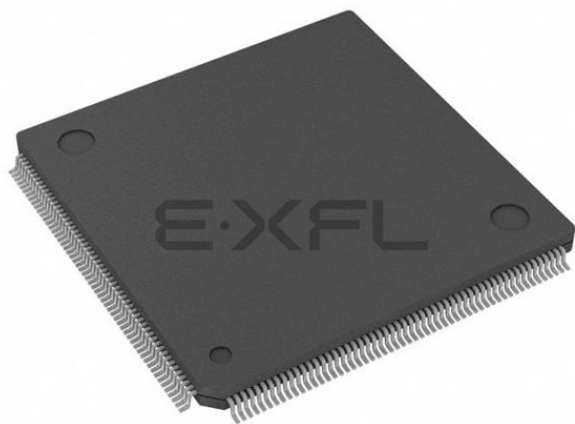




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Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I ² C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	190
Program Memory Size	1MB (1M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c18l0agl2000a

Product Name	S6E2C18H0A S6E2C19H0A S6E2C1AH0A	S6E2C18J0A S6E2C19J0A S6E2C1AJ0A	S6E2C18L0A S6E2C19L0A S6E2C1AL0A
Debug function	SWJ-DP/ETM/HTM		
Unique ID	Yes		

Notes:

- All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.
- See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
27	-	-	-	P59	E	I
				SOT11_1 (SDA11_1)		
				IC02_1		
				TIOB3_1		
				MADATA25_0		
28	-	-	-	P5A	E	I
				SCK11_1 (SCL11_1)		
				IC03_1		
				TIOB4_1		
				MADATA26_0		
29	-	-	-	P5B	E	I
				FRCK0_1		
				TIOB5_1		
				MADATA27_0		
30	21	18	G3	P08	E	K
				SIN14_0		
				TIOB12_0		
				INT17_0		
				MDQM0_0		
31	22	19	G4	P09	E	K
				SOT14_0 (SDA14_0)		
				TIOB13_0		
				INT18_0		
				MDQM1_0		
32	23	20	G5	P0A	L	I
				ADTG_1		
				SCK14_0 (SCL14_0)		
				AIN2_1		
				MCLKOUT_0		
33	-	-	-	P5C	E	I
				TIOA11_2		
				MADATA28_0		
				RTCCO_1		
				SUBOUT_1		
34	24	-	G6	P30	E	K
				TIOA13_2		
				INT03_2		
				MDQM2_0		
				I2SDI0_0		
35	25	-	H4	P31	E	I
				TIOB13_2		
				MDQM3_0		
				I2SCK0_0		
36	26	21	H2	P32	L	K
				BIN2_1		
				INT19_0		
				S_DATA1_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
84	69	59	J8	P74	E	I
				SCK9_0 (SCL9_0)		
				TIOB2_0		
				MAD03_0		
85	70	-	N8	PF2	L	I
				RTO10_1 (PPG10_1)		
				TIOA6_1		
				MRASX_0		
86	71	-	M8	PF3	L	K
				RTO11_1 (PPG10_1)		
				TIOB6_1		
				INT05_1 MCASX_0		
87	72	-	N9	PF4	L	K
				RTO12_1 (PPG12_1)		
				TIOA7_1		
				INT06_1 MSDWEX_0		
88	73	-	P9	PF5	L	K
				RTO13_1 (PPG12_1)		
				TIOB7_1		
				INT07_1 MCSX8_0		
89	74	-	M9	PF6	L	K
				RTO14_1 (PPG14_1)		
				TIOA14_1		
				INT20_1 MSDCKE_0		
90	75	-	L9	PF7	L	K
				RTO15_1 (PPG14_1)		
				TIOB14_1		
				INT21_1 MSDCLK_0		
91	76	60	K9	P75	E	K
				SIN8_0		
				TIOB3_0		
				AIN1_0 INT20_0 MAD04_0		
92	77	61	P10	P76	E	I
				SOT8_0 (SDA8_0)		
				TIOB4_0		
				BIN1_0 MAD05_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
194	162	132	E7	PCF	L	K
				RTS4_1		
				INT12_0		
195	163	133	F7	PD0	L	K
				INT30_1		
196	164	134	B6	PD1	L	K
				INT31_1		
197	165	135	C6	PD2	L	I
				CTS4_1		
				FRCK2_1		
198	166	136	D6	P6E	E	K
				ADTG_5		
				SCK4_1 (SCL4_1)		
				IC23_1		
				INT29_0		
199	-	-	-	P6D	E	I
				SCK14_1 (SCL14_1)		
				IC22_1		
				TIOB6_2		
200	-	-	-	P6C	E	I
				SOT14_1 (SDA14_1)		
				IC21_1		
				TIOA6_2		
201	-	-	-	P6B	E	K
				SIN14_1		
				IC20_1		
				TIOB7_2 INT14_2		
202	-	-	-	P6A	E	I
				DTTI2X_1 TIOA7_2		
203	-	-	-	P69	E	I
				RTO20_1 (PPG20_1)		
				TIOB14_2		
204	-	-	-	P68	E	I
				SCK13_1 (SCL13_0)		
				RTO21_1 (PPG20_1)		
				TIOA14_2		
205	-	-	-	P67	E	I
				SOT13_1 (SDA13_1)		
				RTO22_1 (PPG22_1)		
				TIOB15_2		
206	-	-	-	P66	E	K
				SIN13_1		
				RTO23_1 (PPG22_1)		
				TIOA15_2		
				INT15_2		

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch 7 TIOB pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch 8 TIOB pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch 9 TIOB pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch 10 TIOB pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch 11 TIOB pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch 12 TIOB pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch 13 TIOB pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch 14 TIOB pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base timer ch 15 TIOB pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-

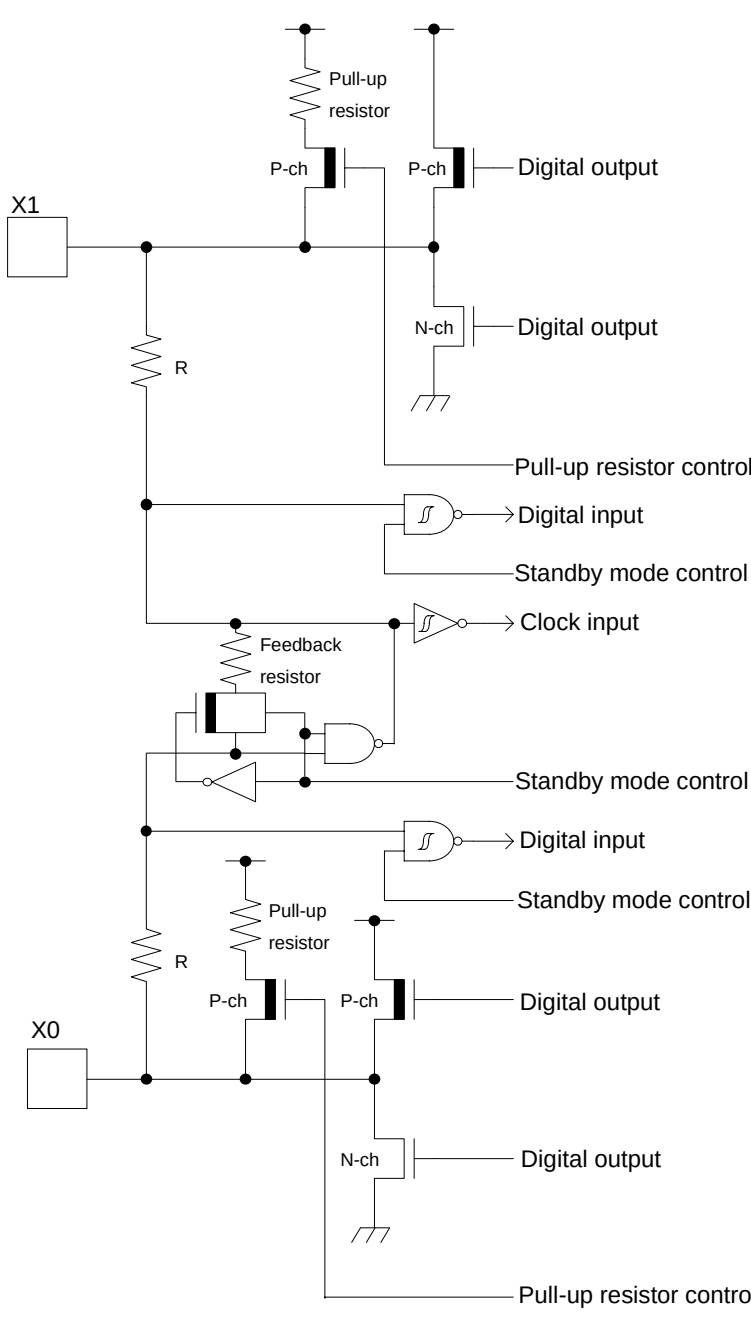
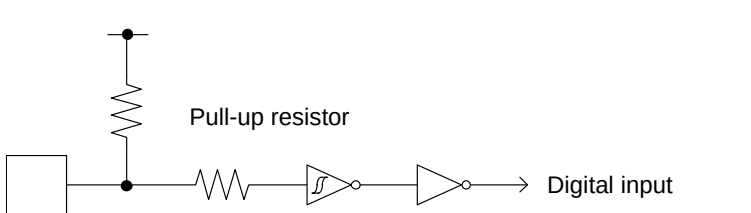
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MAD00_0	External bus interface address bus	81	66	56	J6
	MAD01_0		82	67	57	L8
	MAD02_0		83	68	58	K8
	MAD03_0		84	69	59	J8
	MAD04_0		91	76	60	K9
	MAD05_0		92	77	61	P10
	MAD06_0		93	78	62	N10
	MAD07_0		96	79	63	L10
	MAD08_0		97	80	64	K10
	MAD09_0		98	81	65	M10
	MAD10_0		142	116	92	G10
	MAD11_0		143	117	93	G9
	MAD12_0		144	118	94	F10
	MAD13_0		145	119	95	F11
	MAD14_0		146	120	96	F12
	MAD15_0		147	121	97	F13
	MAD16_0		152	122	98	E10
	MAD17_0		153	123	99	E11
	MAD18_0		154	124	100	E12
	MAD19_0		50	40	35	L1
	MAD20_0		49	39	34	K4
	MAD21_0		48	38	33	K3
	MAD22_0		47	37	32	K2
	MAD23_0		46	36	31	K1
	MAD24_0		45	35	30	J2
	MCSX0_0	External bus interface chip select output pin	71	56	48	M5
	MCSX1_0		70	55	47	L5
	MCSX2_0		61	51	43	N4
	MCSX3_0		60	50	42	M4
	MCSX4_0		59	49	41	L4
	MCSX5_0		58	48	40	M3
	MCSX6_0		57	47	39	N3
	MCSX7_0		56	46	38	N2
	MCSX8_0		88	73	-	P9

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External interrupt	INT06_0	External interrupt request 06 input pin	80	65	55	L6
	INT06_1		87	72	-	N9
	INT06_2		103	-	-	-
	INT07_0	External interrupt request 07 input pin	82	67	57	L8
	INT07_1		88	73	-	P9
	INT07_2		102	-	-	-
	INT08_0	External interrupt request 08 input pin	114	94	78	L11
	INT08_1		127	103	-	J9
	INT08_2		119	-	-	-
	INT09_0	External interrupt request 09 input pin	123	99	83	J13
	INT09_1		128	104	-	H10
	INT09_2		120	-	-	-
	INT10_0	External interrupt request 10 input pin	130	106	86	H9
	INT10_1		138	112	-	G13
	INT10_2		149	-	-	-
	INT11_0	External interrupt request 11 input pin	133	109	89	G14
	INT11_1		139	113	-	F14
	INT11_2		151	-	-	-
	INT12_0	External interrupt request 12 input pin	194	162	132	E7
	INT12_1		169	139	-	C11
	INT12_2		175	-	-	-
	INT13_0	External interrupt request 13 input pin	184	152	122	E8
	INT13_1		170	140	-	D11
	INT13_2		176	-	-	-
	INT14_0	External interrupt request 14 input pin	192	160	130	A6
	INT14_1		171	141	-	B10
	INT14_2		201	-	-	-
	INT15_0	External interrupt request 15 input pin	193	161	131	D7
	INT15_1		172	142	-	C10
	INT15_2		206	-	-	-
	INT16_0	External interrupt request 16 input pin	25	20	17	G2
	INT16_1		45	35	30	J2
	INT17_0	External interrupt request 17 input pin	30	21	18	G3
	INT17_1		46	36	31	K1
	INT18_0	External interrupt request 18 input pin	31	22	19	G4
	INT18_1		47	37	32	K2
	INT19_0	External interrupt request 19 input pin	36	26	21	H2
	INT19_1		48	38	33	K3
	INT20_0	External interrupt request 20 input pin	91	76	60	K9
	INT20_1		89	74	-	M9

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 0	DTTIOX_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	44	34	29	J3
	DTTIOX_1		21	-	-	-
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	37	27	22	J1
	FRCK0_1		29	-	-	-
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	43	33	28	J4
	IC00_1		22	-	-	-
	IC01_0		42	32	27	J5
	IC01_1		26	-	-	-
	IC02_0		41	31	26	H6
	IC02_1		27	-	-	-
	IC03_0		38	28	23	H3
	IC03_1		28	-	-	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0.	45	35	30	J2
	RTO00_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output modes.	10	10	-	E2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0.	46	36	31	K1
	RTO01_1 (PPG00_1)	This pin operates as PPG00 when it is used in PPG0 output modes.	11	11	-	E3
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	47	37	32	K2
	RTO02_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	12	12	-	E4
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0.	48	38	33	K3
	RTO03_1 (PPG02_1)	This pin operates as PPG02 when it is used in PPG0 output modes.	13	-	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	49	39	34	K4
	RTO04_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	19	-	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0.	50	40	35	L1
	RTO05_1 (PPG04_1)	This pin operates as PPG04 when it is used in PPG0 output modes.	20	-	-	-

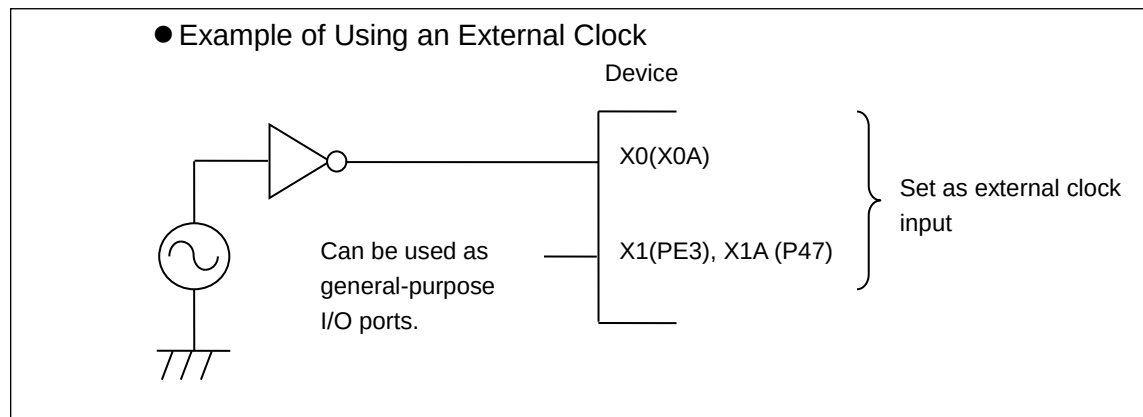
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Reset	INITX	External reset Input pin A reset is valid when INITX = L.	72	57	49	N5
Mode	MD1	Mode 1 pin During serial programming to flash memory, MD1 = L must be input.	104	84	68	N13
	MD0	Mode 0 pin During normal operation, MD0 = L must be input. During serial programming to flash memory, MD0 = H must be input.	105	85	69	N12
Power	VCC	Power supply pin	1	1	1	C1
			39	29	24	H1
			55	45	37	N1
			64	54	46	P4
			109	89	73	M14
			137	-	-	-
			163	133	109	A13
			188	156	126	A9
			213	173	141	A4
GND	VSS	GND pin	40	30	25	H5
			54	44	36	M1
			63	53	45	P3
			108	88	72	N14
			136	-	-	-
			162	132	108	B14
			189	157	127	A8
			216	176	144	B1
			-	-	-	E1
			-	-	-	G1
			-	-	-	P7
			-	-	-	P11
			-	-	-	L14
			-	-	-	A11
			-	-	-	A5
			-	-	-	N7
			-	-	-	M7
			-	-	-	K7
			-	-	-	J7
			-	-	-	G7
			-	-	-	H7
			-	-	-	H8
			-	-	-	G8

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation/GPIO function. When the main oscillation is selected: - Oscillation feedback resistor: approximately 1 MΩ - Standby mode control When the GPIO is selected: - CMOS level output. - CMOS level hysteresis input - Pull-up resistor control - Standby mode control - Pull-up resistor: approximately 50 kΩ $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$
B		- CMOS level hysteresis input - Pull-up resistor: approximately 50 kΩ

Using an External Clock

When using an external clock as an input of the main clock, set X0/X1 to the external clock input, and input the clock to X0. X1(PE3) can be used as a general-purpose I/O port. Similarly, when using an external clock as an input of the sub clock, set X0A/X1A to the external clock input and input the clock to X0A. X1A (P47) can be used as a general-purpose I/O port.

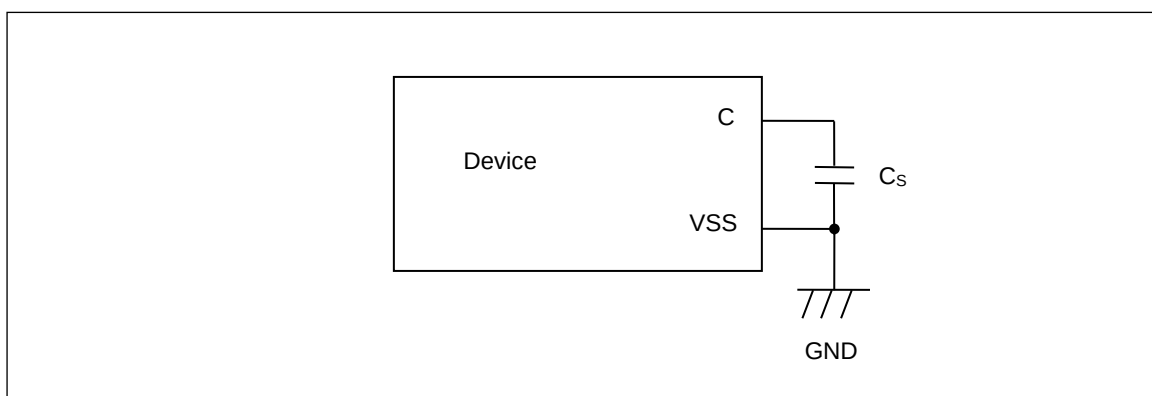


Handling When Using Multi-Function Serial Pin As I²C Pin

If the application uses the multi-function serial pin as an I²C pin, the P-channel transistor of the digital output must be disabled. I²C pins need to conform to electrical limitations like other pins, however, and avoid connecting to live external systems with the MCU power off.

C Pin

Devices in this series contain a regulator. Be sure to connect a smoothing capacitor (C_s) for the regulator between the C pin and the GND pin. Please use a ceramic capacitor or a capacitor of equivalent frequency characteristics as a smoothing capacitor. Some laminated ceramic capacitors have a large capacitance variation due to thermal fluctuation. Please select a capacitor that meets the specifications in the operating conditions to use by evaluating the temperature characteristics of the device. A smoothing capacitor of about 4.7 μF would be recommended for this series.



Mode Pins (MD0)

Connect the MD pin (MD0) directly to VCC or VSS pins. Design the printed circuit board such that the pull-up/down resistance stays low, the distance between the mode pins and VCC pins or VSS pins is as short as possible, and the connection impedance is low when the pins are pulled up/down such as for switching the pin level and rewriting the flash memory data. This is important to prevent the device from erroneously switching to test mode as a result of noise.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State	
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable	
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1	
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-	
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected	
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0		
	GPIO selected										
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled	
	External interrupt enable selected								GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled							
	GPIO selected										

- 1: Oscillation is stopped at Sub Timer mode, sub CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.
- 2: Maintain previous state at Timer mode. GPIO selected internal input fixed at 0 at RTC mode, Stop mode.
- 3: Maintain previous state at Timer mode. Hi-Z/internal input fixed at 0 at RTC mode, Stop mode.
- 4: It shows the case selected by EPFR14.E_SPLC register.

Table 12-7 Typical and Maximum Current Consumption in Sleep Operation (Other than PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I _{CCS}	V _{CC}	Sleep operation*5 (main oscillation)	4 MHz	3.4	82.6	mA	*3 When all peripheral clocks are on
					2.5	81.7	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in High-speed CR)	4 MHz	2.5	81.7	mA	*3 When all peripheral clocks are on
					1.7	80.9	mA	*3 When all peripheral clocks are off
			Sleep operation*6 (sub oscillation)	32 kHz	0.75	79.97	mA	*3 When all peripheral clocks are on
					0.74	79.96	mA	*3 When all peripheral clocks are off
			Sleep operation (built-in low-speed CR)	100 kHz	0.79	80.01	mA	*3 When all peripheral clocks are on
					0.76	79.98	mA	*3 When all peripheral clocks are off

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are fixed.

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

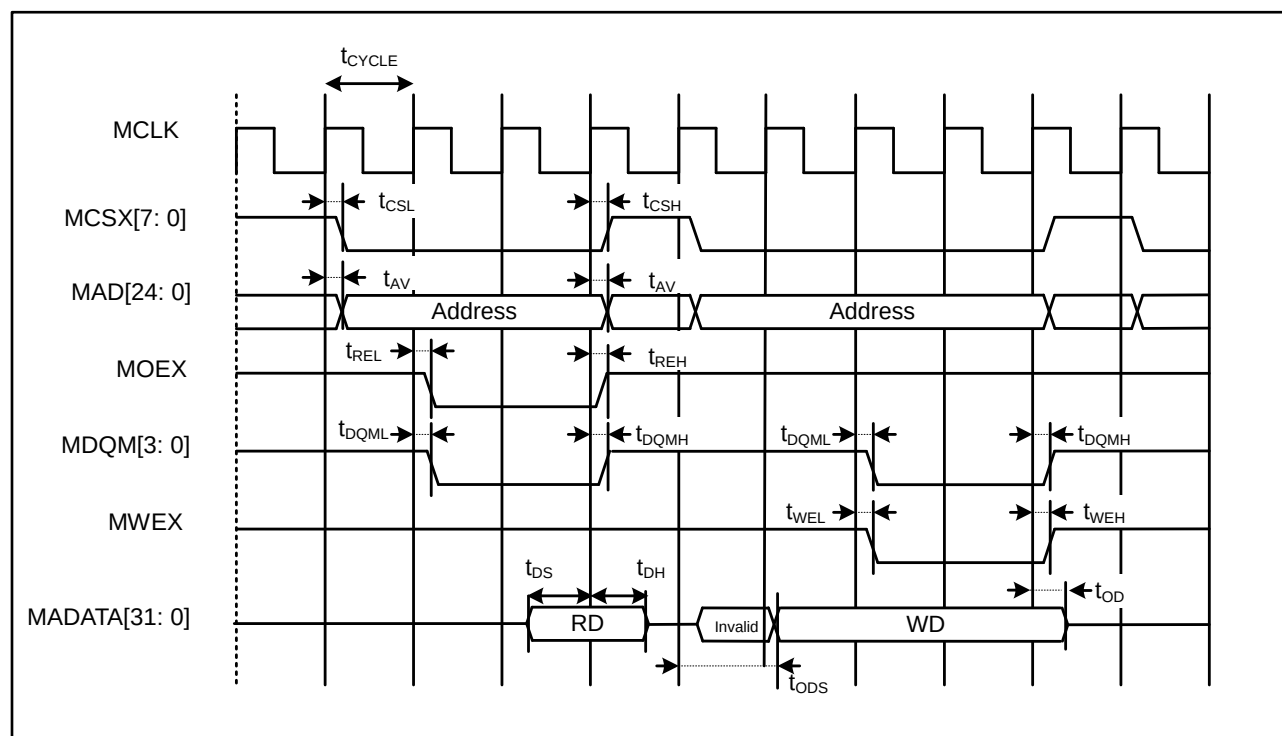
Separate Bus Access Synchronous SRAM Mode

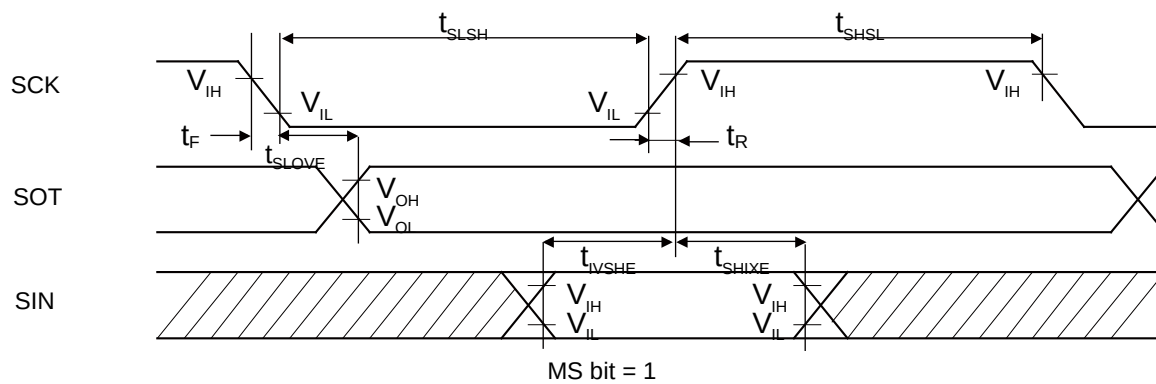
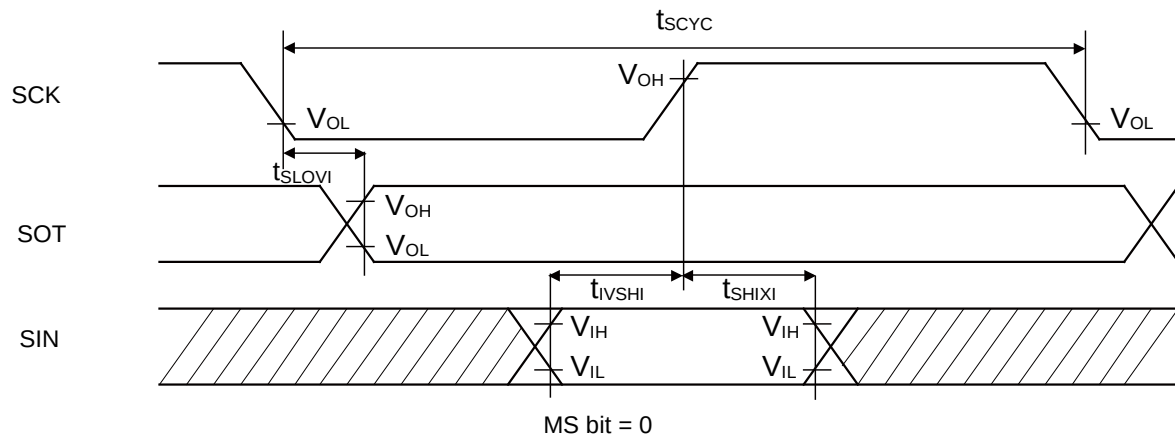
($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Address delay time	t_{AV}	MCLK, MAD[24: 0]	-	1	9	ns	
MCSX delay time	t_{CSL}	MCLK, MCSX[7: 0]	-	1	9	ns	
	t_{CSH}		-	1	9	ns	
MOEX delay time	t_{REL}	MCLK, MOEX	-	1	9	ns	
	t_{REH}		-	1	9	ns	
Data set up → MCLK ↑ time	t_{DS}	MCLK, MADATA[31: 0]	-	19	-	ns	
MCLK ↑ → Data hold time	t_{DH}	MCLK, MADATA[31: 0]	-	0	-	ns	
MWEX delay time	t_{WEL}	MCLK, MWEX	-	1	9	ns	
	t_{WEH}		-	1	9	ns	
MDQM[1: 0] delay time	t_{DQML}	MCLK, MDQM[3: 0]	-	1	9	ns	
	t_{DQMH}		-	1	9	ns	
MCLK ↑ → Data output time	t_{ODS}	MCLK, MADATA[31: 0]	-	MCLK+1	MCLK+18	ns	
MCLK ↑ → Data hold time	t_{OD}	MCLK, MADATA[31: 0]	-	1	18	ns	

Note:

- When the external load capacitance $CL = 30$ pF





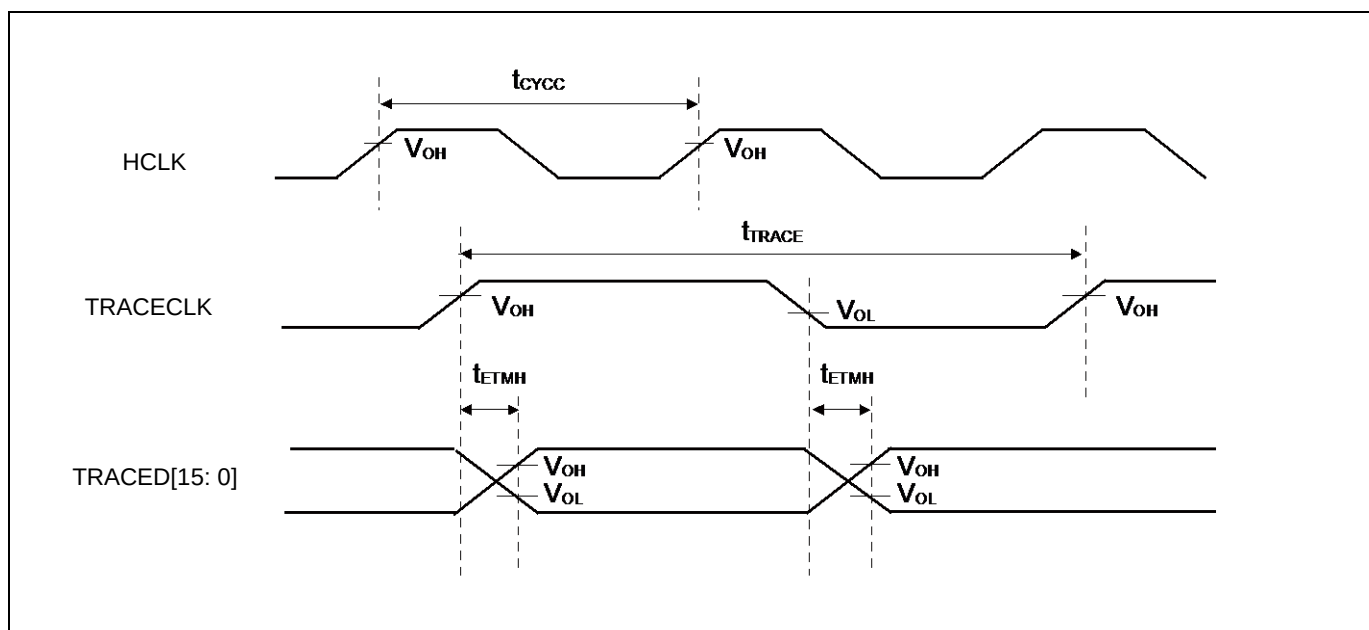
12.4.17 ETM/ HTM Timing

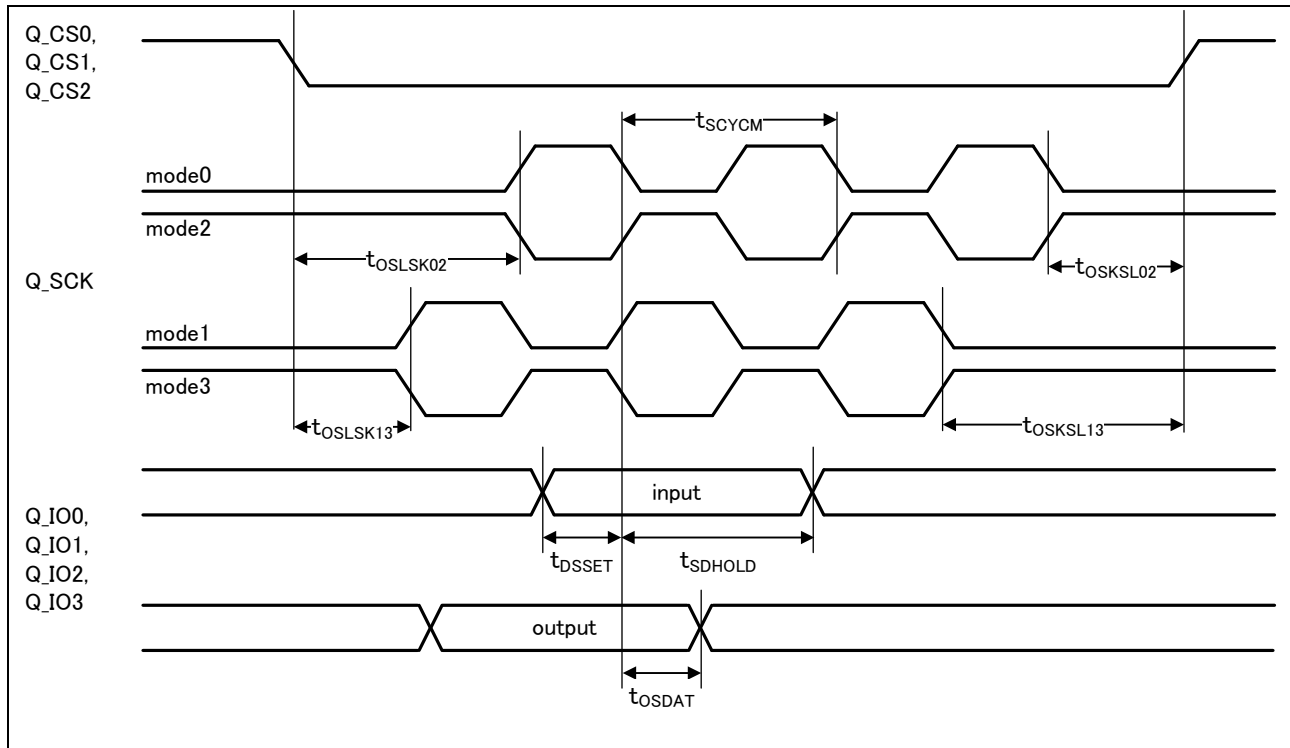
($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Data hold	t_{ETMH}	TRACECLK, TRACED[15: 0]	$V_{\text{CC}} \geq 4.5\text{V}$	2	9	ns	
			$V_{\text{CC}} < 4.5\text{V}$	2	15		
TRACECLK frequency	$1/t_{\text{TRACE}}$	TRACECLK	$V_{\text{CC}} \geq 4.5\text{V}$		50	MHz	
			$V_{\text{CC}} < 4.5\text{V}$		32	MHz	
TRACECLK clock cycle	t_{TRACE}		$V_{\text{CC}} \geq 4.5\text{V}$	20	-	ns	
			$V_{\text{CC}} < 4.5\text{V}$	31.25	-	ns	

Note:

- When the external load capacitance $C_L = 30$ pF.





12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = AV_{RL} = 0V$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15 AVCC - 15	- -	AVRH + 15 AVCC + 15	mV mV	
Conversion time	-	-	0.5 ^{*1}	-	-	μs	AVCC ≥ 4.5 V
Sampling time *2	t_s	-	0.15	-	10	μs	AVCC ≥ 4.5 V
			0.3	-			AVCC < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AVCC ≥ 4.5 V
			50	-	1000		AVCC < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	μs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	μA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	μA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AVCC ≥ 4.5 V
					1.8		AVCC < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	μA	
Analog input voltage	-	ANxx	AVSS	-	AVRH	V	
			AVSS	-	AVCC	V	
Reference voltage	-	AVRH	4.5	-	AVCC	V	Tcck < 50 ns
			2.7	-	AVCC		Tcck ≥ 50 ns
	-	AVRL	AVSS	-	AVSS	V	

1: The conversion time is the value of sampling time (t_s) + compare time (t_c).

The condition of the minimum conversion time is when the value of $T_s = 150$ ns and $T_c = 350$ ns ($AV_{CC} \geq 4.5V$). Ensure that it satisfies the value of sampling time (t_s) and compare clock cycle (t_{CCK}).

For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

- 2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).
 3: The compare time (t_c) is the value of (Equation 2).

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