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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	120
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c19h0agv2000a

Product Name	S6E2C18H0A S6E2C19H0A S6E2C1AH0A	S6E2C18J0A S6E2C19J0A S6E2C1AJ0A	S6E2C18L0A S6E2C19L0A S6E2C1AL0A
Debug function	SWJ-DP/ETM/HTM		
Unique ID	Yes		

Notes:

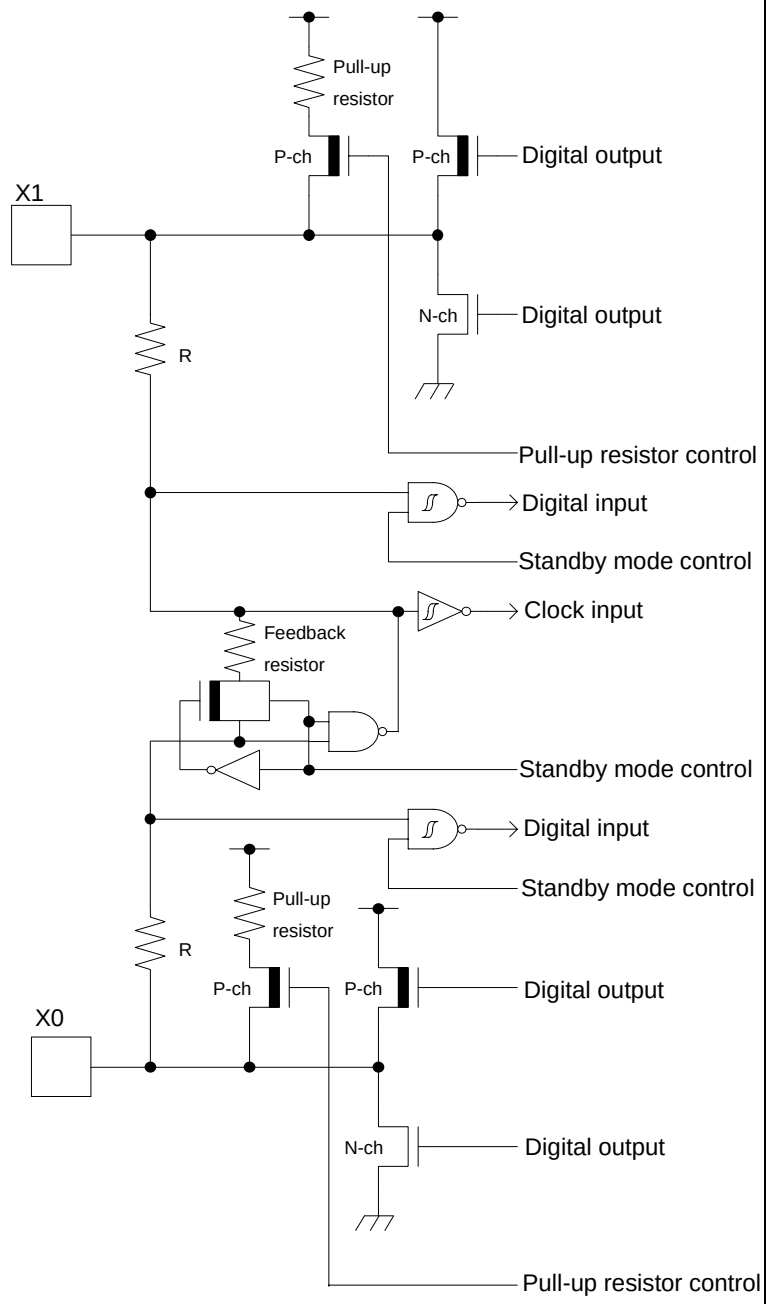
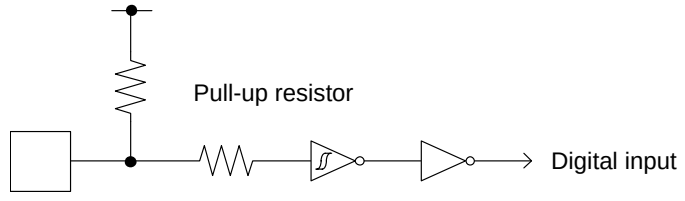
- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.*

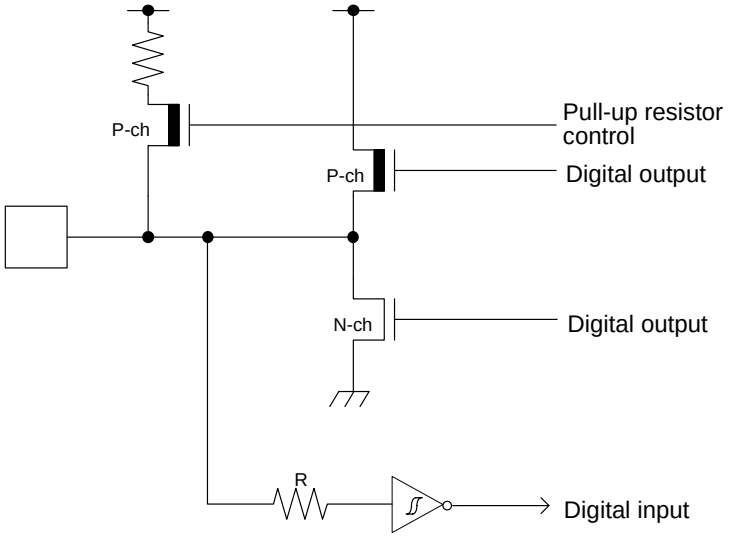
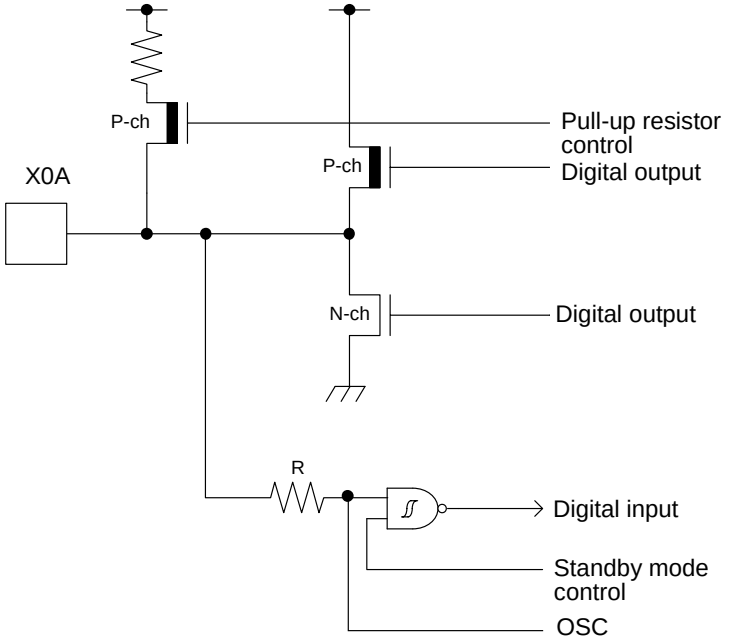
Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
93	78	62	N10	P77 SCK8_0 (SCL8_0) TIOB5_0 ZIN1_0 MAD06_0	E	I
94	-	-	-	PF8 SCS70_1 DTTI1X_1 AIN1_1	E	I
95	-	-	-	PF9 SCS71_1 IC10_1 BIN1_1	E	I
96	79	63	L10	P78 SIN6_0 IC10_0 INT21_0 MAD07_0	E	K
97	80	64	K10	P79 SOT6_0 (SDA6_0) IC11_0 MAD08_0	L	I
98	81	65	M10	P7A SCK6_0 (SCL6_0) IC12_0 MAD09_0	L	I
99	82	66	N11	P7B DA1 SCS60_0 IC13_0 INT22_0	R	J
100	83	67	M11	P7C DA0 SCS61_0 INT04_1	R	J
101	-	-	-	PFA SCK7_1 (SCL7_1) IC11_1 ZIN1_1	E	I
102	-	-	-	PFB SOT7_1 (SDA7_1) IC12_1 INT07_2	E	K
103	-	-	-	PFC SIN7_1 IC13_1 INT06_2	E	K
104	84	68	N13	PE0 MD1	C	E
105	85	69	N12	MD0	J	D

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	146	120	96	F12
	SOT5_1 (SDA5_1)		171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I²C (operation mode 4).	145	119	95	F11
	SCK5_1 (SCL5_1)		172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	97	80	64	K10
	SOT6_1 (SDA6_1)		118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I²C (operation mode 4).	98	81	65	M10
	SCK6_1 (SCL6_1)		126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 1	DTTI1X_0	Input signal controlling waveform generator outputs RTO10 to RTO15 of Multi-Function Timer 1.	70	55	47	L5
	DTTI1X_1		94	-	-	-
	FRCK1_0	16-bit free-run timer ch 1 external clock input pin	71	56	48	M5
	FRCK1_1		78	63	-	K5
	IC10_0	16-bit input capture input pin of Multi-Function Timer 1. ICxx describes channel number.	96	79	63	L10
	IC10_1		95	-	-	-
	IC11_0		97	80	64	K10
	IC11_1		101	-	-	-
	IC12_0		98	81	65	M10
	IC12_1		102	-	-	-
	IC13_0		99	82	66	N11
	IC13_1		103	-	-	-
	RTO10_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	56	46	38	N2
	RTO10_1 (PPG10_1)		85	70	-	N8
	RTO11_0 (PPG10_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG10 when it is used in PPG1 output modes.	57	47	39	N3
	RTO11_1 (PPG10_1)		86	71	-	M8
	RTO12_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	58	48	40	M3
	RTO12_1 (PPG12_1)		87	72	-	N9
	RTO13_0 (PPG12_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG12 when it is used in PPG1 output modes.	59	49	41	L4
	RTO13_1 (PPG12_1)		88	73	-	P9
	RTO14_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	60	50	42	M4
	RTO14_1 (PPG14_1)		89	74	-	M9
	RTO15_0 (PPG14_0)	Waveform generator output pin of Multi-Function Timer 1. This pin operates as PPG14 when it is used in PPG1 output modes.	61	51	43	N4
	RTO15_1 (PPG14_1)		90	75	-	L9

5. I/O Circuit Type

Type	Circuit	Remarks
A		It is possible to select the main oscillation/GPIO function. When the main oscillation is selected: ・ Oscillation feedback resistor: approximately 1 MΩ ・ Standby mode control When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA
B		・ CMOS level hysteresis input ・ Pull-up resistor: approximately 50 kΩ

Type	Circuit	Remarks
O		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・Pull-up resistor control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR register (pseudo-open drain control) ・For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (002-04856)”. ・For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856). ・
P		・CMOS level output ・CMOS level hysteresis input ・Pull-up resistor control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).

6. Handling Precautions

Every semiconductor device has a characteristic, inherent rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

6.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

Processing and Protection of Pins

These precautions must be followed when handling the pins that connect semiconductor devices to power supply and I/O functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions, if present for extended periods of time, can damage the device; therefore, avoid this type of connection.

3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power-supply pin or ground pin.

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

   CAUTION: Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-
P	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled
	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	GPIO selected
	Resource other than above selected						Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	
	GPIO selected									
Q	WKUP enabled	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	WKUP input enabled	Hi-Z/ WKUP input enabled	WKUP input enabled
	External interrupt enable selected							GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0			
	GPIO selected									

1: Oscillation is stopped at Sub Timer mode, sub CR Timer mode, RTC mode, Stop mode, Deep Standby RTC mode, and Deep Standby Stop mode.

2: Maintain previous state at Timer mode. GPIO selected internal input fixed at 0 at RTC mode, Stop mode.

3: Maintain previous state at Timer mode. Hi-Z/internal input fixed at 0 at RTC mode, Stop mode.

4: It shows the case selected by EPFR14.E_SPLC register.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1 ,*3	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1 ,*4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1 ,*4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *5	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	10 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *6	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			10	mA	10 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total maximum output current *7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *5	I_{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	10 mA type
			- 20	mA	12 mA type
H level average output current *6	I_{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 10	mA	10 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	200	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

2: V_{CC} must not drop below V_{SS} - 0.5 V.

3: V_{BAT} must not drop below V_{SS} - 0.5 V.

4: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

12.4.8 Power-On Reset Timing

(V_{SS} = 0V)

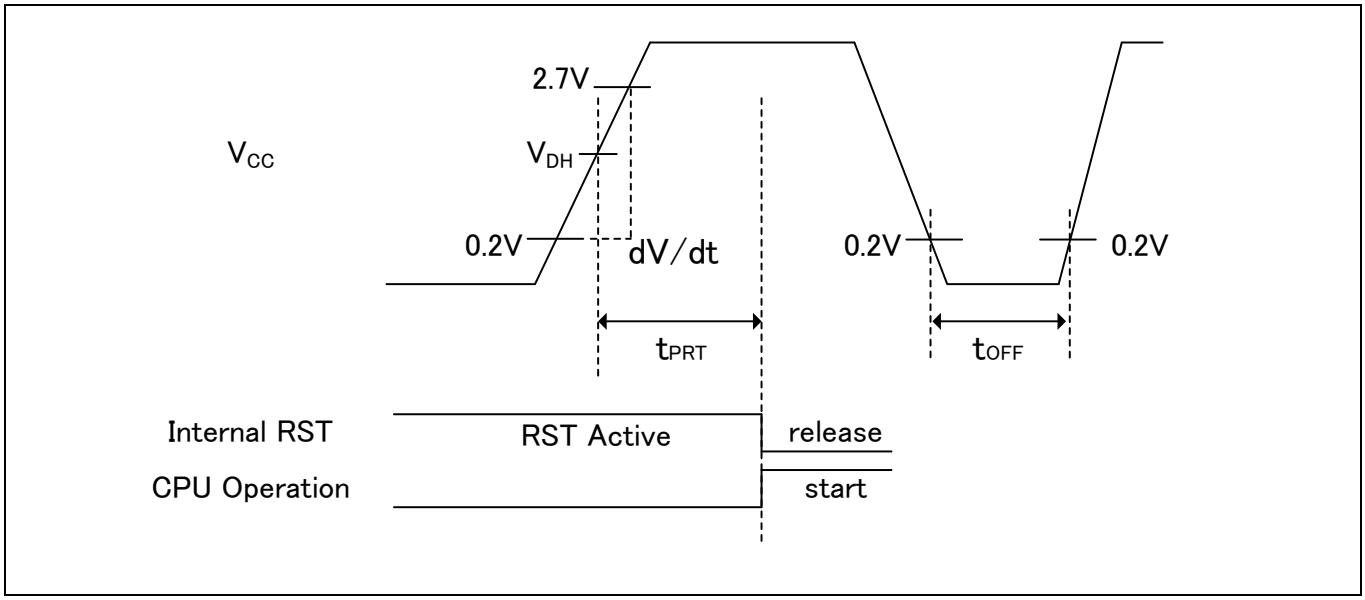
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply shut down time	t_{OFF}	VCC	-	1	-	-	ms	*1
Power ramp rate	dV/dt		V_{CC}: 0.2V to 2.70V	0.6	-	1000	mV/µs	*2
Time until releasing Power-on reset	t_{PRT}		-	0.33	-	0.60	ms	

*1: V_{CC} must be held below 0.2V for a minimum period of t_{OFF}. Improper initialization may occur if this condition is not met.

*2: This dV/dt characteristic is applied at the power-on of cold start (t_{OFF}>1ms).

Note:

- *If t_{OFF} cannot be satisfied designs must assert external reset(INITX) at power-up and at any brownout event per 12. 4. 7.*



Glossary

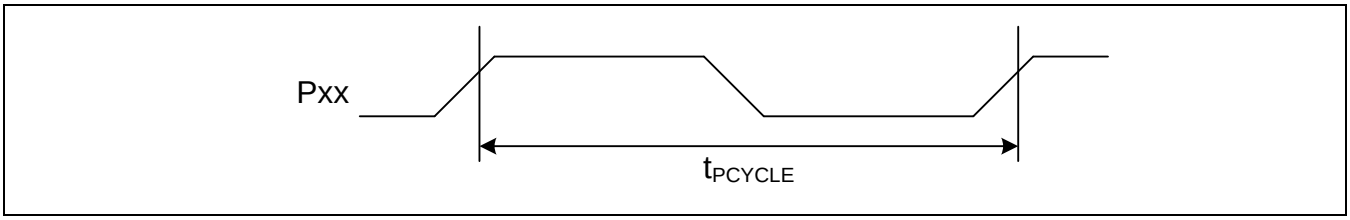
□ V_{DH}: detection voltage of Low Voltage detection reset. See “12.7. Low-Voltage Detection Characteristics”.

12.4.9 GPIO Output Characteristics

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Output frequency	t_{PCYCLE}	Pxx*	V_{CC} ≥ 4.5V	-	50	MHz	
			V_{CC} < 4.5V	-	32	MHz	

*: GPIO is a target.



High-Speed Synchronous Serial (SPI = 1, SCINV = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

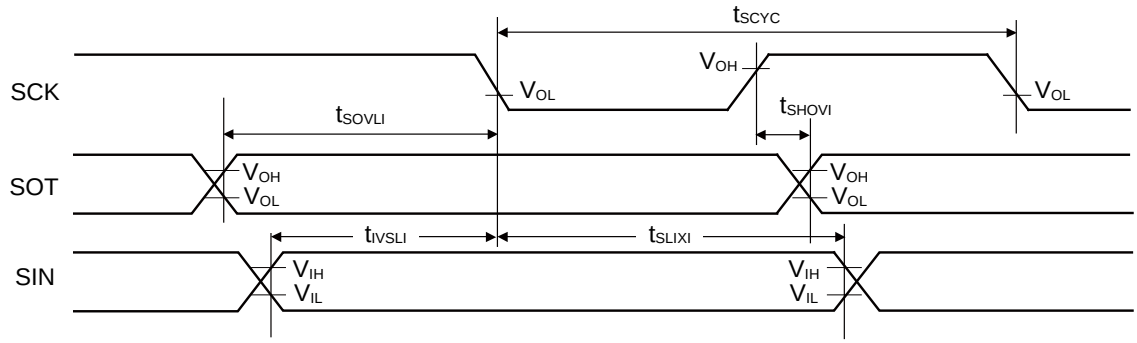
Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↑→SOT delay time	t_{SHOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↓ setup time	t_{IVSLI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↓→SIN hold time	t_{SLIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↑→SOT delay time	t_{SHOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↓ setup time	t_{IVSLE}	SCKx, SINx		5	-	5	-	ns
SCK↓→SIN hold time	t_{SLIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

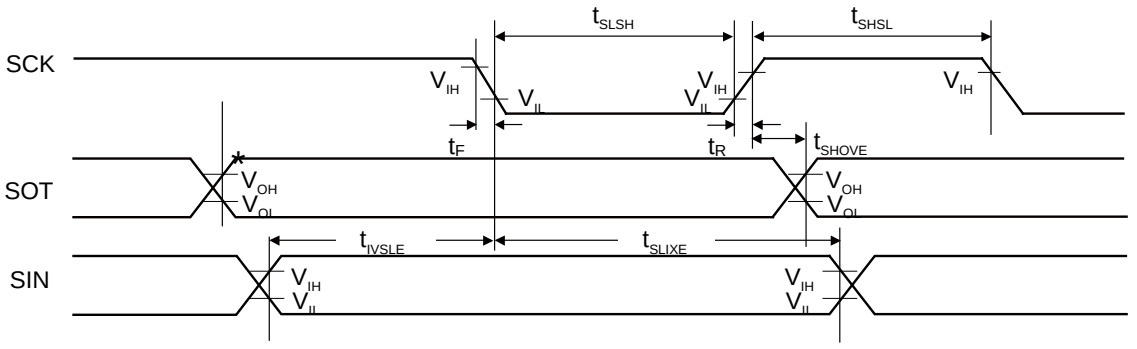
- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*

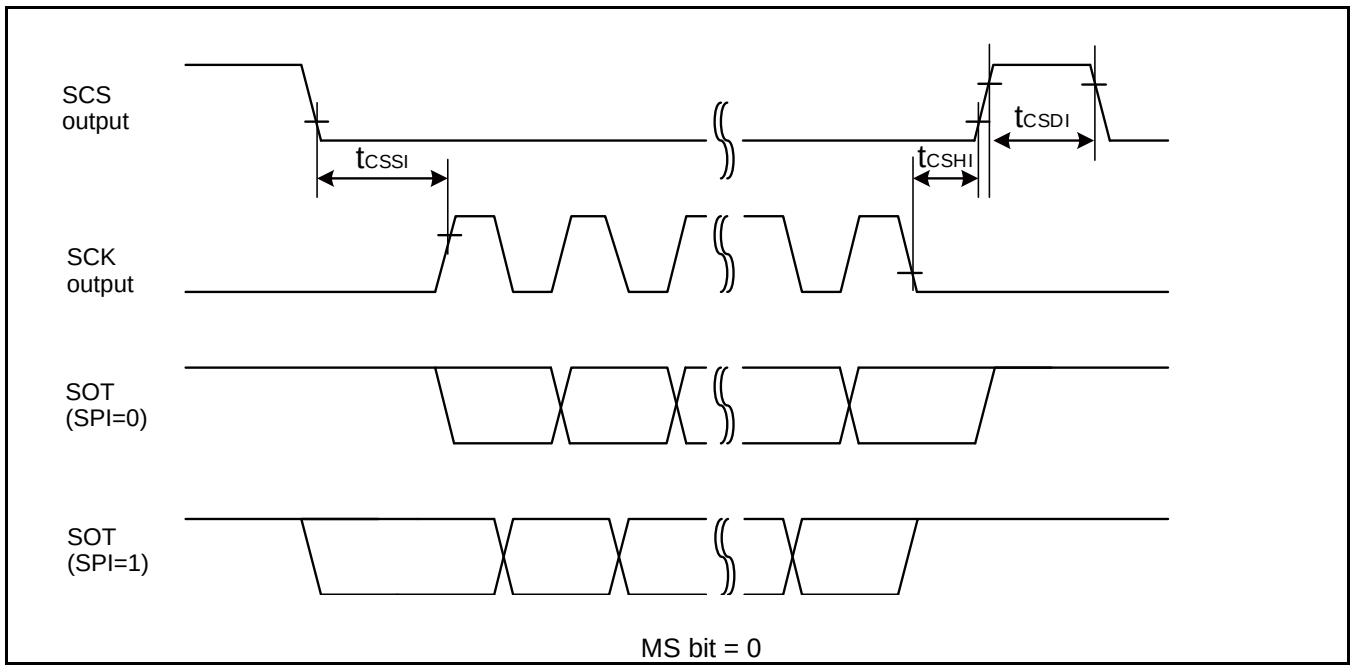


MS bit = 0

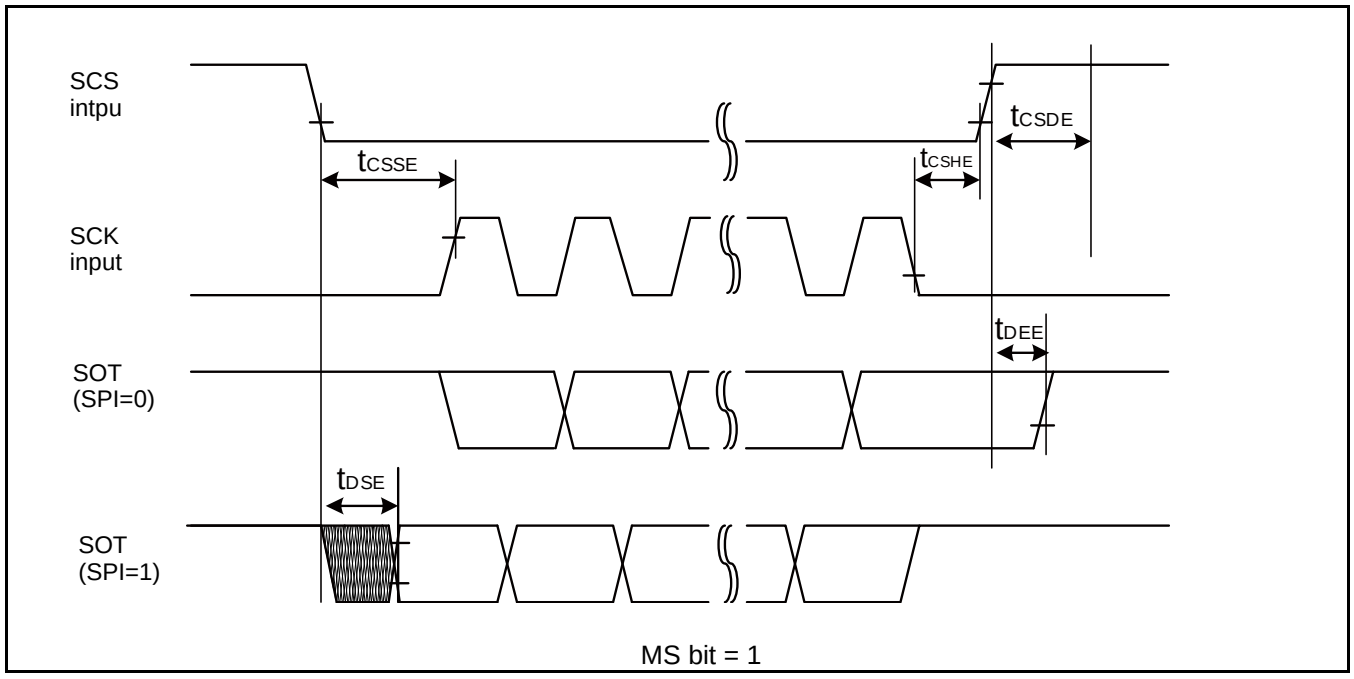


MS bit = 1

*: Changes when writing to TDR register



MS bit = 0



MS bit = 1

Fast mode Plus (Fm+)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	Fast mode Plus (Fm+)*6		Unit	Remarks
			Min	Max		
SCL clock frequency	f_{SCL}	C_L = 30 pF, R = (V_p/I_{OL})*1	0	1000	kHz	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		0.26	-	µs	
SCL clock L width	t_{LOW}		0.5	-	µs	
SCL clock H width	t_{HIGH}		0.26	-	µs	
SCL clock frequency	t_{SUSTA}		0.26	-	µs	
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDDAT}		0	0.45*2, *3	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		50	-	ns	
Stop condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		0.26	-	µs	
Bus free time between "Stop condition" and "START condition"	t_{BUF}		0.5	-	µs	
Noise filter	t_{SP}	60 MHz ≤ t_{CYCP} < 80 MHz	6 t_{CYCP}*4	-	ns	*5
		80 MHz ≤ t_{CYCP} ≤ 100 MHz	8 t_{CYCP}*4	-	ns	

1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. V_p indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

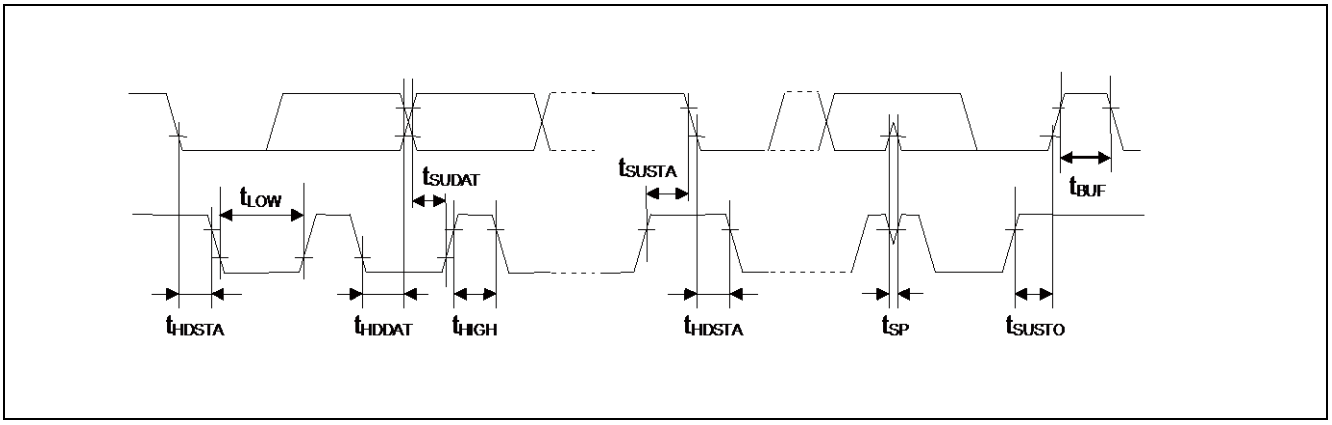
2: The maximum t_{HDDT} must not extend beyond the low period (t_{LOW}) of the device's SCL signal.

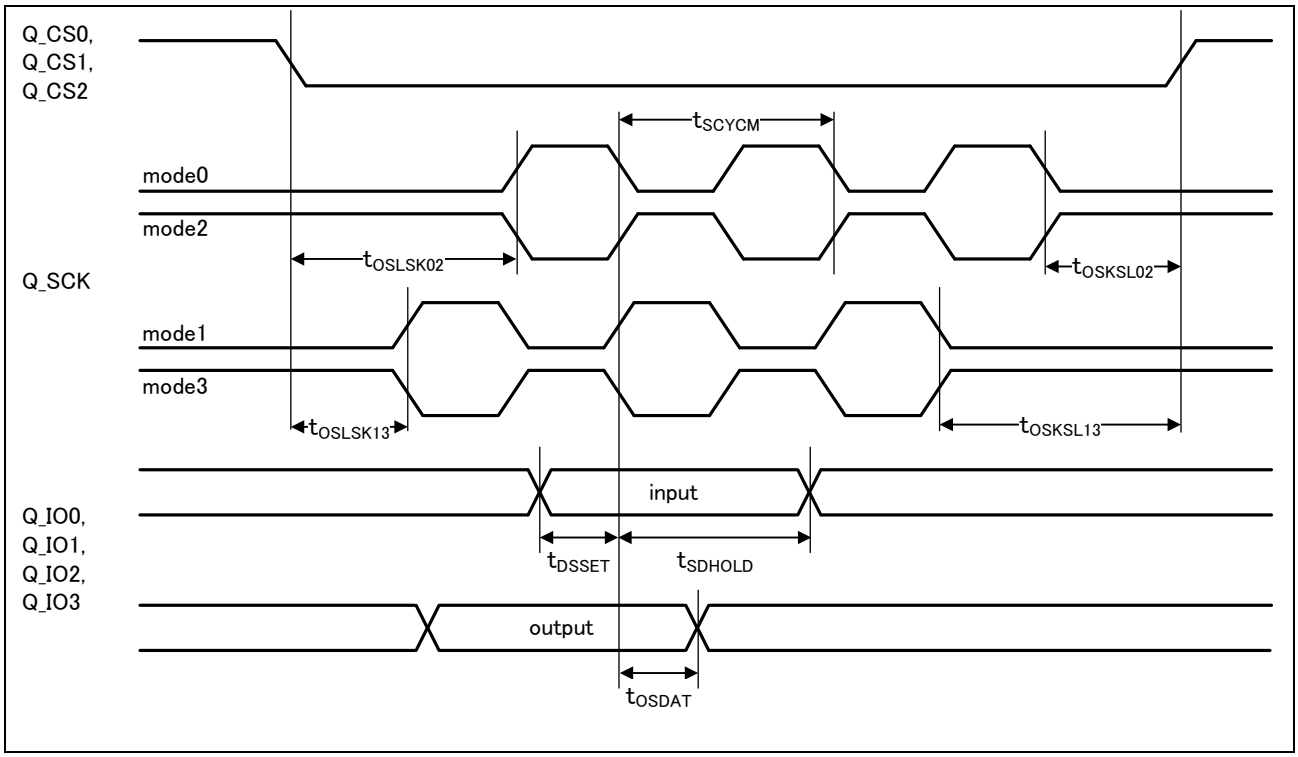
3: The Fast mode I^2C bus device can be used on a Standard-mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns."

4: t_{CYCP} is the APB bus clock cycle time. For more information about the APB bus number to which the I^2C is connected, see 8.Block Diagram in this data sheet.
To use fast mode plus (Fm+), set the peripheral bus clock at 64 MHz or more.

5: The noise filter time can be changed by register settings. Change the number of the noise filter steps according to the APB bus clock frequency.

6: When using fast mode plus (Fm+), set the I/O pin to the mode corresponding to I^2C Fm+ in the EPFR register.
See Chapter 12: I/O Port in FM4 Family Peripheral Manual Main Part (002-04856) for the details.




Q_CS0,
Q_CS1,
Q_CS2
tSCYCM
mode0
mode2
tOSLSK02
tOSKSL02
Q_SCK
mode1
mode3
tOSLSK13
tOSKSL13
input
Q_IO0,
Q_IO1,
Q_IO2,
Q_IO3
tDSSET
tSDHOLD
output
tOSDAT

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = AVRL = 0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH – 15	-	AVRH + 15	mV	
			AV_{CC} - 15	-	AV_{CC} + 15	mV	
Conversion time	-	-	0.5*1	-	-	µs	AV_{CC} ≥ 4.5 V
Sampling time *2	t_S	-	0.15	-	10	µs	AV_{CC} ≥ 4.5 V
			0.3	-			AV_{CC} < 4.5 V
Compare clock cycle*3	t_{CCK}	-	25	-	1000	ns	AV_{CC} ≥ 4.5 V
			50	-	1000		AV_{CC} < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	µs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	µA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	µA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AV_{CC} ≥ 4.5 V
					1.8		AV_{CC} < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	µA	
Analog input voltage	-	ANxx	AV_{SS}	-	AVRH	V	
			AV_{SS}	-	AV_{CC}	V	
Reference voltage	-	AVRH	4.5	-	AV_{CC}	V	Tcck ＜50 ns
			2.7	-	AV_{CC}		Tcck ≥ 50 ns
	-	AVRL	AV_{SS}	-	AV_{SS}	V	

1: The conversion time is the value of sampling time (t_S) + compare time (t_C).

The condition of the minimum conversion time is when the value of Ts = 150 ns and Tc = 350 ns (AV_{CC} ≥ 4.5V). Ensure that it satisfies the value of sampling time (t_S) and compare clock cycle (t_{CCK}).

For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

3: The compare time (t_C) is the value of (Equation 2).

12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

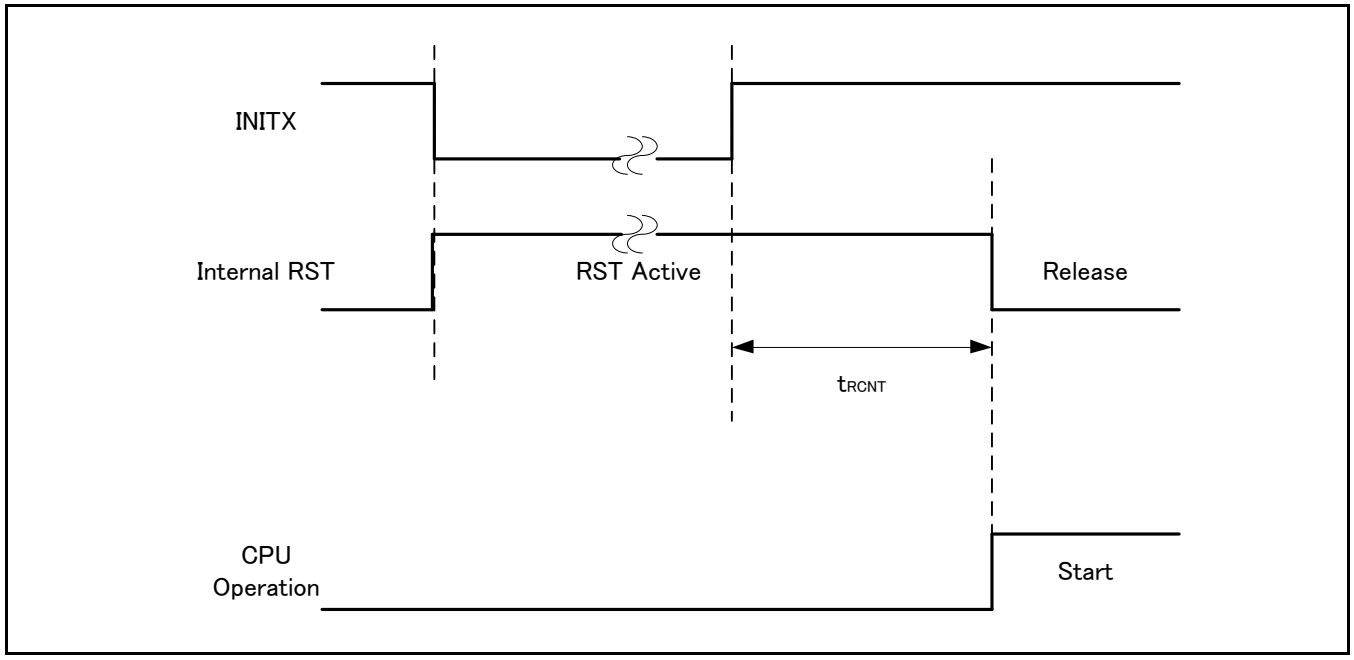
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

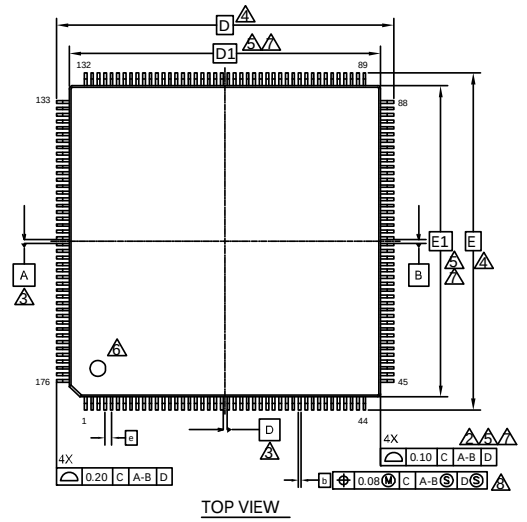
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR Timer mode		315	567	µs	
Sub Timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep Standby RTC mode with RAM retention		336	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		336	667	µs	with RAM retention

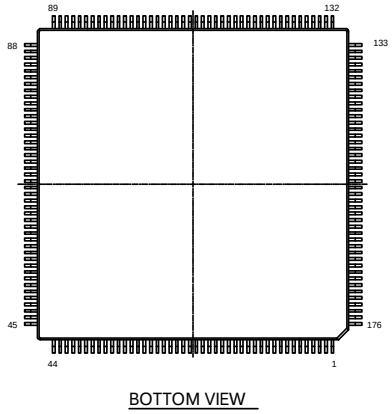
*: The maximum value depends on the built-in CR accuracy.

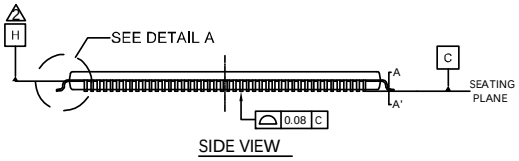
Example of Standby Recovery Operation (when in INITX Recovery)

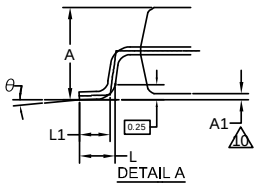


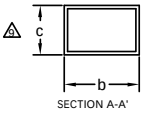
Package Type	Package Code
LQFP 176	LQP 176











SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

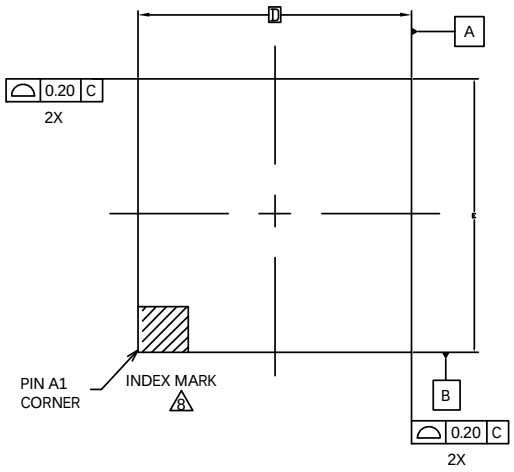
NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

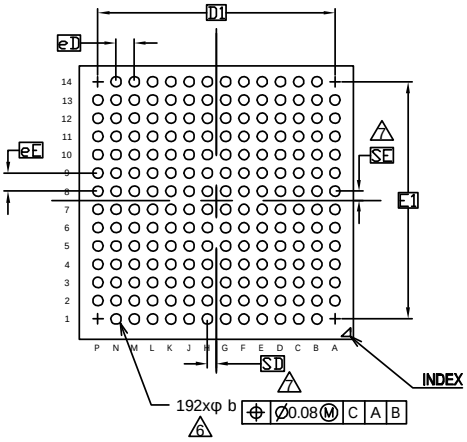
002-15150 **

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**

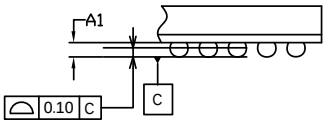
Package Type	Package Code
PFBGA 192	LBE 192



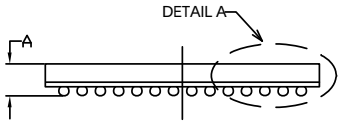
TOP VIEW



BOTTOM VIEW



DETAIL A



SIDE VIEW

SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.45
A1	0.25	0.35	0.45
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E 1	10.40 BSC		
MD	14		
ME	14		
n	192		
Φb	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD / SE	0.40 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
4. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" =0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
9. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-13493 **

PACKAGE OUTLINE, 192 BALL FBGA
12.00X12.00X1.45 MM LBE192 REV**