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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I ² C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c19j0agb1000a

1. Product Lineup

Memory Size

Product Name		S6E2C18H/J/L	S6E2C19H/J/L	S6E2C1AH/J/L
On-chip flash memory		1024 Kbytes	1536 Kbytes	2048 Kbytes
On-chip	SRAM	128 Kbytes	192 Kbytes	256 Kbytes
	SRAM0	64 Kbytes	128 Kbytes	192 Kbytes
	SRAM1	32 Kbytes	32 Kbytes	32 Kbytes
	SRAM2	32 Kbytes	32 Kbytes	32 Kbytes

Function

Product Name			S6E2C18H0A S6E2C19H0A S6E2C1AH0A	S6E2C18J0A S6E2C19J0A S6E2C1AJ0A	S6E2C18L0A S6E2C19L0A S6E2C1AL0A
Pin count			144	176/192	216
CPU			Cortex-M4F, MPU, NVIC 128 ch		
Freq.			200 MHz		
Power supply voltage range			2.7 V to 5.5 V		
DMAC			8ch		
DSTC			256 ch		
External bus interface			Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash NAND flash	Addr: 25-bit (Max), Data: 8-/16-bit CS: 9 (Max), SRAM, NOR flash , NAND flash SDRAM	Addr: 25-bit (Max), Data: 8-/16-/32-bit CS: 9 (Max), SRAM, NOR flash , NAND flash, SDRAM
Multi-function serial interface (UART/CSIO/LIN/I ² C)			16ch (Max) ch 0 to ch 7 : FIFO, ch 8 to ch 15 : No FIFO		
Base timer (PWC/Reload timer/PWM/PPG)			16 ch (Max)		
MF timer	A/D activation compare	6 ch	3 units (Max)		
	Input capture	4 ch			
	Free-run timer	3 ch			
	Output compare	6 ch			
	Waveform generator	3 ch			
	PPG	3 ch			
SD card interface			1 unit		
I ² S			-	1 unit	
High-speed quad SPI			-	1 unit	
QPRC			4 ch (Max)		
Dual timer			1 unit		
Real-time clock			1 unit		
Watch counter			1 unit		
CRC accelerator			Yes (fixed, programmable)		
Watchdog timer			1 ch (SW) + 1 ch (HW)		
External interrupts			32 pins (Max)+ NMI × 1		
I/O ports			120 pins (Max)	152 pins (Max)	190 pins (Max)
12-bit A/D converter			24 ch (3 units)	32 ch (3 units)	
12-bit D/A converter			2 units (Max)		
CSV (clock supervisor)			Yes		
LVD (low-voltage detector)			2 ch		
Built-in CR	High-speed		4 MHz		
	Low-speed		100 kHz		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
172	142	-	C10	P93	S	K
				SCK5_1		
				(SCL5_1)		
				INT15_1		
173	143	-	D10	Q_IO0_0	S	I
				P94		
				CTS5_1		
				Q_SCK_0		
174	144	-	B9	P95	S	I
				RTS5_1		
				Q_CS0_0		
175	-	-	-	P96	S	K
				INT12_2		
				Q_CS1_0		
176	-	-	-	P97	S	K
				INT13_2		
				Q_CS2_0		
177	145	115	C9	PC0	K	I
178	146	116	B8	PC1	K	I
				TIOB6_0		
179	147	117	D9	PC2	K	I
				TIOA6_0		
180	148	118	E9	PC3	K	I
				TIOB7_0		
181	149	119	F9	PC4	K	I
				TIOA7_0		
182	150	120	C8	PC5	K	I
				TIOB14_0		
183	151	121	D8	PC6	K	I
				TIOA14_0		
184	152	122	E8	PC7	E	K
				INT13_0		
				CROUT_1		
185	153	123	A10	PC8	K	I
186	154	124	F8	PC9	K	I
				TIOB15_0		
187	155	125	B7	PCA	K	I
				TIOA15_0		
188	156	126	A9	VCC	-	-
189	157	127	A8	VSS	-	-
190	158	128	A7	PCB	L	K
				INT28_0		
191	159	129	C7	PCC	K	I
192	160	130	A6	PCD	L	K
				SOT4_1		
				(SDA4_1)		
193	161	131	D7	INT14_0	L	K
				PCE		
				SIN4_1		
				INT15_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
207	167	-	E6	P65	E	K
				RTO24_1 (PPG24_1)		
				INT28_1		
208	168	-	B5	P64	I	K
				CTS4_0		
				RTO25_1 (PPG24_1)		
				INT29_1		
209	169	137	C5	P63	L	K
				ADTG_3		
				RTS4_0		
				INT30_0		
				MOEX_0		
210	170	138	B4	P62	L	I
				SCK4_0 (SCL4_0)		
				MWEX_0		
211	171	139	C4	P61	L	I
				UHCONX0		
				SOT4_0 (SDA4_0)		
				MALE_0		
				RTCCO_0		
				SUBOUT_0		
212	172	140	B3	P60	I	Q
				SIN4_0		
				INT31_0		
				WKUP3		
213	173	141	A4	VCC	-	-
214	174	142	A3	P80	H	R
				UDM0		
215	175	143	A2	P81	H	R
				UDP0		
216	176	144	B1	VSS	-	-
-	-	-	E1		-	-
-	-	-	G1		-	-
-	-	-	P7		-	-
-	-	-	P11		-	-
-	-	-	L14		-	-
-	-	-	A11		-	-
-	-	-	A5		-	-
-	-	-	N7		-	-
-	-	-	M7		-	-
-	-	-	L7		-	-
-	-	-	K7		-	-
-	-	-	J7		-	-
--	-	-	G7		-	-
-	-	-	H7		-	-
-	-	-	H8		-	-
-	-	-	G8		-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MADATA00_0	External bus interface data bus (address/data multiplex bus)	2	2	2	B2
	MADATA01_0		3	3	3	C2
	MADATA02_0		4	4	4	C3
	MADATA03_0		5	5	5	D5
	MADATA04_0		6	6	6	D2
	MADATA05_0		7	7	7	D1
	MADATA06_0		8	8	8	D3
	MADATA07_0		9	9	9	D4
	MADATA08_0		14	13	10	E5
	MADATA09_0		15	14	11	F1
	MADATA10_0		16	15	12	F2
	MADATA11_0		17	16	13	F3
	MADATA12_0		18	17	14	F4
	MADATA13_0		23	18	15	F5
	MADATA14_0		24	19	16	F6
	MADATA15_0		25	20	17	G2
	MADATA16_0		10	-	-	-
	MADATA17_0		11	-	-	-
	MADATA18_0		12	-	-	-
	MADATA19_0		13	-	-	-
	MADATA20_0		19	-	-	-
	MADATA21_0		20	-	-	-
	MADATA22_0		21	-	-	-
	MADATA23_0		22	-	-	-
	MADATA24_0		26	-	-	-
	MADATA25_0		27	-	-	-
	MADATA26_0		28	-	-	-
	MADATA27_0		29	-	-	-
	MADATA28_0		33	-	-	-
	MADATA29_0		51	-	-	-
	MADATA30_0		52	-	-	-
	MADATA31_0		53	-	-	-
	MDQM0_0	External bus interface byte mask signal output pin	30	21	18	G3
	MDQM1_0		31	22	19	G4
	MDQM2_0		34	-	-	-
	MDQM3_0		35	-	-	-
	MALE_0	External bus interface address latch enable output signal for multiplex	211	171	139	C4
	MRDY_0	External bus interface external RDY input signal	80	65	55	L6
	MCLKOUT_0	External bus clock signal	32	23	20	G5

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10	General-purpose I/O port 1	114	94	78	L11
	P11		115	95	79	K13
	P12		116	96	80	K12
	P13		117	97	81	K14
	P14		118	98	82	K11
	P15		123	99	83	J13
	P16		124	100	84	J12
	P17		125	101	85	J11
	P18		130	106	86	H9
	P19		131	107	87	H12
	P1A		132	108	88	H14
	P1B		133	109	89	G14
	P1C		134	110	90	H13
	P1D		135	111	91	H11
	P1E		142	116	92	G10
	P1F		143	117	93	G9
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
	P26		152	122	98	E10
	P27		147	121	97	F13
	P28		146	120	96	F12
	P29		145	119	95	F11
	P2A		144	118	94	F10

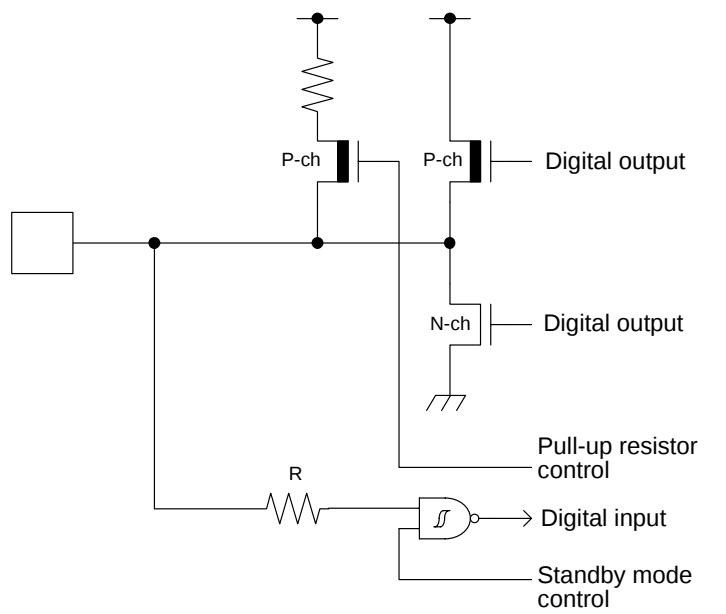
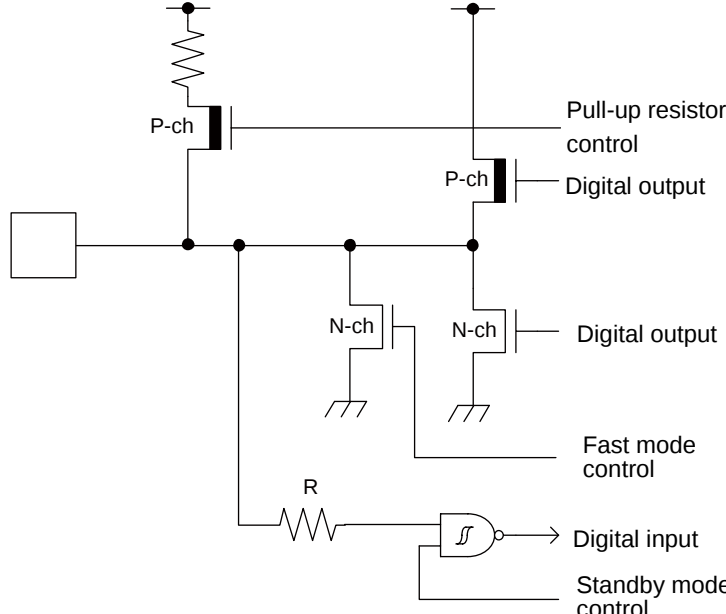
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P50	General-purpose I/O port 5	10	10	-	E2
	P51		11	11	-	E3
	P52		12	12	-	E4
	P53		13	-	-	-
	P54		19	-	-	-
	P55		20	-	-	-
	P56		21	-	-	-
	P57		22	-	-	-
	P58		26	-	-	-
	P59		27	-	-	-
	P5A		28	-	-	-
	P5B		29	-	-	-
	P5C		33	-	-	-
	P5D		51	41	-	L2
	P5E		52	42	-	L3
	P5F		53	43	-	M2
	P60	General-purpose I/O port 6	212	172	140	B3
	P61		211	171	139	C4
	P62		210	170	138	B4
	P63		209	169	137	C5
	P64		208	168	-	B5
	P65		207	167	-	E6
	P66		206	-	-	-
	P67		205	-	-	-
	P68		204	-	-	-
	P69		203	-	-	-
	P6A		202	-	-	-
	P6B		201	-	-	-
	P6C		200	-	-	-
	P6D		199	-	-	-
	P6E		198	166	136	D6

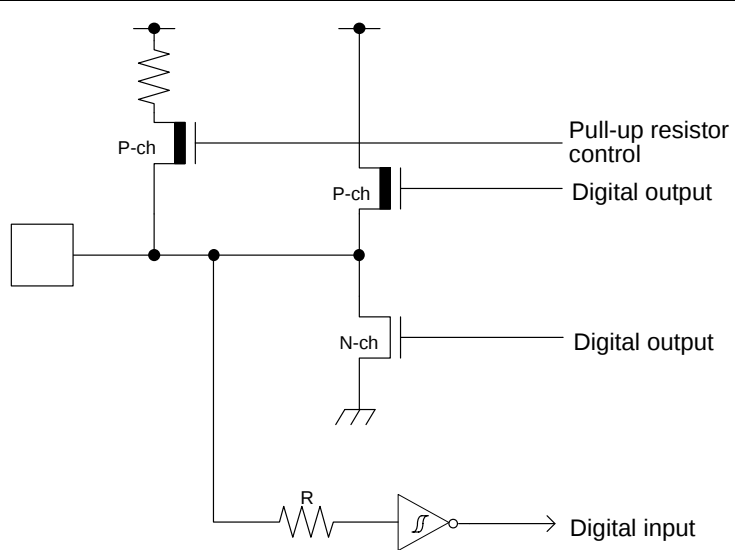
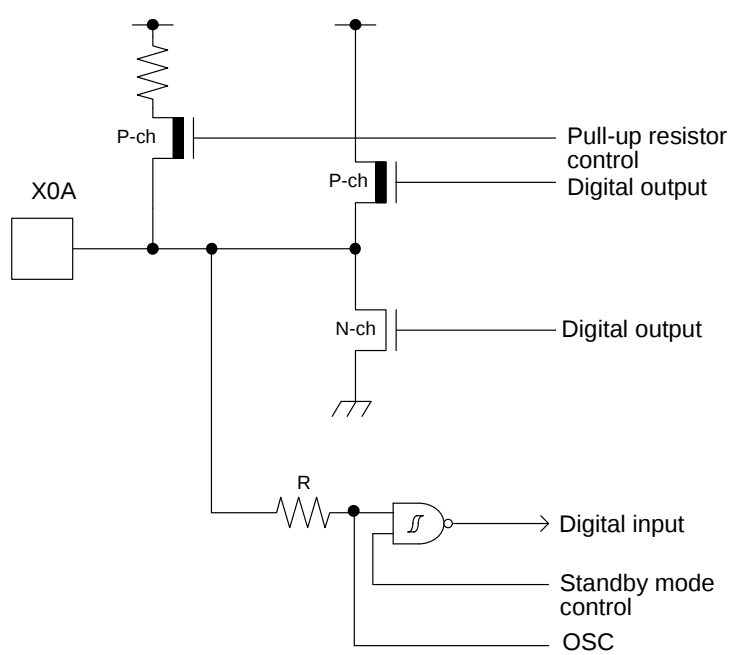
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 3	SIN3_0	Multi-function serial interface ch 3 input pin	25	20	17	G2
	SIN3_1		56	46	38	N2
	SOT3_0 (SDA3_0)	Multi-function serial interface ch 3 output pin. This pin operates as SOT3 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA3 when it is used in an I ² C (operation mode 4).	24	19	16	F6
	SOT3_1 (SDA3_1)		57	47	39	N3
	SCK3_0 (SCL3_0)	Multi-function serial interface ch 3 clock I/O pin. This pin operates as SCK3 when it is used in a CSIO (operation modes 2) and as SCL3 when it is used in an I ² C (operation mode 4).	23	18	15	F5
	SCK3_1 (SCL3_1)		58	48	40	M3
Multi-Function Serial 4	SIN4_0	Multi-function serial interface ch 4 input pin	212	172	140	B3
	SIN4_1		193	161	131	D7
	SOT4_0 (SDA4_0)	Multi-function serial interface ch 4 output pin. This pin operates as SOT4 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA4 when it is used in an I ² C (operation mode 4).	211	171	139	C4
	SOT4_1 (SDA4_1)		192	160	130	A6
	SCK4_0 (SCL4_0)	Multi-function serial interface ch 4 clock I/O pin. This pin operates as SCK4 when it is used in a CSIO (operation mode 2) and as SCL4 when it is used in an I ² C (operation mode 4).	210	170	138	B4
	SCK4_1 (SCL4_1)		198	166	136	D6
	CTS4_0	Multi-function serial interface ch 4 CTS input pin	208	168	-	B5
	CTS4_1		197	165	135	C6
	RTS4_0	Multi-function serial interface ch 4 RTS output pin	209	169	137	C5
	RTS4_1		194	162	132	E7

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 10	SIN10_0	Multi-function serial interface ch 10 input pin	114	94	78	L11
	SIN10_1		51	41	-	L2
	SOT10_0 (SDA10_0)	Multi-function serial interface ch 10 output pin. This pin operates as SOT10 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA10 when it is used in an I ² C (operation mode 4).	115	95	79	K13
	SOT10_1 (SDA10_1)		52	42	-	L3
	SCK10_0 (SCL10_0)	Multi-function serial interface ch 10 clock I/O pin. This pin operates as SCK10 when it is used in a CSIO (operation mode 2) and as SCL10 when it is used in an I ² C (operation mode 4).	116	96	80	K12
	SCK10_1 (SCL10_1)		53	43	-	M2
Multi-Function Serial 11	SIN11_0	Multi-function serial interface ch 11 input pin	123	99	83	J13
	SIN11_1		26	-	-	-
	SOT11_0 (SDA11_0)	Multi-function serial interface ch 11 output pin. This pin operates as SOT11 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA11 when it is used in an I ² C (operation mode 4).	124	100	84	J12
	SOT11_1 (SDA11_1)		27	-	-	-
	SCK11_0 (SCL11_0)	Multi-function serial interface ch 11 clock I/O pin. This pin operates as SCK11 when it is used in a CSIO (operation mode 2) and as SCL11 when it is used in an I ² C (operation mode 4).	125	101	85	J11
	SCK11_1 (SCL11_1)		28	-	-	-
Multi-Function Serial 12	SIN12_0	Multi-function serial interface ch 12 input pin	133	109	89	G14
	SIN12_1		65	-	-	-
	SOT12_0 (SDA12_0)	Multi-function serial interface ch 12 output pin. This pin operates as SOT12 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA12 when it is used in an I ² C (operation mode 4).	134	110	90	H13
	SOT12_1 (SDA12_1)		66	-	-	-
	SCK12_0 (SCL12_0)	Multi-function serial interface ch 12 clock I/O pin. This pin operates as SCK12 when it is used in a CSIO (operation mode 2) and as SCL12 when it is used in an I ² C (operation mode 4).	135	111	91	H11
	SCK12_1 (SCL12_1)		67	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch 0 AIN input pin	56	46	38	N2
	AIN0_1		65	-	-	-
	AIN0_2		114	94	78	L11
	BIN0_0	QPRC ch 0 BIN input pin	57	47	39	N3
	BIN0_1		66	-	-	-
	BIN0_2		115	95	79	K13
	ZIN0_0	QPRC ch 0 ZIN input pin	58	48	40	M3
	ZIN0_1		67	-	-	-
	ZIN0_2		116	96	80	K12
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch 1 AIN input pin	91	76	60	K9
	AIN1_1		94	-	-	-
	AIN1_2		123	99	83	J13
	BIN1_0	QPRC ch 1 BIN input pin	92	77	61	P10
	BIN1_1		45	-	-	-
	BIN1_2		124	100	84	J12
	ZIN1_0	QPRC ch 1 ZIN input pin	93	78	62	N10
	ZIN1_1		101	-	-	-
	ZIN1_2		125	101	85	J11
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch 2 AIN input pin	2	2	2	B2
	AIN2_1		32	23	20	G5
	AIN2_2		120	-	-	-
	BIN2_0	QPRC ch 2 BIN input pin	3	3	3	C2
	BIN2_1		36	26	21	H2
	BIN2_2		121	-	-	-
	ZIN2_0	QPRC ch 2 ZIN input pin	4	4	4	C3
	ZIN2_1		37	27	22	J1
	ZIN2_2		122	-	-	-
Quadrature Position/ Revolution Counter 3	AIN3_0	QPRC ch 3 AIN input pin	18	17	14	F4
	AIN3_1		45	35	30	J2
	AIN3_2		149	-	-	-
	BIN3_0	QPRC ch 3 BIN input pin	23	18	15	F5
	BIN3_1		46	36	31	K1
	BIN3_2		150	-	-	-
	ZIN3_0	QPRC ch 3 ZIN input pin	24	19	16	F6
	ZIN3_1		47	37	32	K2
	ZIN3_2		151	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Real-time clock	RTCCO_0	0.5 seconds pulse output pin of real-time clock	211	171	139	C4
	RTCCO_1		33	-	-	-
	SUBOUT_0	Sub-clock output pin	211	171	139	C4
	SUBOUT_1		33	-	-	-
Low power Consumption mode	WKUP0	Deep Standby mode return signal input pin 0	158	128	104	C13
	WKUP1	Deep Standby mode return signal input pin 1	14	13	10	E5
	WKUP2	Deep Standby mode return signal input pin 2	70	55	47	L5
	WKUP3	Deep Standby mode return signal input pin 3	212	172	140	B3
D/A converter	DA0	D/A converter ch 0 analog output pin	100	83	67	M11
	DA1	D/A converter ch 1 analog output pin	99	82	66	N11
VBAT	VREGCTL	On-board regulator control pin	76	61	53	N6
	VWAKEUP	The return signal input pin from a hibernation state	77	62	54	M6
SD I/F	S_CLK_0	SD memory card interface SD memory card clock output pin	38	28	23	H3
	S_CMD_0	SD memory card interface SD memory card command output	41	31	26	H6
	S_DATA1_0	SD memory card interface SD memory card data bus	36	26	21	H2
	S_DATA0_0		37	27	22	J1
	S_DATA3_0		42	32	27	J5
	S_DATA2_0		43	33	28	J4
	S_CD_0	SD memory card interface SD memory card detection pin	45	35	30	J2
	S_WP_0	SD memory card interface SD memory card write protection	44	34	29	J3
I ² S	I2SMCLK0_0	I ² S external clock pin	51	41	-	L2
	I2SDO0_0	I ² S serial transition data output pin	52	42	-	L3
	I2SWS0_0	I ² S frame synchronization signal pin	53	43	-	M2
	I2SDI0_0	I ² S serial received data input pin	34	24	-	G6
	I2SCK0_0	I ² S bit clock pin	35	25	-	H4
High-speed quad SPI	Q_SCK_0	SPI clock output pin	173	143	-	D10
	Q_IO0_0	SPI data input/output pin	172	142	-	C10
	Q_IO1_0		171	141	-	B10
	Q_IO2_0		170	140	-	D11
	Q_IO3_0		169	139	-	C11
	Q_CS0_0	SPI chip select output pin	174	144	-	B9
	Q_CS1_0		175	-	-	-
	Q_CS2_0		176	-	-	-

Type	Circuit	Remarks
L		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -8 \text{ mA}$, $I_{OL} = 8 \text{ mA}$ • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.
N		• CMOS level output • CMOS level hysteresis input • 5V tolerant • Pull-up resistor control • Standby mode control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ (GPIO) • $I_{OL} = 20 \text{ mA}$ (Fast mode Plus) • Available to control of PZR register (pseudo-open drain control) • For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856). • When this pin is used as an I²C pin, the digital output P-ch transistor is always off.

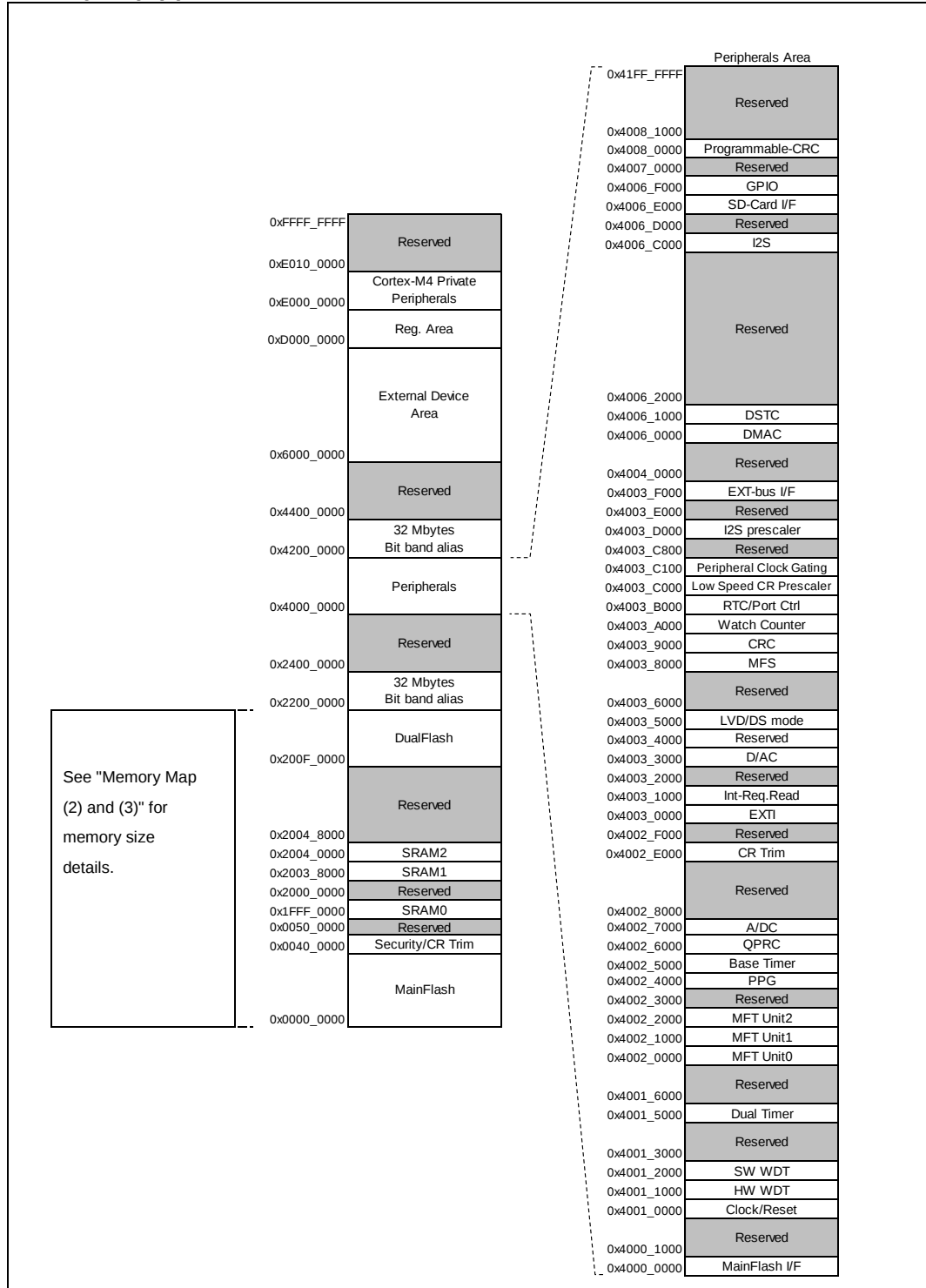
Type	Circuit	Remarks
O		• CMOS level output • CMOS level hysteresis input • 5 V tolerant • Pull-up resistor control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • Available to control of PZR register (pseudo-open drain control) • For PZR registers, refer to GPIO in the "FM4 Family Peripheral Manual Main Part (002-04856)". • For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856). •
P		• CMOS level output • CMOS level hysteresis input • Pull-up resistor control • Pull-up resistor: approximately 50 kΩ • $I_{OH} = -4 \text{ mA}$, $I_{OL} = 4 \text{ mA}$ • For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).

9. Memory Size

See Memory size in 1. Product Lineup to confirm the memory size.

10. Memory Map

Memory Map (1)



12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage ^{*1,*2}	V _{CC}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Power supply voltage (VBAT) ^{*1,*3}	V _{BAT}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Analog power supply voltage ^{*1,*4}	AV _{CC}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Analog reference voltage ^{*1,*4}	AV _{RH}	V _{SS} - 0.5	V _{SS} + 6.5	V	
Input voltage ^{*1}	V _I	V _{SS} - 0.5	V _{CC} + 0.5 (≤ 6.5 V)	V	
		V _{SS} - 0.5	V _{SS} + 6.5	V	5V tolerant
Analog pin input voltage ^{*1}	V _{IA}	V _{SS} - 0.5	AV _{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage ^{*1}	V _O	V _{SS} - 0.5	V _{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current ^{*5}	I _{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	10 mA type
			20	mA	12 mA type
			22.4	mA	I ² C Fm+
L level average output current ^{*6}	I _{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			10	mA	10 mA type
			12	mA	12 mA type
			20	mA	I ² C Fm+
L level total maximum output current	∑I _{OL}	-	100	mA	
L level total maximum output current ^{*7}	∑I _{OLAV}	-	50	mA	
H level maximum output current ^{*5}	I _{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	10 mA type
			- 20	mA	12 mA type
H level average output current ^{*6}	I _{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 10	mA	10 mA type
			- 12	mA	12 mA type
H level total maximum output current	∑I _{OH}	-	- 100	mA	
H level total average output current ^{*7}	∑I _{OHAV}	-	- 50	mA	
Power consumption	P _D	-	200	mW	
Storage temperature	T _{STG}	- 55	+ 150	°C	

1: These parameters are based on the condition that V_{SS} = AV_{SS} = 0.0 V.

2: V_{CC} must not drop below V_{SS} - 0.5 V.

3: V_{BAT} must not drop below V_{SS} - 0.5 V.

4: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

Package thermal resistance and maximum permissible power for each package are shown below.
The operation is guaranteed maximum permissible power or less for semiconductor devices.

Table for Package Thermal Resistance and Maximum Permissible Power

Package	Printed Circuit Board	Thermal Resistance θ_{ja} (°C/W)	Maximum Permissible Power (mW)	
			$T_A = +85\text{ °C}$	$T_A = +105\text{ °C}$
LQS144 (0.5-mm pitch)	Single-layered both sides	48	833	417
	4 layers	33	1212	606
LQP176 (0.5-mm pitch)	Single-layered both sides	45	889	444
	4 layers	31	1290	645
LQQ216 (0.4-mm pitch)	Single-layered both sides	46	870	435
	4 layers	32	1250	625
LBE192 (0.8-mm pitch)	Single-layered both sides	-	-	-
	4 layers	35	1143	571

WARNING:

- The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges. Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
- No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

When Using High-Speed Synchronous Serial Chip Select (SCINV = 1, CSLVL = 0)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t _{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↓ hold time	t _{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t _{CSDI}		(*3)-20 +5t _{CYCP}	(*3)+20 +5t _{CYCP}	(*3)-20 +5t _{CYCP}	(*3)+20 +5t _{CYCP}	ns
SCS↑→SCK↑ setup time	t _{CSSE}	External shift clock operation	3t _{CYCP} +15	-	3t _{CYCP} +15	-	ns
SCK↓→SCS↓ hold time	t _{CSHE}		0	-	0	-	ns
SCS deselect time	t _{CSDE}		3t _{CYCP} +15	-	3t _{CYCP} +15	-	ns
SCS↑→SOT delay time	t _{DSE}		-	40	-	40	ns
SCS↓→SOT delay time	t _{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

Notes:

- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).
- When the external load capacitance C_L = 30 pF.

12.5 12-bit A/D Converter

Electrical Characteristics for the A/D Converter

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = AV_{RL} = 0V$)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	12	bit	
Integral nonlinearity	-	-	- 4.5	-	+ 4.5	LSB	AVRH = 2.7 V to 5.5 V
Differential nonlinearity	-	-	- 2.5	-	+ 2.5	LSB	
Zero transition voltage	V_{ZT}	ANxx	- 15	-	+ 15	mV	
Full-scale transition voltage	V_{FST}	ANxx	AVRH - 15 AVCC - 15	- -	AVRH + 15 AVCC + 15	mV mV	
Conversion time	-	-	0.5 ^{*1}	-	-	μs	AVCC ≥ 4.5 V
Sampling time *2	t_s	-	0.15	-	10	μs	AVCC ≥ 4.5 V
			0.3	-			AVCC < 4.5 V
Compare clock cycle *3	t_{CCK}	-	25	-	1000	ns	AVCC ≥ 4.5 V
			50	-	1000		AVCC < 4.5 V
State transition time to operation permission	t_{STT}	-	-	-	1.0	μs	
Power supply current (analog + digital)	-	AVCC	-	0.69	0.92	mA	A/D 1 unit operation
			-	1.3	22	μA	When A/D stop
Reference power supply current (AVRH)	-	AVRH	-	1.1	1.97	mA	A/D 1 unit operation AVRH = 5.5 V
			-	0.3	6.3	μA	When A/D stop
Analog input capacity	C_{AIN}	-	-	-	12.05	pF	
Analog input resistance	R_{AIN}	-	-	-	1.2	kΩ	AVCC ≥ 4.5 V
					1.8		AVCC < 4.5 V
Interchannel disparity	-	-	-	-	4	LSB	
Analog port input leak current	-	ANxx	-	-	5	μA	
Analog input voltage	-	ANxx	AVSS	-	AVRH	V	
			AVSS	-	AVCC	V	
Reference voltage	-	AVRH	4.5	-	AVCC	V	Tcck < 50 ns
			2.7	-	AVCC		Tcck ≥ 50 ns
	-	AVRL	AVSS	-	AVSS	V	

1: The conversion time is the value of sampling time (t_s) + compare time (t_c).

The condition of the minimum conversion time is when the value of $T_s = 150$ ns and $T_c = 350$ ns ($AV_{CC} \geq 4.5V$). Ensure that it satisfies the value of sampling time (t_s) and compare clock cycle (t_{CCK}).

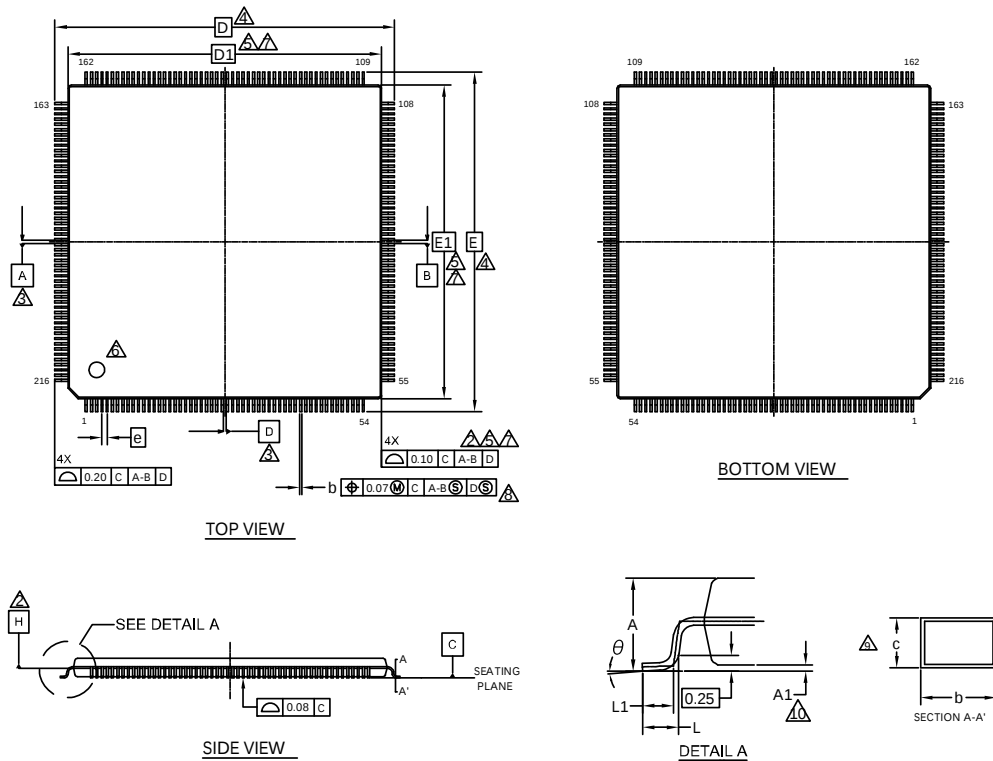
For setting of sampling time and compare clock cycle, see Chapter 1-1: A/D Converter in FM4 Family Peripheral Manual Analog Macro Part (002-04860). The register setting of the A/D converter is reflected by the APB bus clock timing. For more information about the APB bus number to which the A/D converter is connected, see 8. Block Diagram in this data sheet.

The sampling clock and compare clock are set at base clock (HCLK).

2: A necessary sampling time changes by external impedance. Ensure that it sets the sampling time to satisfy (Equation 1).

3: The compare time (t_c) is the value of (Equation 2).

Package Type	Package Code
LQFP 216	LQQ 216



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.13	0.18	0.23
c	0.09	—	0.20
D	26.00 BSC.		
D1	24.00 BSC.		
e	0.40 BSC.		
E	26.00 BSC.		
E1	24.00 BSC.		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

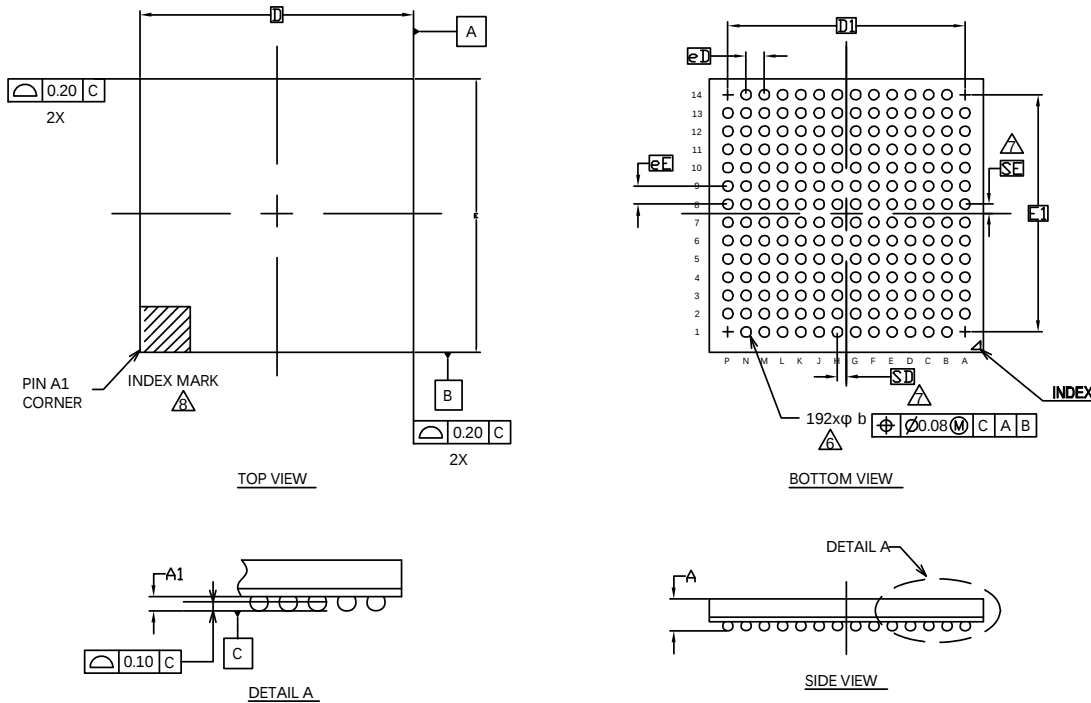
NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
- DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
- TO BE DETERMINED AT SEATING PLANE C.
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
- DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
- REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS, DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS, BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
- DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBER PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
- THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
- A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15153 **

PACKAGE OUTLINE, 216 LEAD LQFP
24.0X24.0X1.7 MM LQQ216 REV**

Package Type	Package Code
PFBGA 192	LBE 192



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.45
A1	0.25	0.35	0.45
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E1	10.40 BSC		
MD	14		
ME	14		
n	192		
Φb	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD/SE	0.40 BSC		

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-13493 **

PACKAGE OUTLINE, 192 BALL FBGA
12.00X12.00X1.45 MM LBE192 REV**