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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I ² C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c19j0agv2000a

■ LIN

- LIN protocol Rev.2.1 supported
- Full-duplex double buffer
- Master/slave mode supported
- LIN break field generation (can change to 13- to 16-bit length)
- LIN break delimiter generation (can change to 1- to 4-bit length)
- Various error detect functions available (parity errors, framing errors, and overrun errors)

■ I²C

- Standard mode (Max 100 kbps)/Fast mode (Max 400 kbps) supported
- Fast mode Plus (Fm+) (Max 1000 kbps, only for ch 3 = ch A and ch 7 = ch B) supported

DMA Controller (Eight Channels)

DMA controller has an independent bus, so the CPU and DMA controller can process simultaneously.

- Eight independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 GB)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System Data Transfer Controller; 256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the descriptor system and, following the specified contents of the descriptor that has already been constructed on the memory, can access directly the memory/peripheral device and perform the data-transfer operation.

It supports the software activation, the hardware activation, and the chain activation functions.

A/D Converter (Max 32 Channels)

- 12-bit A/D Converter
 - Successive approximation type
 - Built-in three units
 - Conversion time: 0.5 μ s at 5 V
 - Priority conversion available (priority at two levels)
 - Scanning conversion mode
 - Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for priority conversion: 4 steps)

D/A Converter (Max two channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 16 channels)

Operation mode is selected from the following for each channel:

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals; moreover, the port relocate function is built in. It can set the I/O port to which the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in port-relocate function
- Up to 120 high-speed general-purpose I/O ports in 144-pin package
- Some pins 5 V tolerant I/O.
See "4. Pin Descriptions" and "5. I/O Circuit Type" for the corresponding pins.

Multi-function Timer (Max three units)

The multi-function timer is composed of the following blocks:

Minimum resolution: 5.00 ns

- 16-bit free-run timer $\times$ 3 ch/unit
- Input capture $\times$ 4 ch/unit
- Output compare $\times$ 6 ch/unit
- A/D activation compare $\times$ 6 ch/unit
- Waveform generator $\times$ 3 ch/unit
- 16-bit PPG timer $\times$ 3 ch/unit

The following functions can be used to achieve the motor control:

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (motor emergency stop) interrupt function

LQP176

(Top View)

LQFP - 176

Note:

- The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

LQ216

(Top View)

1	VCC	152	VSS
2	PA0RT020_0TIOA8_0IAIN2_0INT00_0MADATA00_0	153	P03
3	PA1RT021_0TIOA9_0IBIN2_0MADATA01_0	154	P02
4	PA2RT022_0TIOA10_0IZIN2_0MADATA02_0	155	VCC
5	PA3RT023_0TIOA11_0MADATA03_0	156	P01NMIXMKWUP0
6	PA4RT024_0TIOA12_0MADATA04_0	157	P01ADT0_0I0H0_0INT07_0ICROUT_0
7	PASISIN1_0RT025_0TIOA13_0INT01_0MADATA05_0	158	P01AN230T08_0INT08_0
8	PA6ISOT1_0IT026_0TIOA14_0MADATA06_0	159	P01AN230T08_0INT08_0
9	PA7ISCK1_0IC20_0MADATA07_0	160	P01AN230T08_0INT08_0
10	PS0ISCK2_0RT020_0TIOA8_0MADATA16_0	161	P01AN230T08_0INT08_0
11	PS1ISCK3_0RT021_0TIOA9_0MADATA17_0	162	P01AN230T08_0INT08_0
12	PS2RT022_0TIOA10_0MADATA18_0	163	P01AN230T08_0INT08_0
13	PS2RT022_0TIOA10_0MADATA18_0	164	P01AN230T08_0INT08_0
14	PASISIN7_0IC21_0INT02_0MADATA08_0	165	P01AN230T08_0INT08_0
15	PASISOT7_0IC22_0MADATA09_0	166	P01AN230T08_0INT08_0
16	PAASISCK7_0IC23_0MADATA10_0	167	P01AN230T08_0INT08_0
17	PABISCK7_0IC23_0INT03_0MADATA11_0	168	P01AN230T08_0INT08_0
18	PAISCK571_0TIOB8_0IAIN3_0MADATA12_0	169	P01AN230T08_0INT08_0
19	PASISIN15_0TIOA13_0INT02_0MADATA19_0	170	P01AN230T08_0INT08_0
20	PS0ISOT15_0TIOA13_0INT02_0MADATA21_0	171	P01AN230T08_0INT08_0
21	PS6ISCK15_0TIOB8_0INT08_0MADATA22_0	172	P01AN230T08_0INT08_0
22	PS7IC08_0TIOB1_0MADATA23_0	173	P01AN230T08_0INT08_0
23	PADISCK3_0TIOB9_0IBIN3_0MADATA13_0	174	P01AN230T08_0INT08_0
24	PAEADT0_0SOT1_0TIOB8_0I0H0_0MADATA14_0	175	P01AN230T08_0INT08_0
25	PAFISIN2_0TIOB1_0INT1_0MADATA15_0	176	P01AN230T08_0INT08_0
26	PS8ISIN11_0IC01_0TIOB2_0INT02_0MADATA24_0	177	P01AN230T08_0INT08_0
27	PS9ISOT11_0IC02_0TIOB3_0MADATA25_0	178	P01AN230T08_0INT08_0
28	PSAISCK11_0IC03_0TIOB4_0MADATA26_0	179	P01AN230T08_0INT08_0
29	PSBIFRICK_0TIOB5_0MADATA27_0	180	P01AN230T08_0INT08_0
30	PS0ISIN14_0TIOB12_0INT17_0MADQ0_0	181	P01AN230T08_0INT08_0
31	PS0ISOT14_0TIOB13_0INT18_0MADQ0_0	182	P01AN230T08_0INT08_0
32	PSAADT0_0ISCK4_0IAIN2_0MADKOUT_0	183	P01AN230T08_0INT08_0
33	PSCTIOA11_2MADATA28_0RTIC0_0ISUBOUT_0	184	P01AN230T08_0INT08_0
34	PS0TIOA13_2INT03_0MADQ2_0IS2SD0_0	185	P01AN230T08_0INT08_0
35	PS1TIOB13_2MADQ03_0IS2CK0_0	186	P01AN230T08_0INT08_0
36	PS2BIN2_0INT19_0IS_0DATA1_0	187	P01AN230T08_0INT08_0
37	PS3IFRCK_0I0H2_0IS_0DATA0_0	188	P01AN230T08_0INT08_0
38	PS4ISCK3_0INT00_0IS_0CLK_0	189	P01AN230T08_0INT08_0
39	VCC	190	VCC
40	VSS	191	VSS
41	PS5IC02_0INT01_0IS_0CMD_0	192	P01AN230T08_0INT08_0
42	PS6IC01_0INT02_0IS_0DATA3_0	193	P01AN230T08_0INT08_0
43	PS7IC00_0INT03_0IS_0DATA2_0	194	P01AN230T08_0INT08_0
44	PS8ADT0_0SOT10_0IS_0WP_0	195	P01AN230T08_0INT08_0
45	PS9ISIN2_0TIOA0_0IAIN1_0INT16_0IS_0CD_0MAD24_0	196	P01AN230T08_0INT08_0
46	PSAISOT2_0TIOA1_0IBIN1_0INT17_0MAD23_0	197	P01AN230T08_0INT08_0
47	PSBISCK2_0TIOA2_0IZIN1_0INT18_0MAD22_0MNALE_0	198	P01AN230T08_0INT08_0
48	PS0ISIN13_0RT020_0TIOA1_0INT19_0MAD21_0MNCLE_0	199	P01AN230T08_0INT08_0
49	PS0ISOT1_0TIOA4_0IAIN2_0MAD20_0MNRX_0	200	P01AN230T08_0INT08_0
50	PSISCK13_0RT025_0TIOA5_0MAD19_0MNRX_0	201	P01AN230T08_0INT08_0
51	PS0ISIN10_0TIOB11_2INT01_0MADATA29_0IS2SMCLK_0	202	P01AN230T08_0INT08_0
52	PS0ISOT10_0TIOA12_2MADATA30_0IS2SD0_0	203	P01AN230T08_0INT08_0
53	PS5ISCK10_0TIOB12_2MADATA31_0IS2SW0_0	204	P01AN230T08_0INT08_0
54	VSS	205	VSS
55	VCC	206	VCC
56	PA0ISIN2_0IAIN2_0INT2_0	207	PA0ISIN2_0IAIN2_0INT2_0
57	PA0ISIN2_0IAIN2_0INT2_0	208	PA0ISIN2_0IAIN2_0INT2_0
58	PA0ISIN2_0IAIN2_0INT2_0	209	PA0ISIN2_0IAIN2_0INT2_0
59	PA0ISIN2_0IAIN2_0INT2_0	210	PA0ISIN2_0IAIN2_0INT2_0
60	PA0ISIN2_0IAIN2_0INT2_0	211	PA0ISIN2_0IAIN2_0INT2_0
61	PA0ISIN2_0IAIN2_0INT2_0	212	PA0ISIN2_0IAIN2_0INT2_0
62	PA0ISIN2_0IAIN2_0INT2_0	213	PA0ISIN2_0IAIN2_0INT2_0
63	PA0ISIN2_0IAIN2_0INT2_0	214	PA0ISIN2_0IAIN2_0INT2_0
64	PA0ISIN2_0IAIN2_0INT2_0	215	PA0ISIN2_0IAIN2_0INT2_0
65	PA0ISIN2_0IAIN2_0INT2_0	216	PA0ISIN2_0IAIN2_0INT2_0
66	PA0ISIN2_0IAIN2_0INT2_0	217	PA0ISIN2_0IAIN2_0INT2_0
67	PA0ISIN2_0IAIN2_0INT2_0	218	PA0ISIN2_0IAIN2_0INT2_0
68	PA0ISIN2_0IAIN2_0INT2_0	219	PA0ISIN2_0IAIN2_0INT2_0
69	PA0ISIN2_0IAIN2_0INT2_0	220	PA0ISIN2_0IAIN2_0INT2_0
70	PA0ISIN2_0IAIN2_0INT2_0	221	PA0ISIN2_0IAIN2_0INT2_0
71	PA0ISIN2_0IAIN2_0INT2_0	222	PA0ISIN2_0IAIN2_0INT2_0
72	PA0ISIN2_0IAIN2_0INT2_0	223	PA0ISIN2_0IAIN2_0INT2_0
73	PA0ISIN2_0IAIN2_0INT2_0	224	PA0ISIN2_0IAIN2_0INT2_0
74	PA0ISIN2_0IAIN2_0INT2_0	225	PA0ISIN2_0IAIN2_0INT2_0
75	PA0ISIN2_0IAIN2_0INT2_0	226	PA0ISIN2_0IAIN2_0INT2_0
76	PA0ISIN2_0IAIN2_0INT2_0	227	PA0ISIN2_0IAIN2_0INT2_0
77	PA0ISIN2_0IAIN2_0INT2_0	228	PA0ISIN2_0IAIN2_0INT2_0
78	PA0ISIN2_0IAIN2_0INT2_0	229	PA0ISIN2_0IAIN2_0INT2_0
79	PA0ISIN2_0IAIN2_0INT2_0	230	PA0ISIN2_0IAIN2_0INT2_0
80	PA0ISIN2_0IAIN2_0INT2_0	231	PA0ISIN2_0IAIN2_0INT2_0
81	PA0ISIN2_0IAIN2_0INT2_0	232	PA0ISIN2_0IAIN2_0INT2_0
82	PA0ISIN2_0IAIN2_0INT2_0	233	PA0ISIN2_0IAIN2_0INT2_0
83	PA0ISIN2_0IAIN2_0INT2_0	234	PA0ISIN2_0IAIN2_0INT2_0
84	PA0ISIN2_0IAIN2_0INT2_0	235	PA0ISIN2_0IAIN2_0INT2_0
85	PA0ISIN2_0IAIN2_0INT2_0	236	PA0ISIN2_0IAIN2_0INT2_0
86	PA0ISIN2_0IAIN2_0INT2_0	237	PA0ISIN2_0IAIN2_0INT2_0
87	PA0ISIN2_0IAIN2_0INT2_0	238	PA0ISIN2_0IAIN2_0INT2_0
88	PA0ISIN2_0IAIN2_0INT2_0	239	PA0ISIN2_0IAIN2_0INT2_0
89	PA0ISIN2_0IAIN2_0INT2_0	240	PA0ISIN2_0IAIN2_0INT2_0
90	PA0ISIN2_0IAIN2_0INT2_0	241	PA0ISIN2_0IAIN2_0INT2_0
91	PA0ISIN2_0IAIN2_0INT2_0	242	PA0ISIN2_0IAIN2_0INT2_0
92	PA0ISIN2_0IAIN2_0INT2_0	243	PA0ISIN2_0IAIN2_0INT2_0
93	PA0ISIN2_0IAIN2_0INT2_0	244	PA0ISIN2_0IAIN2_0INT2_0
94	PA0ISIN2_0IAIN2_0INT2_0	245	PA0ISIN2_0IAIN2_0INT2_0
95	PA0ISIN2_0IAIN2_0INT2_0	246	PA0ISIN2_0IAIN2_0INT2_0
96	PA0ISIN2_0IAIN2_0INT2_0	247	PA0ISIN2_0IAIN2_0INT2_0
97	PA0ISIN2_0IAIN2_0INT2_0	248	PA0ISIN2_0IAIN2_0INT2_0
98	PA0ISIN2_0IAIN2_0INT2_0	249	PA0ISIN2_0IAIN2_0INT2_0
99	PA0ISIN2_0IAIN2_0INT2_0	250	PA0ISIN2_0IAIN2_0INT2_0
100	PA0ISIN2_0IAIN2_0INT2_0	251	PA0ISIN2_0IAIN2_0INT2_0
101	PA0ISIN2_0IAIN2_0INT2_0	252	PA0ISIN2_0IAIN2_0INT2_0
102	PA0ISIN2_0IAIN2_0INT2_0	253	PA0ISIN2_0IAIN2_0INT2_0
103	PA0ISIN2_0IAIN2_0INT2_0	254	PA0ISIN2_0IAIN2_0INT2_0
104	PA0ISIN2_0IAIN2_0INT2_0	255	PA0ISIN2_0IAIN2_0INT2_0
105	PA0ISIN2_0IAIN2_0INT2_0	256	PA0ISIN2_0IAIN2_0INT2_0
106	PA0ISIN2_0IAIN2_0INT2_0	257	PA0ISIN2_0IAIN2_0INT2_0
107	PA0ISIN2_0IAIN2_0INT2_0	258	PA0ISIN2_0IAIN2_0INT2_0
108	PA0ISIN2_0IAIN2_0INT2_0	259	PA0ISIN2_0IAIN2_0INT2_0
109	PA0ISIN2_0IAIN2_0INT2_0	260	PA0ISIN2_0IAIN2_0INT2_0
110	PA0ISIN2_0IAIN2_0INT2_0	261	PA0ISIN2_0IAIN2_0INT2_0
111	PA0ISIN2_0IAIN2_0INT2_0	262	PA0ISIN2_0IAIN2_0INT2_0
112	PA0ISIN2_0IAIN2_0INT2_0	263	PA0ISIN2_0IAIN2_0INT2_0
113	PA0ISIN2_0IAIN2_0INT2_0	264	PA0ISIN2_0IAIN2_0INT2_0
114	PA0ISIN2_0IAIN2_0INT2_0	265	PA0ISIN2_0IAIN2_0INT2_0
115	PA0ISIN2_0IAIN2_0INT2_0	266	PA0ISIN2_0IAIN2_0INT2_0
116	PA0ISIN2_0IAIN2_0INT2_0	267	PA0ISIN2_0IAIN2_0INT2_0
117	PA0ISIN2_0IAIN2_0INT2_0	268	PA0ISIN2_0IAIN2_0INT2_0
118	PA0ISIN2_0IAIN2_0INT2_0	269	PA0ISIN2_0IAIN2_0INT2_0
119	PA0ISIN2_0IAIN2_0INT2_0	270	PA0ISIN2_0IAIN2_0INT2_0
120	PA0ISIN2_0IAIN2_0INT2_0	271	PA0ISIN2_0IAIN2_0INT2_0
121	PA0ISIN2_0IAIN2_0INT2_0	272	PA0ISIN2_0IAIN2_0INT2_0
122	PA0ISIN2_0IAIN2_0INT2_0	273	PA0ISIN2_0IAIN2_0INT2_0
123	PA0ISIN2_0IAIN2_0INT2_0	274	PA0ISIN2_0IAIN2_0INT2_0
124	PA0ISIN2_0IAIN2_0INT2_0	275	PA0ISIN2_0IAIN2_0INT2_0
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131	PA0ISIN2_0IAIN2_0INT2_0	282	PA0ISIN2_0IAIN2_0INT2_0
132	PA0ISIN2_0IAIN2_0INT2_0	283	PA0ISIN2_0IAIN2_0INT2_0
133	PA0ISIN2_0IAIN2_0INT2_0	284	PA0ISIN2_0IAIN2_0INT2_0
134	PA0ISIN2_0IAIN2_0INT2_0	285	PA0ISIN2_0IAIN2_0INT2_0
135	PA0ISIN2_0IAIN2_0INT2_0	286	PA0ISIN2_0IAIN2_0INT2_0
136	PA0ISIN2_0IAIN2_0INT2_0	287	PA0ISIN2_0IAIN2_0INT2_0
137	PA0ISIN2_0IAIN2_0INT2_0	288	PA0ISIN2_0IAIN2_0INT2_0
138	PA0ISIN2_0IAIN2_0INT2_0	289	PA0ISIN2_0IAIN2_0INT2_0
139	PA0ISIN2_0IAIN2_0INT2_0	290	PA0ISIN2_0IAIN2_0INT2_0
140	PA0ISIN2_0IAIN2_0INT2_0	291	PA0ISIN2_0IAIN2_0INT2_0
141	PA0ISIN2_0IAIN2_0INT2_0	292	PA0ISIN2_0IAIN2_0INT2_0
142	PA0ISIN2_0IAIN2_0INT2_0	293	PA0ISIN2_0IAIN2_0INT2_0
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147	PA0ISIN2_0IAIN2_0INT2_0	298	PA0ISIN2_0IAIN2_0INT2_0
148	PA0ISIN2_0IAIN2_0INT2_0	299	PA0ISIN2_0IAIN2_0INT2_0
149	PA0ISIN2_0IAIN2_0INT2_0	300	PA0ISIN2_0IAIN2_0INT2_0
150	PA0ISIN2_0IAIN2_0INT2_0	301	PA0ISIN2_0IAIN2_0INT2_0
151	PA0ISIN2_0IAIN2_0INT2_0	302	PA0ISIN2_0IAIN2_0INT2_0
152	PA0ISIN2_0IAIN2_0INT2_0	303	PA0ISIN2_0IAIN2_0INT2_0
153	PA0ISIN2_0IAIN2_0INT2_0	304	PA0ISIN2_0IAIN2_0INT2_0
154	PA0ISIN2_0IAIN2_0INT2_0	305	PA0ISIN2_0IAIN2_0INT2_0
155	PA0ISIN2_0IAIN2_0INT2_0	306	PA0ISIN2_0IAIN2_0INT2_0
156	PA0ISIN2_0IAIN2_0INT2_0	307	PA0ISIN2_0IAIN2_0INT2_0
157	PA0ISIN2_0IAIN2_0INT2_0	308	PA0ISIN2_0IAIN2_0INT2_0
158	PA0ISIN2_0IAIN2_0INT2_0	309	PA0ISIN2_0IAIN2_0INT2_0
159	PA0ISIN2_0IAIN2_0INT2_0	310	PA0ISIN2_0IAIN2_0INT2_0
160	PA0ISIN2_0IAIN2_0INT2_0	311	PA0ISIN2_0IAIN2_0INT2_0
161	PA0ISIN2_0IAIN2_0INT2_0	312	PA0ISIN2_0IAIN2_0INT2_0
162	PA0ISIN2_0IAIN2_0INT2_0	313	PA0ISIN2_0IAIN2_0INT2_0
163	PA0ISIN2_0IAIN2_0INT2_0	314	PA0ISIN2_0IAIN2_0INT2_0
164	PA0ISIN2_0IAIN2_0INT2_0	315	PA0ISIN2_0IAIN2_0INT2_0
165	PA0ISIN2_0IAIN2_0INT2_0	316	PA0ISIN2_0IAIN2_0INT2_0
166	PA0ISIN2_0IAIN2_0INT2_0	317	PA0ISIN2_0IAIN2_0INT2_0
167	PA0ISIN2_0IAIN2_0INT2_0	318	PA0ISIN2_0IAIN2_0INT2_0
168	PA0ISIN2_0IAIN2_0INT2_0	319	PA0ISIN2_0IAIN2_0INT2_0
169	PA0ISIN2_0IAIN2_0INT2_0	320	PA0ISIN2_0IAIN2_0INT2_0
170	PA0ISIN2_0IAIN2_0INT2_0	321	PA0ISIN2_0IAIN2_0INT2_0
171	PA0ISIN2_0IAIN2_0INT2_0	322	PA0ISIN2_0IAIN2_0INT2_0
172	PA0ISIN2_0IAIN2_0INT2_0	323	PA0ISIN2_0IAIN2_0INT2_0
173	PA0ISIN2_0IAIN2_0INT2_0	324	PA0ISIN2_0IAIN2_0INT2_0
174	PA0ISIN2_0IAIN2_0INT2_0	325	PA0ISIN2_0IAIN2_0INT2_0
175	PA0ISIN2_0IAIN2_0INT2_0	326	PA0ISIN2_0IAIN2_0INT2_0
176	PA0ISIN2_0IAIN2_0INT2_0	327	PA0ISIN2_0IAIN2_0INT2_0
177	PA0ISIN2_0IAIN2_0INT2_0	328	PA0ISIN2_0IAIN2_0INT2_0
178	PA0ISIN2_0IAIN2_0INT2_0	329	PA0ISIN2_0IAIN2_0INT2_0
179	PA0ISIN2_0IAIN2_0INT2_0	330	PA0ISIN2_0IAIN2_0INT2_0
180	PA0ISIN2_0IAIN2_0INT2_0	331	PA0ISIN2_0IAIN2_0INT2_0
181	PA0ISIN2_0IAIN2_0INT2_0	332	PA0ISIN2_0IAIN2_0INT2_0
182	PA0ISIN2_0IAIN2_0INT2_0	333	PA0ISIN2_0IAIN2_0INT2_0
183	PA0ISIN2_0IAIN2_0INT2_0	334	PA0ISIN2_0IAIN2_0INT2_0
184	PA0ISIN2_0IAIN2_0INT2_0	335	PA0ISIN2_0IAIN2_0INT2_0
185	PA0ISIN2_0IAIN2_0INT2_0	336	PA0ISIN2_0IAIN2_0INT2_0
186	PA0ISIN2_0IAIN2_0INT2_0	337	PA0ISIN2_0IAIN2_0INT2_0
187	PA0ISIN2_0IAIN2_0INT2_0	338	PA0ISIN2_0IAIN2_0INT2_0
188	PA0ISIN2_0IAIN2_0INT2_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
93	78	62	N10	P77	E	I
				SCK8_0		
				(SCL8_0)		
				TIOB5_0		
				ZIN1_0		
94	-	-	-	MAD06_0	E	I
				PF8		
				SCS70_1		
				DTT11X_1		
				AIN1_1		
95	-	-	-	PF9	E	I
				SCS71_1		
				IC10_1		
				BIN1_1		
96	79	63	L10	P78	E	K
				SIN6_0		
				IC10_0		
				INT21_0		
97	80	64	K10	MAD07_0	L	I
				P79		
				SOT6_0		
				(SDA6_0)		
98	81	65	M10	IC11_0	L	I
				MAD08_0		
				P7A		
				SCK6_0		
99	82	66	N11	(SCL6_0)	R	J
				IC12_0		
				MAD09_0		
				P7B		
100	83	67	M11	DA1	R	J
				SCS60_0		
				IC13_0		
				INT22_0		
101	-	-	-	P7C	E	I
				DA0		
				SCS61_0		
				INT04_1		
102	-	-	-	PFA	E	K
				SCK7_1		
				(SCL7_1)		
				IC11_1		
103	-	-	-	ZIN1_1	E	K
				PFB		
				SOT7_1		
				(SDA7_1)		
104	84	68	N13	IC12_1	C	E
				INT07_2		
				PFC		
				SIN7_1		
105	85	69	N12	IC13_1	J	D
				INT06_2		
104	84	68	N13	PE0	C	E
				MD1		
105	85	69	N12	MD0	J	D

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch 7 TIOB pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch 8 TIOB pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch 9 TIOB pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch 10 TIOB pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch 11 TIOB pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch 12 TIOB pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10	General-purpose I/O port 1	114	94	78	L11
	P11		115	95	79	K13
	P12		116	96	80	K12
	P13		117	97	81	K14
	P14		118	98	82	K11
	P15		123	99	83	J13
	P16		124	100	84	J12
	P17		125	101	85	J11
	P18		130	106	86	H9
	P19		131	107	87	H12
	P1A		132	108	88	H14
	P1B		133	109	89	G14
	P1C		134	110	90	H13
	P1D		135	111	91	H11
	P1E		142	116	92	G10
	P1F		143	117	93	G9
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
	P26		152	122	98	E10
	P27		147	121	97	F13
	P28		146	120	96	F12
	P29		145	119	95	F11
	P2A		144	118	94	F10

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I ² C (operation mode 4).	146	120	96	F12
	SOT5_1 (SDA5_1)		171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I ² C (operation mode 4).	145	119	95	F11
	SCK5_1 (SCL5_1)		172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I ² C (operation mode 4).	97	80	64	K10
	SOT6_1 (SDA6_1)		118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I ² C (operation mode 4).	98	81	65	M10
	SCK6_1 (SCL6_1)		126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent this, do the following:

1. Avoid exposure to rapid temperature changes, which can cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
3. When Dry Packages are opened, it is recommended to have humidity between 40% and 70%.
4. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in these aluminum laminate bags for storage.
5. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons, and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ). Wearing of conductive clothing and shoes, and the use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of Styrofoam or other highly static-prone materials for storage of completed board assemblies.

Pin Status Type	Function Group	Power-On Reset or Low-Voltage Detection State	INITX Input State	Device Internal Reset State	Run mode or Sleep mode State	Timer mode, RTC mode, or Stop mode State		Deep Standby RTC mode or Deep Standby Stop mode State		Return from Deep Standby mode State				
		Power Supply Unstable	Power Supply Stable		Power Supply Stable	Power Supply Stable		Power Supply Stable		Power Supply Stable				
		-	INITX=0	INITX=1	INITX=1	INITX=1		INITX=1		INITX=1				
		-	-	-	-	SPL=0	SPL=1	SPL=0	SPL=1	-				
K	External interrupt enable selected	Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected				
	Resource other than above selected	Hi-Z	Hi-Z/ input enabled	Hi-Z/ input enabled			Hi-Z/internal input fixed at 0							
	GPIO selected													
L	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled				
	Resource other than above selected		Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Hi-Z/internal input fixed at 0	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected			
	GPIO selected													
M	Analog input selected	Hi-Z	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled	Hi-Z/ internal input fixed at 0/ analog input enabled				
	External interrupt enable selected		Setting disabled	Setting disabled	Setting disabled	Maintain previous state	Maintain previous state	Maintain previous state	GPIO selected, internal input fixed at 0	Hi-Z/internal input fixed at 0	GPIO selected			
	Resource other than above selected							Hi-Z/internal input fixed at 0						
	GPIO selected													

12.2 Recommended Operating Conditions

Parameter		Symbol	Conditions	Value		Unit	Remarks
				Min	Max		
Power supply voltage		V _{CC}	-	2.7 *3	5.5	V	
Power supply voltage (VBAT)		V _{BAT}	-	1.65	5.5	V	
Analog power supply voltage		AV _{CC}	-	2.7	5.5	V	AV _{CC} = V _{CC}
Analog reference voltage		AVRH	-	*2	AV _{CC}	V	
		AVRL	-	AV _{SS}	AV _{SS}	V	
Operating temperature	Junction temperature	T _J	-	- 40	+ 125	°C	
	Ambient temperature	T _A	-	-40	*1	°C	

- 1: The maximum temperature of the ambient temperature (T_A) can guarantee a range that does not exceed the junction temperature (T_J).

The calculation formula of the ambient temperature (T_A) is:

$$T_A (\text{Max}) = T_J (\text{Max}) - P_d (\text{Max}) \times \theta_{JA}$$

P_d: Power dissipation (W)

θ_{JA}: Package thermal resistance (°C/W)

$$P_d (\text{Max}) = V_{CC} \times I_{CC} (\text{Max}) + \sum (I_{OL} \times V_{OL}) + \sum ((V_{CC} - V_{OH}) \times (-I_{OH}))$$

I_{OL}: L level output current

I_{OH}: H level output current

V_{OL}: L level output voltage

V_{OH}: H level output voltage

- 2: The minimum value of analog reference voltage depends on the value of compare clock cycle (T_{ck}). See 12.5. 12-bit A/D Converter for the details.
- 3: For the voltage range between V_{CC} (min) and the low voltage detection reset (VDH), the MCU must be clocked from either the High-speed CR or the low-speed CR.

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency* ⁴	Value		Unit	Remarks	
						Typ* ¹	Max* ²			
Power supply current	I _{CC}	VCC	Normal operation * ⁷ ,* ⁸ (PLL)	* ⁵	200 MHz	117	224	mA	* ³ When all peripheral clocks are on	
					192 MHz	113	219	mA		
					180 MHz	106	211	mA		
				* ⁶	160 MHz	95	197	mA		* ³ When all peripheral clocks are off
					144 MHz	86	186	mA		
					120 MHz	73	169	mA		
					100 MHz	61	155	mA		
					80 MHz	50	140	mA		
					60 MHz	39	126	mA		
					40 MHz	27	112	mA		
					20 MHz	16	97	mA		
					8 MHz	8.7	88.9	mA		
					4 MHz	6.4	86.1	mA		
				* ⁵	200 MHz	71	168	mA		
					192 MHz	68	165	mA		
					180 MHz	64	159	mA		
					* ⁶	160 MHz	58	151	mA	
						144 MHz	52	144	mA	
						120 MHz	44	134	mA	
						100 MHz	38	126	mA	
						80 MHz	31	117	mA	
						60 MHz	24	109	mA	
						40 MHz	17	100	mA	
						20 MHz	10	91	mA	
						8 MHz	6.3	86.1	mA	
						4 MHz	5.0	84.5	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory.”

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-8 Typical and Maximum Current Consumption in Stop Mode, Timer Mode and RTC Mode

Parameter	Symbol	Pin Name	Conditions	Frequency	Value		Unit	Remarks	
					Typ*1	Max*2			
Power supply current	I _{CCH}	V _{CC}	Stop mode	-	0.56	3.01	mA	*3, *4 T _A = +25°C	
					-	27.03	mA	*3, *4 T _A = +85°C	
					-	39.92	mA	*3, *4 T _A = +105°C	
	I _{CCT}		Timer mode*5 (main oscillation)	4 MHz	1.40	3.85	mA	*3, *4 T _A = +25°C	
					-	27.87	mA	*3, *4 T _A = +85°C	
					-	40.76	mA	*3, *4 T _A = +105°C	
			Timer mode (built-in High-speed CR)	4 MHz	0.95	3.40	mA	*3, *4 T _A = +25°C	
					-	27.42	mA	*3, *4 T _A = +85°C	
					-	40.31	mA	*3, *4 T _A = +105°C	
			Timer mode*6 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T _A = +25°C	
					-	27.04	mA	*3, *4 T _A = +85°C	
					-	39.93	mA	*3, *4 T _A = +105°C	
			Timer mode (built-in low-speed CR)	100 kHz	0.58	3.03	mA	*3, *4 T _A = +25°C	
					-	27.05	mA	*3, *4 T _A = +85°C	
					-	39.94	mA	*3, *4 T _A = +105°C	
			I _{CCR}	RTC mode*5 (sub oscillation)	32 kHz	0.57	3.02	mA	*3, *4 T _A = +25°C
						-	27.04	mA	*3, *4 T _A = +85°C
						-	39.93	mA	*3, *4 T _A = +105°C

1: V_{CC} = 3.3 V

2: V_{CC} = 5.5 V

3: When all ports are fixed

4: When LVD is off

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

6: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

12.4.6 Operating Conditions of Main PLL (in the Case of Using Built-in High-Speed CR Clock for Input Clock of Main PLL)
 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time ^{*1} (lock up time)	t _{LOCK}	100	-	-	μs	
PLL input clock frequency	f _{PLLI}	3.8	4	4.2	MHz	
PLL multiplication rate	-	50	-	95	multiplier	
PLL macro oscillation clock frequency	f _{PLLO}	190	-	400	MHz	
Main PLL clock frequency ^{*2}	f _{CLKPLL}	-	-	200	MHz	

1: Time from when the PLL starts operating until the oscillation stabilizes

2: For more information about Main PLL clock (CLKPLL), see Chapter 2-1: Clock in FM4 Family Peripheral Manual Main Part (002-04856).

Note:

- The High-speed CR clock (CLKHC) should be set with frequency/temperature trimming to act as the source clock of the Main PLL.

12.4.7 Reset Input Characteristics

 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Typ		
Reset input time	t _{INITX}	INITX	-	500	-	ns	

Synchronous Serial (SPI = 0, SCINV = 1)

 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5 V		V _{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↑→SOT delay time	t _{SHOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↓ setup time	t _{IVSLI}	SCKx, SINx		50	-	30	-	ns
SCK↓→SIN hold time	t _{SLIXI}	SCKx, SINx		0	-	0	-	ns
Serial clock L pulse width	t _{SLSH}	SCKx		2t _{CYCP} - 10	-	2t _{CYCP} - 10	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx	External shift clock operation	t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↑→SOT delay time	t _{SHOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↓ setup time	t _{IVSLE}	SCKx, SINx		10	-	10	-	ns
SCK↓→SIN hold time	t _{SLIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.
- When the external load capacitance C_L = 30 pF.

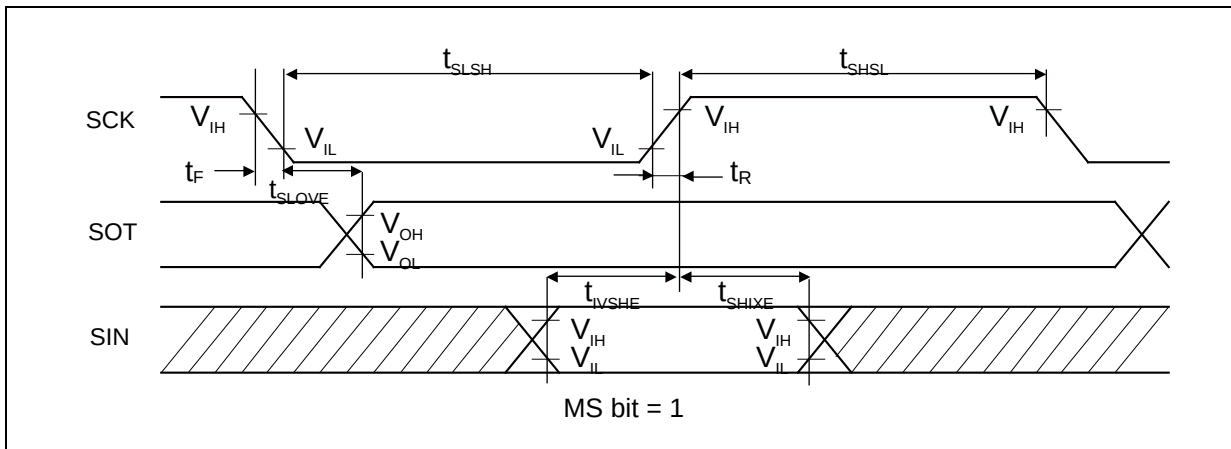
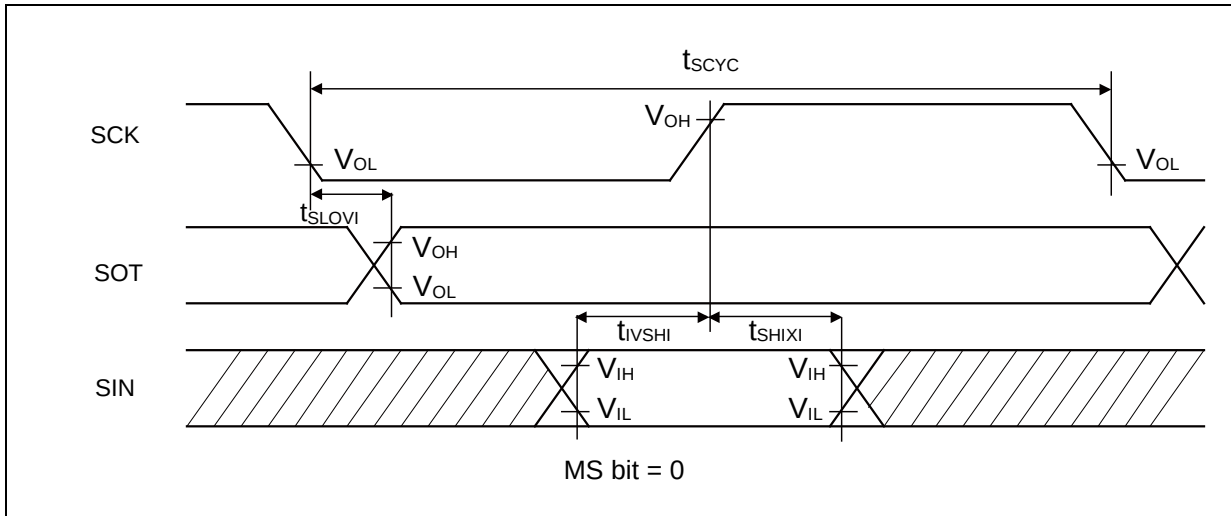
High-Speed Synchronous Serial (SPI = 0, SCINV = 0)

 (V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V _{CC} < 4.5V		V _{CC} ≥ 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t _{SCYC}	SCKx	Internal shift clock operation	4t _{CYCP}	-	4t _{CYCP}	-	ns
SCK↓→SOT delay time	t _{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t _{IVSHI}	SCKx, SINx		14	-	12.5	-	ns
				12.5*				
SCK↑→SIN hold time	t _{SHIXI}	SCKx, SINx		5	-	5	-	ns
Serial clock L pulse width	t _{LSH}	SCKx	External shift clock operation	2t _{CYCP} - 5	-	2t _{CYCP} - 5	-	ns
Serial clock H pulse width	t _{SHSL}	SCKx		t _{CYCP} + 10	-	t _{CYCP} + 10	-	ns
SCK↓→SOT delay time	t _{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t _{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t _{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t _F	SCKx		-	5	-	5	ns
SCK rise time	t _R	SCKx		-	5	-	5	ns

Notes:

- The above characteristics apply to CLK synchronous mode.
- t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.
- These characteristics only guarantee the following pins:
 No chip select: SIN4_0, SOT4_0, SCK4_0
 Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- When the external load capacitance C_L = 30 pF. (For *, when C_L = 10 pF)

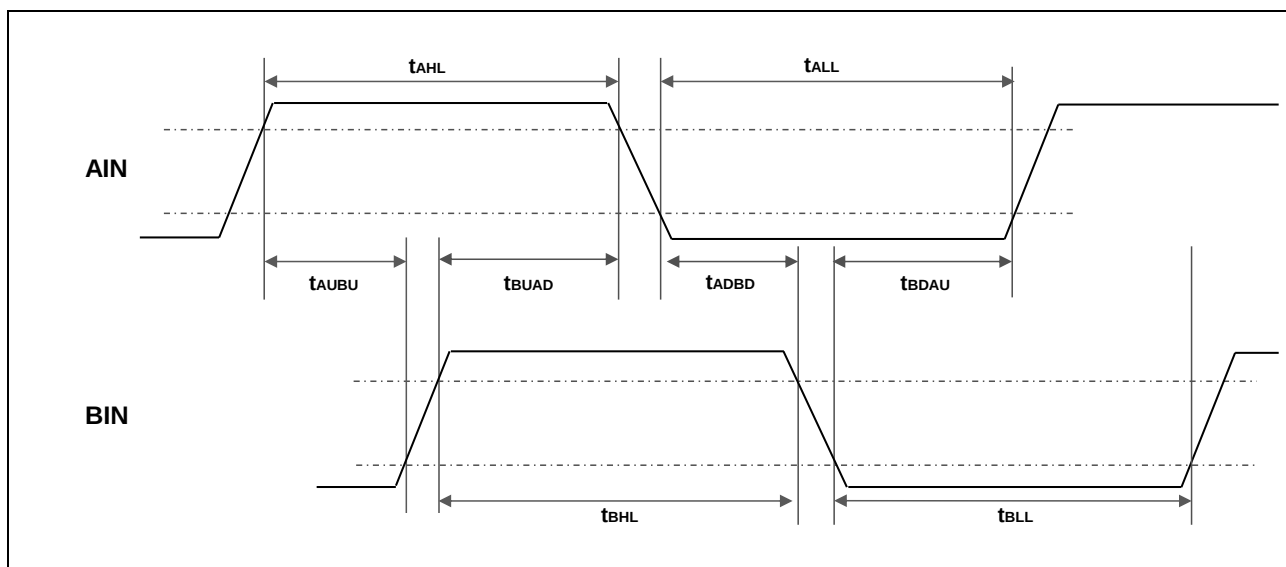


12.4.14 Quadrature Position/Revolution Counter Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+105^{\circ}C$)

Parameter	Symbol	Conditions	Value		Unit
			Min	Max	
AIN pin H width	t_{AHL}	-	$2t_{CYCP}^*$	-	ns
AIN pin L width	t_{ALL}	-			
BIN pin H width	t_{BHL}	-			
BIN pin L width	t_{BLL}	-			
BIN rise time from AIN pin H level	t_{AUBU}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin H level	t_{BUAD}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin L level	t_{ADBD}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin L level	t_{BDAU}	PC_Mode2 or PC_Mode3			
AIN rise time from BIN pin H level	t_{BUAU}	PC_Mode2 or PC_Mode3			
BIN fall time from AIN pin H level	t_{AUBD}	PC_Mode2 or PC_Mode3			
AIN fall time from BIN pin L level	t_{BDAD}	PC_Mode2 or PC_Mode3			
BIN rise time from AIN pin L level	t_{ADBU}	PC_Mode2 or PC_Mode3			
ZIN pin H width	t_{ZHL}	QCR: CGSC = 0			
ZIN pin L width	t_{ZLL}	QCR: CGSC = 0			
AIN/BIN rise and fall time from determined ZIN level	t_{ZABE}	QCR: CGSC = 1			
Determined ZIN level from AIN/BIN rise and fall time	t_{ABEZ}	QCR: CGSC = 1			

*: t_{CYCP} indicates the APB bus clock cycle time except when in Stop mode, in Timer mode. For more information about the APB bus number to which the quadrature position/revolution counter is connected, see 8. Block Diagram in this data sheet.



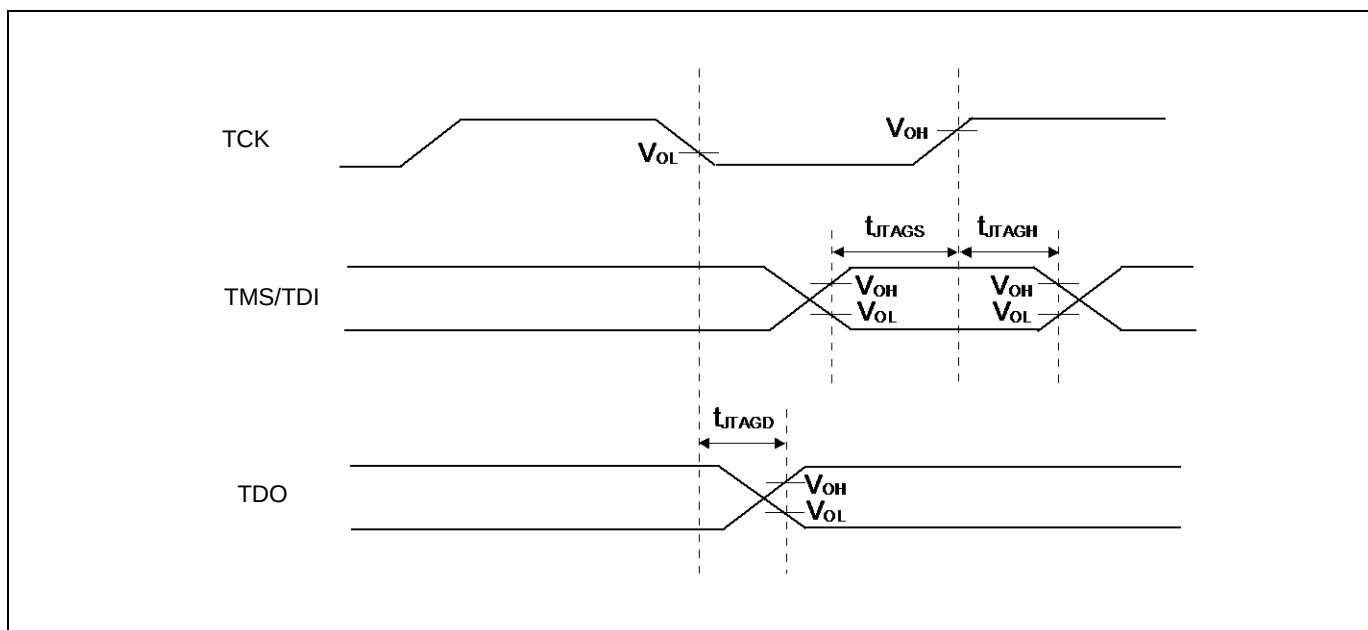
12.4.18 JTAG Timing

($V_{CC} = 2.7V$ to $5.5V$, $V_{SS} = 0V$)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
TMS, TDI setup time	t_{JTAS}	TCK, TMS, TDI	$V_{CC} \geq 4.5 V$ $V_{CC} < 4.5 V$	15	-	ns	
TMS, TDI hold time	t_{JTGH}	TCK, TMS, TDI	$V_{CC} \geq 4.5 V$ $V_{CC} < 4.5 V$	15	-	ns	
TDO delay time	t_{JTGD}	TCK, TDO	$V_{CC} \geq 4.5 V$	-	25	ns	
			$V_{CC} < 4.5 V$	-	45		

Note:

- When the external load capacitance $C_L = 30 pF$.



12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

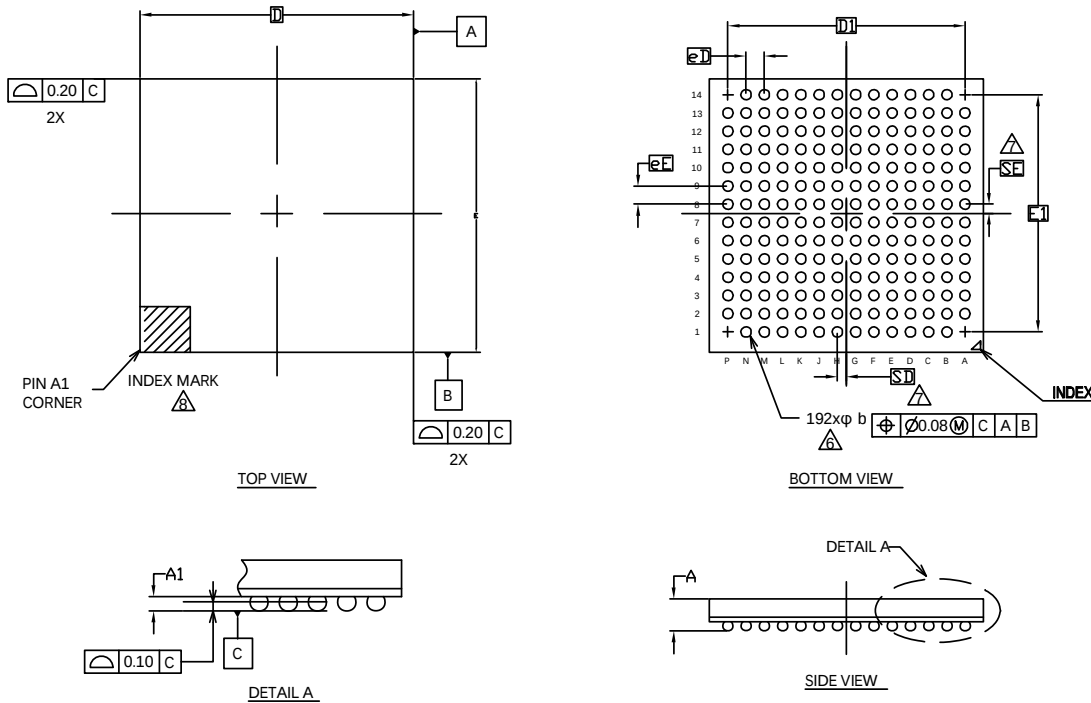
Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t _{LVDW}	-	-	-	6000×t _{CYCP} *	μs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

Package Type	Package Code
PFBGA 192	LBE 192



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.45
A1	0.25	0.35	0.45
D	12.00 BSC		
E	12.00 BSC		
D1	10.40 BSC		
E1	10.40 BSC		
MD	14		
ME	14		
n	192		
Φb	0.35	0.45	0.55
eD	0.80 BSC		
eE	0.80 BSC		
SD/SE	0.40 BSC		

NOTES

- ALL DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS AND TOLERANCES METHODS PER ASME Y14.5-2009. THIS OUTLINE CONFORMS TO JEP95, SECTION 4.5.
- BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-010.
- "e" REPRESENTS THE SOLDER BALL GRID PITCH.
- SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION. SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION. n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
- DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
- "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW. WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0. WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
- A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK. METALLIZED MARK INDENTATION OR OTHER MEANS.
- "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

002-13493 **

PACKAGE OUTLINE, 192 BALL FBGA
12.00X12.00X1.45 MM LBE192 REV**