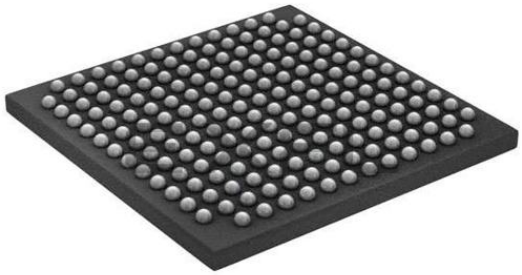

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	152
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	192-LFBGA
Supplier Device Package	192-FBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c1aj0agb1000a

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
84	69	59	J8	P74 SCK9_0 (SCL9_0) TIOB2_0 MAD03_0	E	I
85	70	-	N8	PF2 RTO10_1 (PPG10_1) TIOA6_1 MRASX_0	L	I
86	71	-	M8	PF3 RTO11_1 (PPG10_1) TIOB6_1 INT05_1 MCASX_0	L	K
87	72	-	N9	PF4 RTO12_1 (PPG12_1) TIOA7_1 INT06_1 MSDWEX_0	L	K
88	73	-	P9	PF5 RTO13_1 (PPG12_1) TIOB7_1 INT07_1 MCSX8_0	L	K
89	74	-	M9	PF6 RTO14_1 (PPG14_1) TIOA14_1 INT20_1 MSDCKE_0	L	K
90	75	-	L9	PF7 RTO15_1 (PPG14_1) TIOB14_1 INT21_1 MSDCLK_0	L	K
91	76	60	K9	P75 SIN8_0 TIOB3_0 AIN1_0 INT20_0 MAD04_0	E	K
92	77	61	P10	P76 SOT8_0 (SDA8_0) TIOB4_0 BIN1_0 MAD05_0	E	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
132	108	88	H14	P1A AN10 SCK2_0 (SCL2_0) TIOA4_2 TRACED0	F	N
133	109	89	G14	P1B AN11 SIN12_0 TIOB4_2 INT11_0 TRACED1	F	O
134	110	90	H13	P1C AN12 SOT12_0 (SDA12_0) TIOA5_2 TRACED2	F	N
135	111	91	H11	P1D AN13 SCK12_0 (SCL12_0) TIOB5_2 TRACED3	F	N
136	-	-	-	VSS	-	-
137	-	-	-	VCC	-	-
138	112	-	G13	PB4 AN20 SIN8_1 TIOA11_1 INT10_1 TRACED4	F	O
139	113	-	F14	PB5 AN21 SOT8_1 (SDA8_1) TIOB11_1 INT11_1 TRACED5	F	O
140	114	-	G12	PB6 AN22 SCK8_1 (SCL8_1) TIOA12_1 TRACED6	F	N
141	115	-	G11	PB7 AN23 TIOB12_1 TRACED7	F	N
142	116	92	G10	P1E AN14 TIOA8_1 INT26_1 MAD10_0	F	M

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
154	124	100	E12	P24 AN29 TIOA13_1 MAD18_0	F	L
155	125	101	E13	P23 UHCONX1 AN30 SCK0_0 (SCL0_0) TIOB13_1	F	L
156	126	102	D12	P22 AN31 SOT0_0 (SDA0_0) INT26_0	F	M
157	127	103	D13	P21 ADTG_4 SIN0_0 INT27_0 CROUT_0	I	K
158	128	104	C13	P20 NMIX WKUP0	I	F
159	129	105	E14	VCC	-	-
160	130	106	D14	P82 UDM1	H	R
161	131	107	C14	P83 UDP1	H	R
162	132	108	B14	VSS	-	-
163	133	109	A13	VCC	-	-
164	134	110	B13	P00 TRSTX	E	G
165	135	111	A12	P01 TCK SWCLK	E	G
166	136	112	C12	P02 TDI	E	G
167	137	113	B12	P03 TMS SWDIO	E	G
168	138	114	B11	P04 TDO SWO	E	G
169	139	-	C11	P90 INT12_1 Q_IO3_0	S	K
170	140	-	D11	P91 SIN5_1 INT13_1 Q_IO2_0	S	K
171	141	-	B10	P92 SOT5_1 (SDA5_1) INT14_1 Q_IO1_0	S	K

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 13	TIOA13_0	Base Timer ch 13 TIOA pin	7	7	7	D1
	TIOA13_1		154	124	100	E12
	TIOA13_2		34	24	-	G6
	TIOB13_0	Base Timer ch 13 TIOB pin	31	22	19	G4
	TIOB13_1		155	125	101	E13
	TIOB13_2		35	25	-	H4
Base Timer 14	TIOA14_0	Base Timer ch 14 TIOA pin	183	151	121	D8
	TIOA14_1		89	74	-	M9
	TIOA14_2		204	-	-	-
	TIOB14_0	Base Timer ch 14 TIOB pin	182	150	120	C8
	TIOB14_1		90	75	-	L9
	TIOB14_2		203	-	-	-
Base Timer 15	TIOA15_0	Base Timer ch 15 TIOA pin	187	155	125	B7
	TIOA15_1		78	63	-	K5
	TIOA15_2		206	-	-	-
	TIOB15_0	Base timer ch 15 TIOB pin	186	154	124	F8
	TIOB15_1		79	64	-	K6
	TIOB15_2		205	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
GPIO	P00	General-purpose I/O port 0	164	134	110	B13
	P01		165	135	111	A12
	P02		166	136	112	C12
	P03		167	137	113	B12
	P04		168	138	114	B11
	P08		30	21	18	G3
	P09		31	22	19	G4
	P0A		32	23	20	G5
	P10	General-purpose I/O port 1	114	94	78	L11
	P11		115	95	79	K13
	P12		116	96	80	K12
	P13		117	97	81	K14
	P14		118	98	82	K11
	P15		123	99	83	J13
	P16		124	100	84	J12
	P17		125	101	85	J11
	P18		130	106	86	H9
	P19		131	107	87	H12
	P1A		132	108	88	H14
	P1B		133	109	89	G14
	P1C		134	110	90	H13
	P1D		135	111	91	H11
	P1E		142	116	92	G10
	P1F		143	117	93	G9
	P20	General-purpose I/O port 2	158	128	104	C13
	P21		157	127	103	D13
	P22		156	126	102	D12
	P23		155	125	101	E13
	P24		154	124	100	E12
	P25		153	123	99	E11
	P26		152	122	98	E10
	P27		147	121	97	F13
	P28		146	120	96	F12
	P29		145	119	95	F11
	P2A		144	118	94	F10

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 0	SIN0_0	Multi-function serial interface ch 0 input pin	157	127	103	D13
	SIN0_1		151	-	-	-
	SOT0_0 (SDA0_0)	Multi-function serial interface ch 0 output pin. This pin operates as SOT0 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA0 when it is used in an I²C (operation mode 4).	156	126	102	D12
	SOT0_1 (SDA0_1)		150	-	-	-
	SCK0_0 (SCL0_0)	Multi-function serial interface ch 0 clock I/O pin. This pin operates as SCK0 when it is used in a CSIO (operation mode 2) and as SCL0 when it is used in an I²C (operation mode 4)	155	125	101	E13
	SCK0_1 (SCL0_1)		149	-	-	-
Multi-Function Serial 1	SIN1_0	Multi-function serial interface ch 1 input pin	7	7	7	D1
	SIN1_1		80	65	55	L6
	SOT1_0 (SDA1_0)	Multi-function serial interface ch 1 output pin. This pin operates as SOT1 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA1 when it is used in an I²C (operation mode 4).	8	8	8	D3
	SOT1_1 (SDA1_1)		81	66	56	J6
	SCK1_0 (SCL1_0)	Multi-function serial interface ch 1 clock I/O pin. This pin operates as SCK1 when it is used in a CSIO (operation mode 2) and as SCL1 when it is used in an I²C (operation mode 4).	9	9	9	D4
	SCK1_1 (SCL1_1)		70	55	47	L5
Multi-Function Serial 2	SIN2_0	Multi-function serial interface ch 2 input pin	130	106	86	H9
	SIN2_1		45	35	30	J2
	SOT2_0 (SDA2_0)	Multi-function serial interface ch 2 output pin. This pin operates as SOT2 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA2 when it is used in an I²C (operation mode 4).	131	107	87	H12
	SOT2_1 (SDA2_1)		46	36	31	K1
	SCK2_0 (SCL2_0)	Multi-function serial interface ch 2 clock I/O pin. This pin operates as SCK2 when it is used in a CSIO (operation mode 2) and as SCL2 when it is used in an I²C (operation mode 4).	132	108	88	H14
	SCK2_1 (SCL2_1)		47	37	32	K2

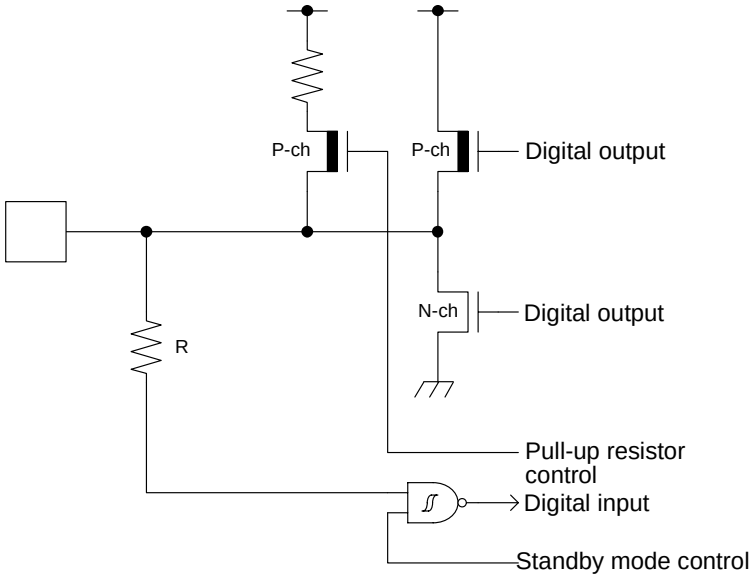
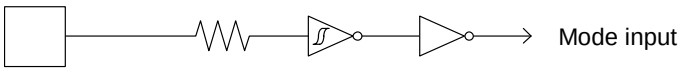
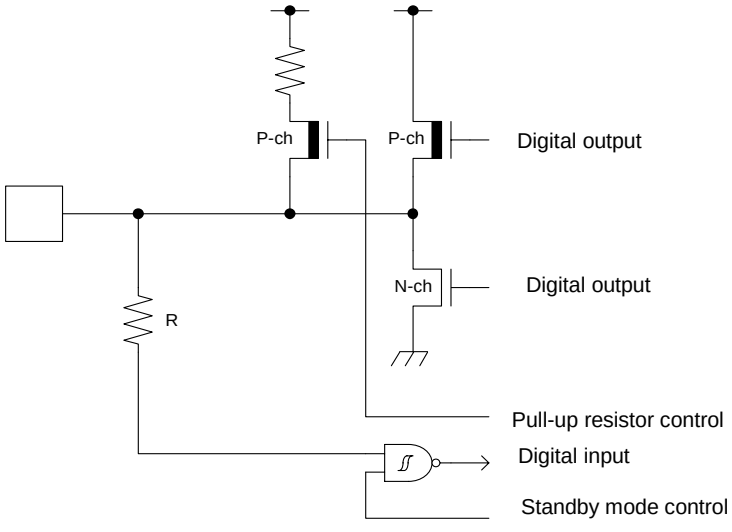
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Timer 0	DTTI0X_0	Input signal controlling waveform generator outputs RTO00 to RTO05 of Multi-Function Timer 0.	44	34	29	J3
	DTTI0X_1		21	-	-	-
	FRCK0_0	16-bit free-run timer ch 0 external clock input pin	37	27	22	J1
	FRCK0_1		29	-	-	-
	IC00_0	16-bit input capture input pin of Multi-Function Timer 0. ICxx describes channel number.	43	33	28	J4
	IC00_1		22	-	-	-
	IC01_0		42	32	27	J5
	IC01_1		26	-	-	-
	IC02_0		41	31	26	H6
	IC02_1		27	-	-	-
	IC03_0		38	28	23	H3
	IC03_1		28	-	-	-
	RTO00_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	45	35	30	J2
	RTO00_1 (PPG00_1)		10	10	-	E2
	RTO01_0 (PPG00_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG00 when it is used in PPG0 output modes.	46	36	31	K1
	RTO01_1 (PPG00_1)		11	11	-	E3
	RTO02_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	47	37	32	K2
	RTO02_1 (PPG02_1)		12	12	-	E4
	RTO03_0 (PPG02_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG02 when it is used in PPG0 output modes.	48	38	33	K3
	RTO03_1 (PPG02_1)		13	-	-	-
	RTO04_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	49	39	34	K4
	RTO04_1 (PPG04_1)		19	-	-	-
	RTO05_0 (PPG04_0)	Waveform generator output pin of Multi-Function Timer 0. This pin operates as PPG04 when it is used in PPG0 output modes.	50	40	35	L1
	RTO05_1 (PPG04_1)		20	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Quadrature Position/ Revolution Counter 0	AIN0_0	QPRC ch 0 AIN input pin	56	46	38	N2
	AIN0_1		65	-	-	-
	AIN0_2		114	94	78	L11
	BIN0_0	QPRC ch 0 BIN input pin	57	47	39	N3
	BIN0_1		66	-	-	-
	BIN0_2		115	95	79	K13
	ZIN0_0	QPRC ch 0 ZIN input pin	58	48	40	M3
	ZIN0_1		67	-	-	-
	ZIN0_2		116	96	80	K12
Quadrature Position/ Revolution Counter 1	AIN1_0	QPRC ch 1 AIN input pin	91	76	60	K9
	AIN1_1		94	-	-	-
	AIN1_2		123	99	83	J13
	BIN1_0	QPRC ch 1 BIN input pin	92	77	61	P10
	BIN1_1		45	-	-	-
	BIN1_2		124	100	84	J12
	ZIN1_0	QPRC ch 1 ZIN input pin	93	78	62	N10
	ZIN1_1		101	-	-	-
	ZIN1_2		125	101	85	J11
Quadrature Position/ Revolution Counter 2	AIN2_0	QPRC ch 2 AIN input pin	2	2	2	B2
	AIN2_1		32	23	20	G5
	AIN2_2		120	-	-	-
	BIN2_0	QPRC ch 2 BIN input pin	3	3	3	C2
	BIN2_1		36	26	21	H2
	BIN2_2		121	-	-	-
	ZIN2_0	QPRC ch 2 ZIN input pin	4	4	4	C3
	ZIN2_1		37	27	22	J1
	ZIN2_2		122	-	-	-
Quadrature Position/ Revolution Counter 3	AIN3_0	QPRC ch 3 AIN input pin	18	17	14	F4
	AIN3_1		45	35	30	J2
	AIN3_2		149	-	-	-
	BIN3_0	QPRC ch 3 BIN input pin	23	18	15	F5
	BIN3_1		46	36	31	K1
	BIN3_2		150	-	-	-
	ZIN3_0	QPRC ch 3 ZIN input pin	24	19	16	F6
	ZIN3_1		47	37	32	K2
	ZIN3_2		151	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Clock	X0	Main clock (oscillation) input pin	106	86	70	P12
	X1	Main clock (oscillation) I/O pin	107	87	71	P13
	X0A	Sub clock (oscillation) input pin	73	58	50	P5
	X1A	Sub clock (oscillation) I/O pin	74	59	51	P6
	CROUT_0	Built-in High-speed CR-oscillation clock output port	157	127	103	D13
	CROUT_1		184	152	122	E8
Analog power	AVCC	A/D converter and D/A converter analog power-supply pin	110	90	74	M13
	AVRL	A/D converter analog reference voltage input pin	112	92	76	L13
	AVRH	A/D converter analog reference voltage input pin	113	93	77	L12
VBAT power	VBAT	VBAT power supply pin Backup power supply (battery etc.) and system power supply	75	60	52	P8
Analog GND	AVSS	A/D converter and D/A converter GND pin	111	91	75	M12
C pin	C	Power supply stabilization capacity pin	62	52	44	P2

Note:

- *While this device contains a Test Access Port (TAP) based on the IEEE 1149.1-2001 JTAG standard, it is not fully compliant to all requirements of that standard. This device may contain a 32-bit device ID that is the same as the 32-bit device ID in other devices with different functionality. The TAP pins may also be configurable for purposes other than access to the TAP controller.*

Type	Circuit	Remarks
I		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・Pull-up resistor control ・Standby mode control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR registers (pseudo-open drain control) ・For PZR registers, refer to GPIO in the FM4 Family Peripheral Manual Main Part (002-04856).
J		CMOS level hysteresis input
K		・CMOS level output ・TTL level hysteresis input ・Pull-up resistor control ・Standby mode control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA

6.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.

2. Discharge of static electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.

3. Corrosive gases, dust, or oil

   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.

4. Radiation, including cosmic radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.

5. Smoke, flame

   CAUTION: Plastic molded devices are flammable and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

Table 12-5 Typical and Maximum Current Consumption in Sleep Operation (PLL), when PCLK0 = PCLK1 = PCLK2 = HCLK/2

Parameter	Symbol	Pin Name	Conditions	Frequency*4	Value		Unit	Remarks
					Typ*1	Max*2		
Power supply current	I_{CCS}	VCC	Sleep operation*5 (PLL)	200 MHz	88	188	mA	*3 When all peripheral clocks are on
				192 MHz	85	184	mA	
				180 MHz	80	178	mA	
				160 MHz	72	164	mA	
				144 MHz	65	156	mA	
				120 MHz	55	144	mA	
				100 MHz	47	134	mA	
				80 MHz	38	124	mA	
				60 MHz	30	114	mA	
				40 MHz	21	104	mA	
				20 MHz	12	93	mA	
				8 MHz	7.4	87.2	mA	
				4 MHz	5.8	85.2	mA	
				200 MHz	44	134	mA	*3 When all peripheral clocks are off
				192 MHz	42	132	mA	
				180 MHz	40	129	mA	
				160 MHz	36	123	mA	
				144 MHz	33	119	mA	
				120 MHz	28	113	mA	
				100 MHz	24	108	mA	
				80 MHz	20	103	mA	
				60 MHz	16	98	mA	
				40 MHz	12	93	mA	
				20 MHz	7.6	87.6	mA	
				8 MHz	5.2	84.7	mA	
				4 MHz	4.4	83.7	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

12.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
H level input voltage (hysteresis input)	V_{IHS}	CMOS hysteresis input pin, MD0, MD1	-	V_{CC}×0.8	-	V_{CC} + 0.3	V	
		MADATAxx	V_{CC} > 3.0 V, V_{CC} ≤ 3.6 V,	2.4	-	V_{CC} + 0.3	V	At External Bus
		5V tolerant input pin	-	V_{CC}×0.8	-	V_{SS} + 5.5	V	
		Input pin doubled as I^2C Fm+	-	V_{CC}×0.7	-	V_{SS} + 5.5	V	
		TTL Schmitt input pin	-	2.0	-	V_{CC}+0.3	V	
L level input voltage (hysteresis input)	V_{ILS}	CMOS hysteresis input pin, MD0, MD1	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		5V tolerant input pin	-	V_{SS} - 0.3	-	V_{CC}×0.2	V	
		Input pin doubled as I^2C Fm+	-	V_{SS}	-	V_{CC}×0.3	V	
		TTL Schmitt input pin	-	V_{SS} - 0.3	-	0.8	V	
H level output voltage	V_{OH}	4 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 2 mA					
		8 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 8 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 4 mA					
		10 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 10 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		12 mA type	V_{CC} ≥ 4.5 V, I_{OH} = - 12 mA	V_{CC} - 0.5	-	V_{CC}	V	
			V_{CC} < 4.5 V, I_{OH} = - 8 mA					
		The pin doubled as I^2C Fm+	V_{CC} ≥ 4.5 V, I_{OH} = - 4 mA	V_{CC} - 0.5	-	V_{CC}	V	At GPIO
			V_{CC} < 4.5V, I_{OH} = - 3 mA					

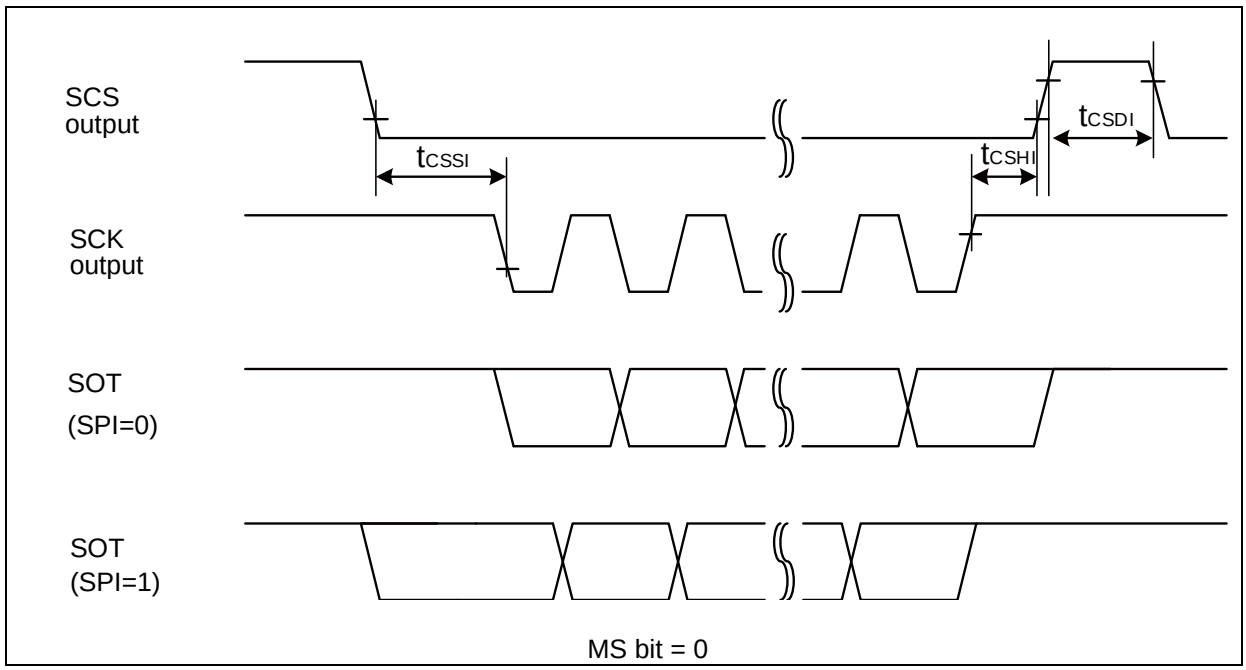
Synchronous Serial (SPI = 1, SCINV = 1)

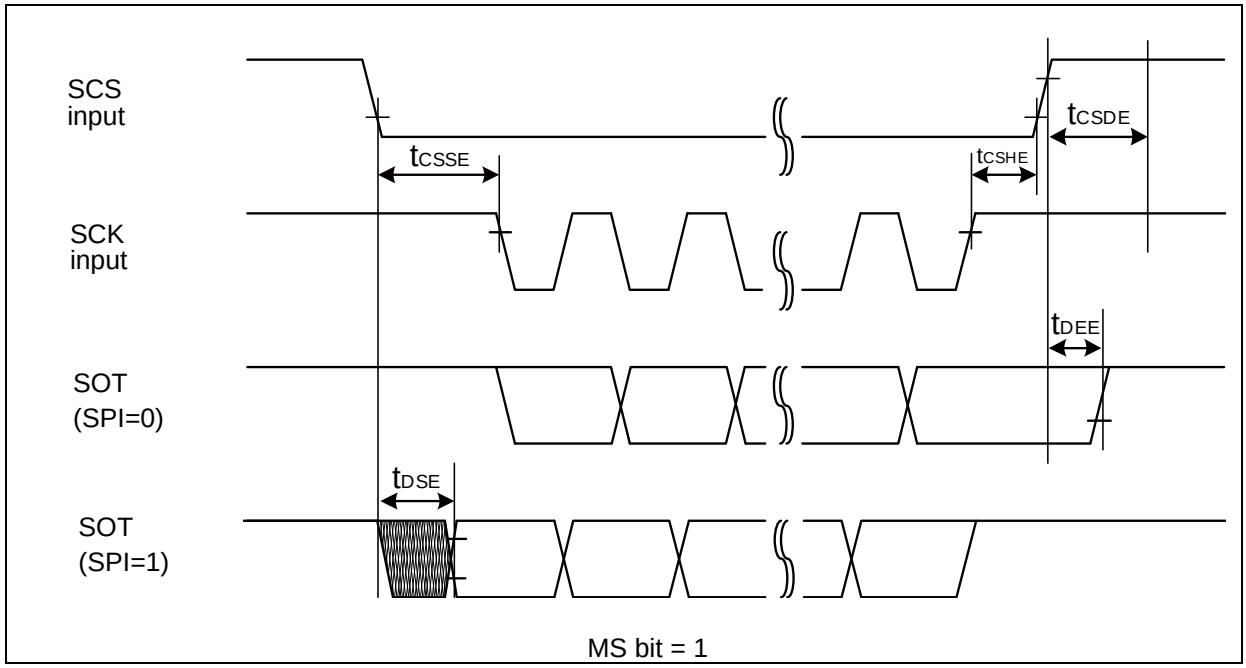
(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Baud rate	-	-	-	-	8	-	8	Mbps
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 30	+ 30	- 20	+ 20	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		50	-	30	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		0	-	0	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 30	-	$2t_{CYCP}$ - 30	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	50	-	30	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		10	-	10	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		20	-	20	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the same relocate port number; for example, the combination of SCKx_0 and SOTx_1 is not guaranteed.*
- *When the external load capacitance C_L = 30 pF.*


SCS
output
SCK
output
SOT
(SPI=0)
SOT
(SPI=1)
tCSSI
tCSHI
tCSDI
MS bit = 0


SCS
input
SCK
input
SOT
(SPI=0)
SOT
(SPI=1)
tCSSE
tCSHE
tCSDE
tDEE
tDSE
MS bit = 1

High-Speed Synchronous Serial (SPI = 1, SCINV = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Pin Name	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock operation	$4t_{CYCP}$	-	$4t_{CYCP}$	-	ns
SCK↓→SOT delay time	t_{SLOVI}	SCKx, SOTx		- 10	+ 10	- 10	+ 10	ns
SIN→SCK↑ setup time	t_{IVSHI}	SCKx, SINx		14 12.5*	-	12.5	-	ns
SCK↑→SIN hold time	t_{SHIXI}	SCKx, SINx		5	-	5	-	ns
SOT→SCK↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CYCP}$ - 10	-	$2t_{CYCP}$ - 10	-	ns
Serial clock L pulse width	t_{SLSH}	SCKx	External shift clock operation	$2t_{CYCP}$ - 5	-	$2t_{CYCP}$ - 5	-	ns
Serial clock H pulse width	t_{SHSL}	SCKx		t_{CYCP} + 10	-	t_{CYCP} + 10	-	ns
SCK↓→SOT delay time	t_{SLOVE}	SCKx, SOTx		-	15	-	15	ns
SIN→SCK↑ setup time	t_{IVSHE}	SCKx, SINx		5	-	5	-	ns
SCK↑→SIN hold time	t_{SHIXE}	SCKx, SINx		5	-	5	-	ns
SCK fall time	t_F	SCKx		-	5	-	5	ns
SCK rise time	t_R	SCKx		-	5	-	5	ns

Notes:

- *The above characteristics apply to CLK synchronous mode.*
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *These characteristics only guarantee the following pins:*

  No chip select: SIN4_0, SOT4_0, SCK4_0

  Chip select: SIN6_0, SOT6_0, SCK6_0, SCS60_0, SCS61_0, SCS62_0, SCS63_0
- *When the external load capacitance C_L = 30 pF. (for *, when C_L = 10 pF)*

12.7 Low-Voltage Detection Characteristics

12.7.1 Low-Voltage Detection Reset

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	-	2.46	2.55	2.64	V	When voltage drops
Released voltage	VDH	-	2.51	2.60	2.69	V	When voltage rises

12.7.2 Interrupt of Low-Voltage Detection

Parameter	Symbol	Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Detected voltage	VDL	SVHI = 00111	2.80	2.90	3.00	V	When voltage drops
Released voltage	VDH		2.90	3.00	3.11	V	When voltage rises
Detected voltage	VDL	SVHI = 00100	2.99	3.10	3.21	V	When voltage drops
Released voltage	VDH		3.09	3.20	3.31	V	When voltage rises
Detected voltage	VDL	SVHI = 01100	3.18	3.30	3.42	V	When voltage drops
Released voltage	VDH		3.28	3.40	3.52	V	When voltage rises
Detected voltage	VDL	SVHI = 01111	3.67	3.80	3.93	V	When voltage drops
Released voltage	VDH		3.76	3.90	4.04	V	When voltage rises
Detected voltage	VDL	SVHI = 01110	3.76	3.90	4.04	V	When voltage drops
Released voltage	VDH		3.86	4.00	4.14	V	When voltage rises
Detected voltage	VDL	SVHI = 01001	4.05	4.20	4.35	V	When voltage drops
Released voltage	VDH		4.15	4.30	4.45	V	When voltage rises
Detected voltage	VDL	SVHI = 01000	4.15	4.30	4.45	V	When voltage drops
Released voltage	VDH		4.25	4.40	4.55	V	When voltage rises
Detected voltage	VDL	SVHI = 11000	4.25	4.40	4.55	V	When voltage drops
Released voltage	VDH		4.34	4.50	4.66	V	When voltage rises
LVD stabilization wait time	t_{LVDW}	-	-	-	$6000 \times t_{CYCP}$*	µs	

*: t_{CYCP} indicates the APB2 bus clock cycle time.

12.10 Standby Recovery Time

12.10.1 Recovery Cause: Interrupt/WKUP

The time from the interrupt occurring to the time of program operation start is shown.

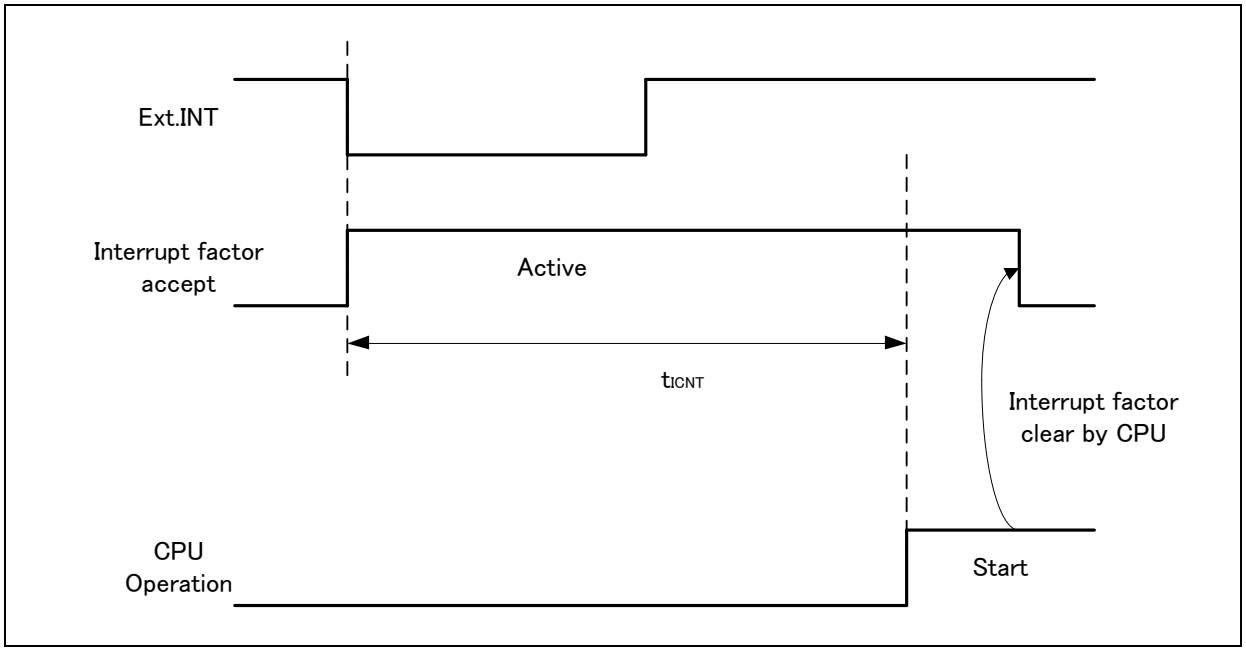
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{ICNT}	HCLK×1		µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		40	80	µs	
Low-speed CR Timer mode		450	900	µs	
Sub Timer mode		896	1136	µs	
RTC mode Stop mode (High-speed CR/Main/PLL Run mode return)		316	581	µs	
RTC mode Stop mode (Low-speed CR/sub Run mode return)		270	540	µs	
Deep Standby RTC mode with RAM retention		365	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		365	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in External Interrupt Recovery*)



*: External interrupt is set to detecting fall edge.

12.10.2 Recovery Cause: Reset

The time from reset release to the program operation start is shown.

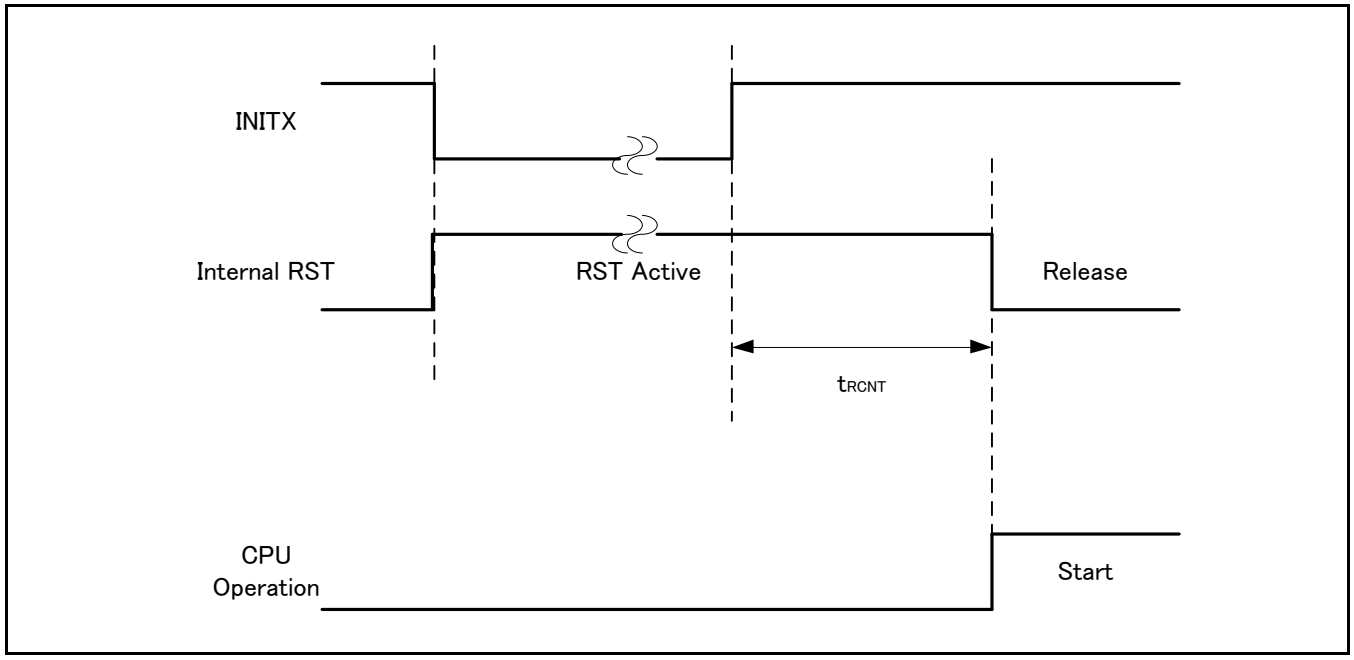
Recovery Count Time

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

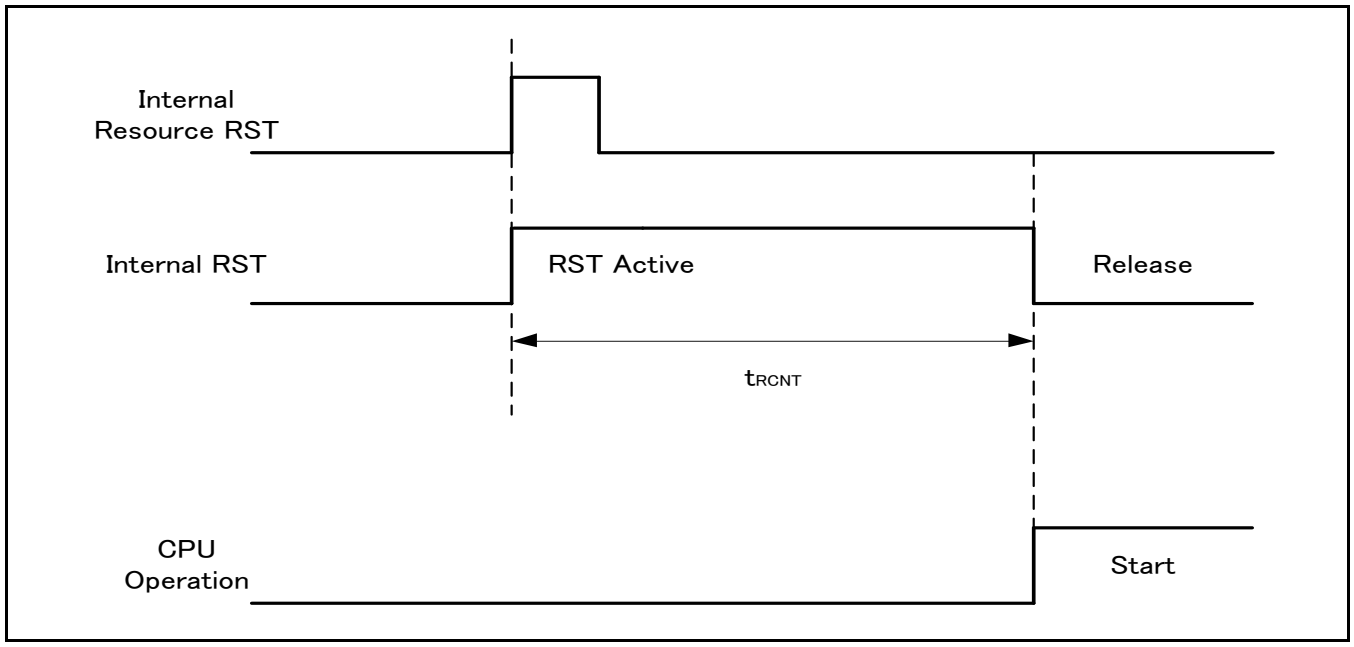
Parameter	Symbol	Value		Unit	Remarks
		Typ	Max*		
Sleep mode	t_{RCNT}	155	266	µs	
High-speed CR Timer mode Main Timer mode PLL Timer mode		155	266	µs	
Low-speed CR Timer mode		315	567	µs	
Sub Timer mode		315	567	µs	
RTC mode Stop mode		315	567	µs	
Deep Standby RTC mode with RAM retention		336	667	µs	without RAM retention
Deep Standby Stop mode with RAM retention		336	667	µs	with RAM retention

*: The maximum value depends on the built-in CR accuracy.

Example of Standby Recovery Operation (when in INITX Recovery)



Example of Standby Recovery Operation (when in Internal Resource Reset Recovery*)



*: Depending on the low-power consumption mode, the reset issue from the internal resource is not included in the recovery cause.

Notes:

- *The return factor is different in each low power consumption mode.*
  See Chapter 6: Low Power Consumption mode and Operations of Standby modes in "FM4 Family Peripheral Manual Main Part (002-04856).
- *The recovery process is unique for each operating mode. See Chapter 6: Low Power Consumption mode in FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the power-on reset/low-voltage detection reset, they are not included in the return factor. See 12.4.8 Power-On Reset Timing.*
- *In recovering from reset, CPU changes to High-speed Run mode. In the case of using the main clock and PLL clock, they need further main clock oscillation stabilization wait time and oscillation stabilization wait time of Main PLL clock.*
- *Internal resource reset indicates Watchdog reset and CSV reset.*