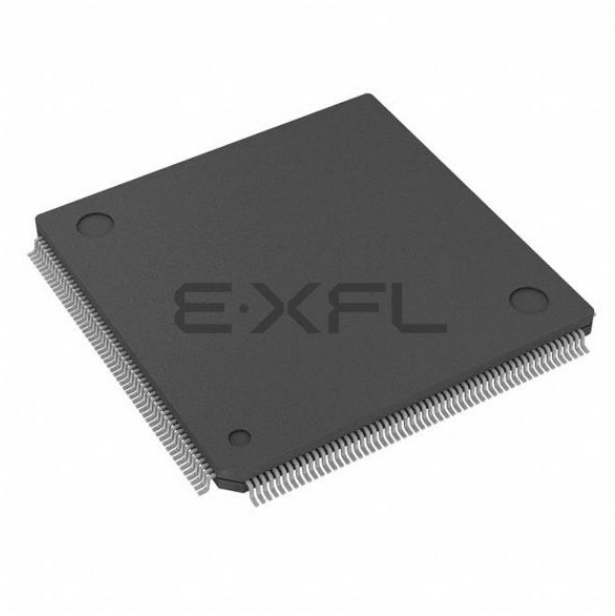

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	200MHz
Connectivity	CSIO, EBI/EMI, I²C, LINbus, SD, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	190
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	216-LQFP
Supplier Device Package	216-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/s6e2c1al0agl2000a

Table of Contents

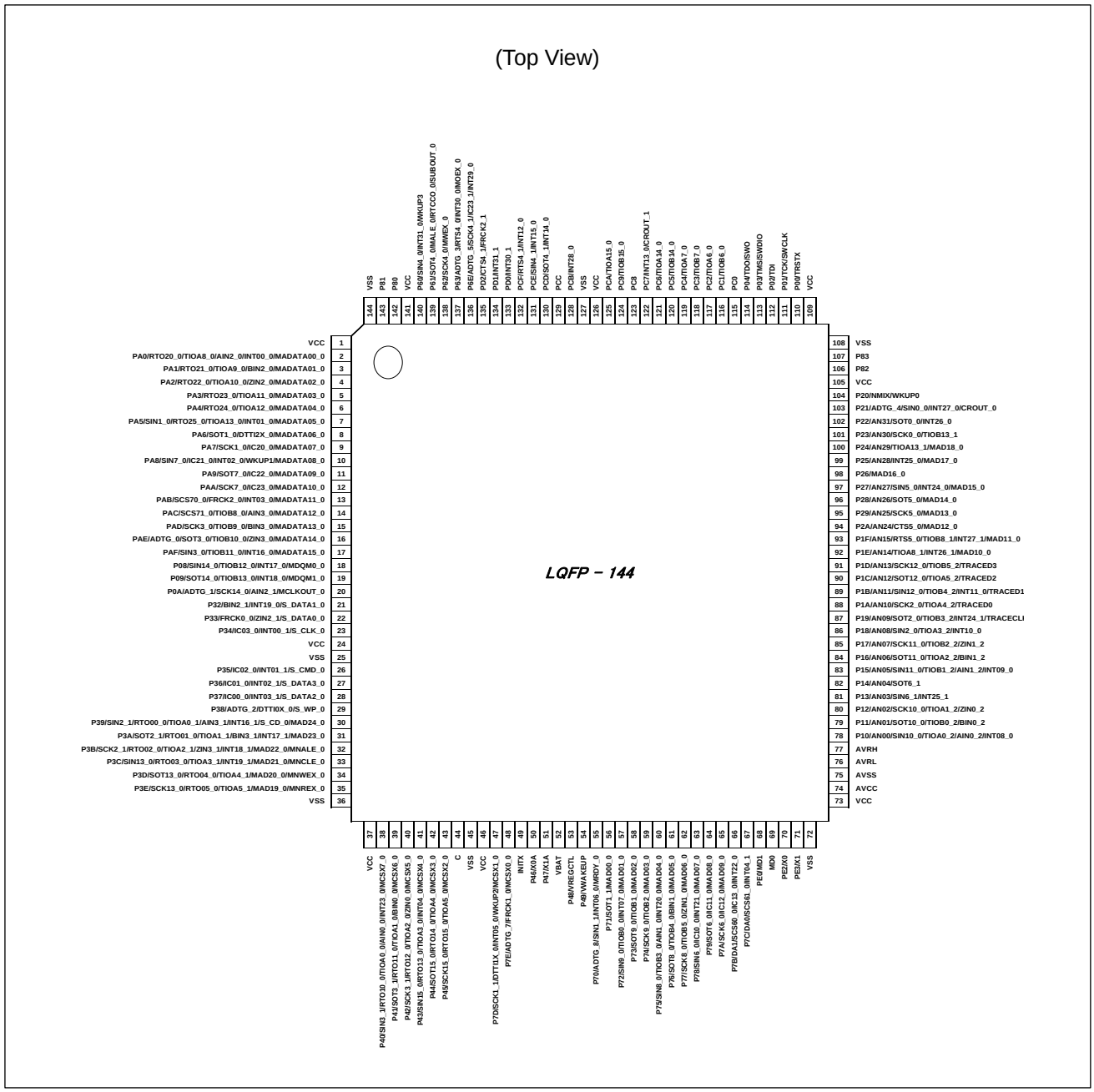
Product Name	S6E2C18H0A S6E2C19H0A S6E2C1AH0A	S6E2C18J0A S6E2C19J0A S6E2C1AJ0A	S6E2C18L0A S6E2C19L0A S6E2C1AL0A
Debug function	SWJ-DP/ETM/HTM		
Unique ID	Yes		

Notes:

- *All signals of the peripheral function in each product cannot be allocated by limiting the pins of package. It is necessary to use the port relocate function of the I/O port according to your function use.*
- *See 12.4.3 Built-In CR Oscillation Characteristics for the accuracy of the built-in CR.*

3. Pin Assignments

LQS144



Note:

- *The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.*

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
8	8	8	D3	PA6 SOT1_0 (SDA1_0)) DTTI2X_0 MADATA06_0	E	I
9	9	9	D4	PA7 SCK1_0 (SCL1_0) IC20_0 MADATA07_0	E	I
10	10	-	E2	P50 SCS72_0 RTO00_1 (PPG00_1) TIOA8_2 MADATA16_0	E	I
11	11	-	E3	P51 SCS73_0 RTO01_1 (PPG00_1) TIOB8_2 MADATA17_0	E	I
12	12	-	E4	P52 RTO02_1 (PPG02_1) TIOA9_2 MADATA18_0	E	I
13	-	-	-	P53 RTO03_1 (PPG02_1) TIOB9_2 MADATA19_0	E	I
14	13	10	E5	PA8 SIN7_0 IC21_0 INT02_0 WKUP1 MADATA08_0	I	Q
15	14	11	F1	PA9 SOT7_0 (SDA7_0) IC22_0 MADATA09_0	N	I
16	15	12	F2	PAA SCK7_0 (SCL7_0) IC23_0 MADATA10_0	N	I
17	16	13	F3	PAB SCS70_0 FRCK2_0 INT03_0 MADATA11_0	E	K

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQQ216	LQP176	LQS144	LBE192			
93	78	62	N10	P77 SCK8_0 (SCL8_0) TIOB5_0 ZIN1_0 MAD06_0	E	I
94	-	-	-	PF8 SCS70_1 DTTI1X_1 AIN1_1	E	I
95	-	-	-	PF9 SCS71_1 IC10_1 BIN1_1	E	I
96	79	63	L10	P78 SIN6_0 IC10_0 INT21_0 MAD07_0	E	K
97	80	64	K10	P79 SOT6_0 (SDA6_0) IC11_0 MAD08_0	L	I
98	81	65	M10	P7A SCK6_0 (SCL6_0) IC12_0 MAD09_0	L	I
99	82	66	N11	P7B DA1 SCS60_0 IC13_0 INT22_0	R	J
100	83	67	M11	P7C DA0 SCS61_0 INT04_1	R	J
101	-	-	-	PFA SCK7_1 (SCL7_1) IC11_1 ZIN1_1	E	I
102	-	-	-	PFB SOT7_1 (SDA7_1) IC12_1 INT07_2	E	K
103	-	-	-	PFC SIN7_1 IC13_1 INT06_2	E	K
104	84	68	N13	PE0 MD1	C	E
105	85	69	N12	MD0	J	D

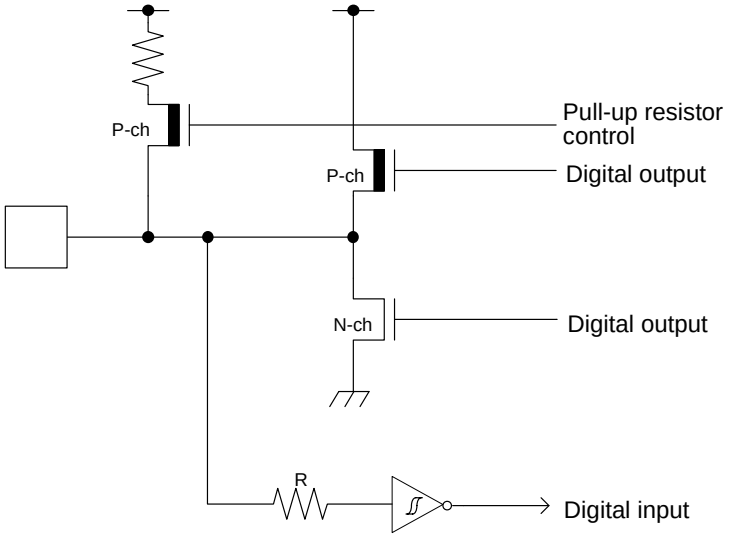
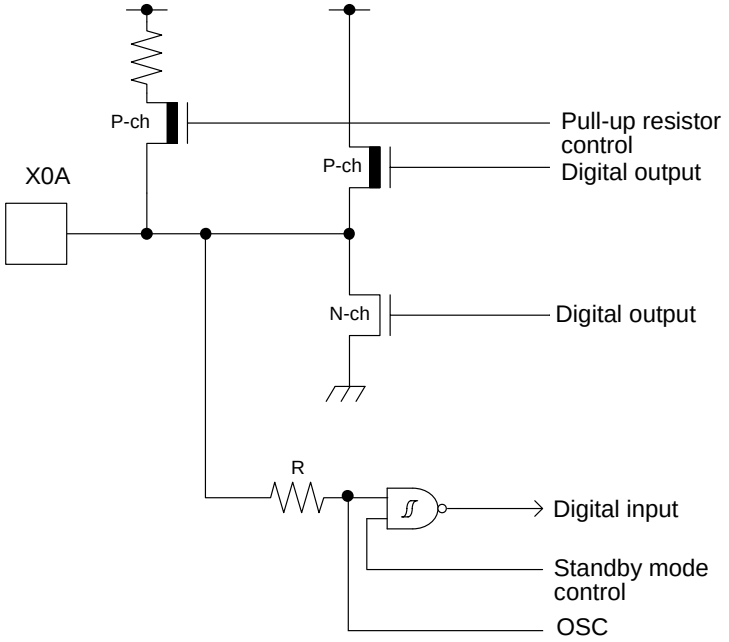
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Base Timer 7	TIOA7_0	Base Timer ch 7 TIOA pin	181	149	119	F9
	TIOA7_1		87	72	-	N9
	TIOA7_2		202	-	-	-
	TIOB7_0	Base Timer ch 7 TIOB pin	180	148	118	E9
	TIOB7_1		88	73	-	P9
	TIOB7_2		201	-	-	-
Base Timer 8	TIOA8_0	Base Timer ch 8 TIOA pin	2	2	2	B2
	TIOA8_1		142	116	92	G10
	TIOA8_2		10	10	-	E2
	TIOB8_0	Base Timer ch 8 TIOB pin	18	17	14	F4
	TIOB8_1		143	117	93	G9
	TIOB8_2		11	11	-	E3
Base Timer 9	TIOA9_0	Base Timer ch 9 TIOA pin	3	3	3	C2
	TIOA9_1		126	102	-	J10
	TIOA9_2		12	12	-	E4
	TIOB9_0	Base Timer ch 9 TIOB pin	23	18	15	F5
	TIOB9_1		127	103	-	J9
	TIOB9_2		13	-	-	-
Base Timer 10	TIOA10_0	Base Timer ch 10 TIOA pin	4	4	4	C3
	TIOA10_1		128	104	-	H10
	TIOA10_2		19	-	-	-
	TIOB10_0	Base Timer ch 10 TIOB pin	24	19	16	F6
	TIOB10_1		129	105	-	J14
	TIOB10_2		20	-	-	-
Base Timer 11	TIOA11_0	Base Timer ch 11 TIOA pin	5	5	5	D5
	TIOA11_1		138	112	-	G13
	TIOA11_2		33	-	-	-
	TIOB11_0	Base Timer ch 11 TIOB pin	25	20	17	G2
	TIOB11_1		139	113	-	F14
	TIOB11_2		51	41	-	L2
Base Timer 12	TIOA12_0	Base Timer ch 12 TIOA pin	6	6	6	D2
	TIOA12_1		140	114	-	G12
	TIOA12_2		52	42	-	L3
	TIOB12_0	Base Timer ch 12 TIOB pin	30	21	18	G3
	TIOB12_1		141	115	-	G11
	TIOB12_2		53	43	-	M2

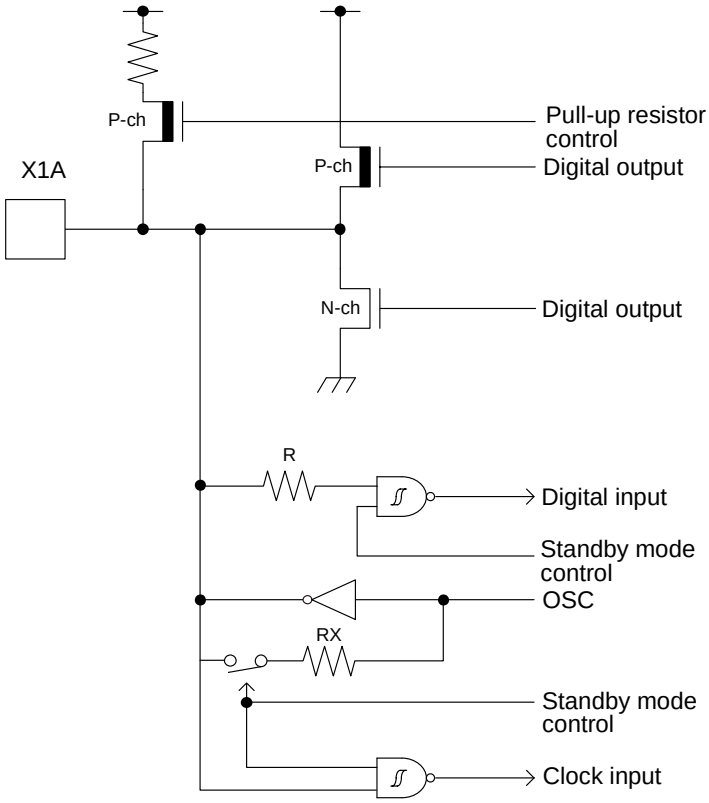
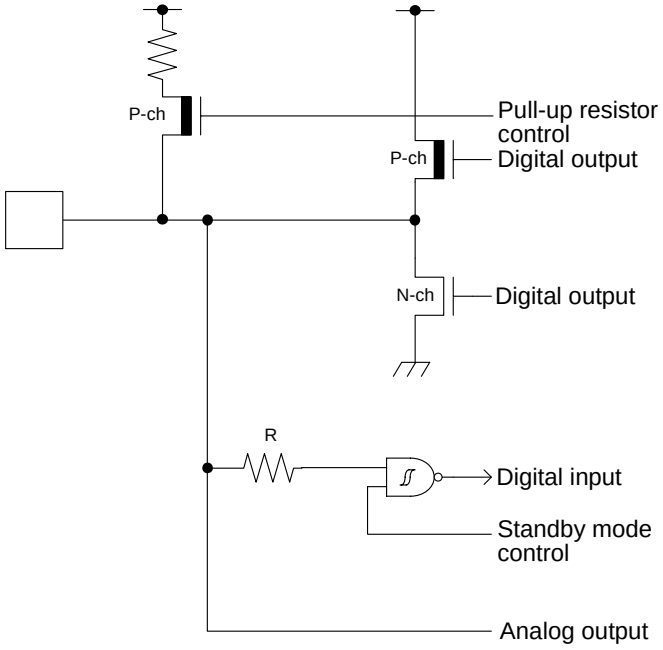
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Debugger	SWCLK	Serial wire debug interface clock input pin	165	135	111	A12
	SWDIO	Serial wire debug interface data input/output pin	167	137	113	B12
	SWO	Serial wire viewer output pin	168	138	114	B11
	TCK	JTAG test clock input pin	165	135	111	A12
	TDI	JTAG test data input pin	166	136	112	C12
	TDO	JTAG debug data output pin	168	138	114	B11
	TMS	JTAG test mode state input/output pin	167	137	113	B12
	TRACECLK	Trace CLK output pin of ETM/HTM	131	107	87	H12
	TRACED0	Trace data output pin of ETM/ Trace data output pin of HTM	132	108	88	H14
	TRACED1		133	109	89	G14
	TRACED2		134	110	90	H13
	TRACED3		135	111	91	H11
	TRACED4	Trace data output pin of HTM	138	112	-	G13
	TRACED5		139	113	-	F14
	TRACED6		140	114	-	G12
	TRACED7		141	115	-	G11
	TRACED8		119	-	-	-
	TRACED9		120	-	-	-
	TRACED10		121	-	-	-
	TRACED11		122	-	-	-
	TRACED12		148	-	-	-
	TRACED13		149	-	-	-
	TRACED14		150	-	-	-
	TRACED15		151	-	-	-
	TRSTX	JTAG test reset Input pin	164	134	110	B13

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
External bus	MNALE_0	External bus interface ALE signal to control NAND flash output pin	47	37	32	K2
	MNCLE_0	External bus interface CLE signal to control NAND flash output pin	48	38	33	K3
	MNREX_0	External bus interface read enable signal to control NAND flash	50	40	35	L1
	MNWEX_0	External bus interface write enable signal to control NAND flash	49	39	34	K4
	MOEX_0	External bus interface read enable signal for SRAM	209	169	137	C5
	MWEX_0	External bus interface write enable signal for SRAM	210	170	138	B4
	MSDCLK_0	SDRAM interface SDRAM clock output pin	90	75	-	L9
	MSDCKE_0	SDRAM interface SDRAM clock enable pin	89	74	-	M9
	MRASX_0	SDRAM interface SDRAM column active strobe pin	85	70	-	N8
	MCASX_0	SDRAM interface SDRAM row active strobe pin	86	71	-	M8
	MSDWEX_0	SDRAM interface SDRAM write enable pin	87	72	-	N9
External interrupt	INT00_0	External interrupt request 00 input pin	2	2	2	B2
	INT00_1		38	28	23	H3
	INT00_2		19	-	-	-
	INT01_0	External interrupt request 01 input pin	7	7	7	D1
	INT01_1		41	31	26	H6
	INT01_2		51	41	-	L2
	INT02_0	External interrupt request 02 input pin	14	13	10	E5
	INT02_1		42	32	27	J5
	INT02_2		26	-	-	-
	INT03_0	External interrupt request 03 input pin	17	16	13	F3
	INT03_1		43	33	28	J4
	INT03_2		34	24	-	G6
	INT04_0	External interrupt request 04 input pin	59	49	41	L4
	INT04_1		100	83	67	M11
	INT04_2		65	-	-	-
	INT05_0	External interrupt request 05 input pin	70	55	47	L5
	INT05_1		86	71	-	M8
	INT05_2		68	-	-	-

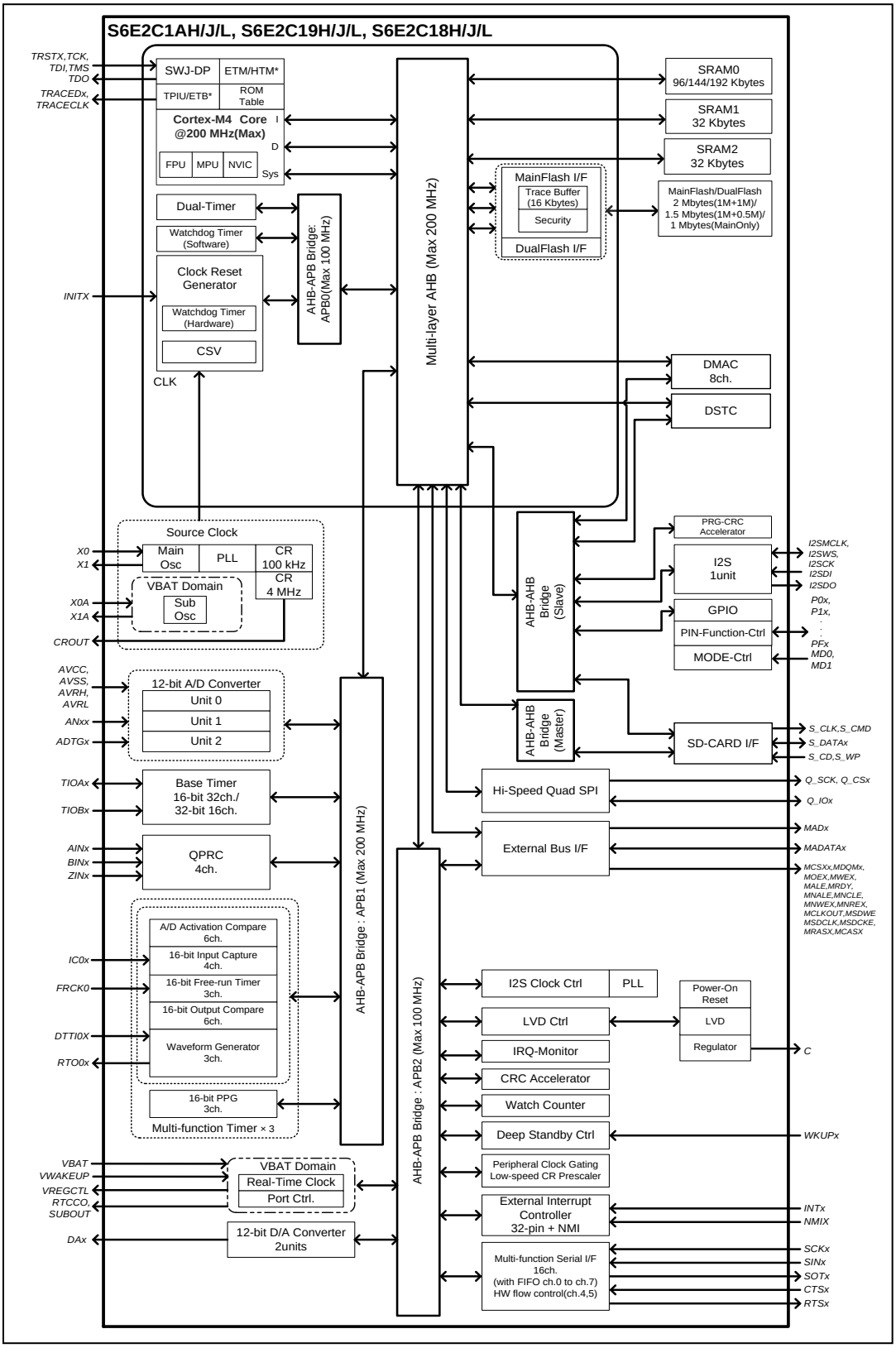
Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 5	SIN5_0	Multi-function serial interface ch 5 input pin	147	121	97	F13
	SIN5_1		170	140	-	D11
	SOT5_0 (SDA5_0)	Multi-function serial interface ch 5 output pin. This pin operates as SOT5 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA5 when it is used in an I²C (operation mode 4).	146	120	96	F12
	SOT5_1 (SDA5_1)		171	141	-	B10
	SCK5_0 (SCL5_0)	Multi-function serial interface ch 5 clock I/O pin. This pin operates as SCK5 when it is used in a CSIO (operation mode 2) and as SCL5 when it is used in an I²C (operation mode 4).	145	119	95	F11
	SCK5_1 (SCL5_1)		172	142	-	C10
	CTS5_0	Multi-function serial interface ch 5 CTS input pin	144	118	94	F10
	CTS5_1		173	143	-	D10
	RTS5_0	Multi-function serial interface ch 5 RTS output pin	143	117	93	G9
	RTS5_1		174	144	-	B9
Multi-Function Serial 6	SIN6_0	Multi-function serial interface ch 6 input pin	96	79	63	L10
	SIN6_1		117	97	81	K14
	SOT6_0 (SDA6_0)	Multi-function serial interface ch 6 output pin. This pin operates as SOT6 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA6 when it is used in an I²C (operation mode 4).	97	80	64	K10
	SOT6_1 (SDA6_1)		118	98	82	K11
	SCK6_0 (SCL6_0)	Multi-function serial interface ch 6 clock I/O pin. This pin operates as SCK6 when it is used in a CSIO (operation mode 2) and as SCL6 when it is used in an I²C (operation mode 4).	98	81	65	M10
	SCK6_1 (SCL6_1)		126	102	-	J10
	SCS60_0	Multi-function serial interface ch 6 chip select 0 input/output pin	99	82	66	N11
	SCS60_1		127	103	-	J9
	SCS61_0	Multi-function serial interface ch 6 chip select1 input/output pin	100	83	67	M11
	SCS61_1		128	104	-	H10
	SCS62_0	Multi-function serial interface ch 6 chip select2 input/output pin	79	64	-	K6
	SCS62_1		129	105	-	J14
	SCS63_0	Multi-function serial interface ch 6 chip select3 input/output pin	78	63	-	K5
	SCS63_1		119	-	-	-

Module	Pin Name	Function	Pin Number			
			LQQ 216	LQP 176	LQS 144	LBE 192
Multi-Function Serial 13	SIN13_0	Multi-function serial interface ch 13 input pin	48	38	33	K3
	SIN13_1		206	-	-	-
	SOT13_0 (SDA13_0)	Multi-function serial interface ch 13 output pin. This pin operates as SOT13 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA13 when it is used in an I²C (operation mode 4).	49	39	34	K4
	SOT13_1 (SDA13_1)		205	-	-	-
	SCK13_0 (SCL13_0)	Multi-function serial interface ch 13 clock I/O pin. This pin operates as SCK13 when it is used in a CSIO (operation mode 2) and as SCL13 when it is used in an I²C (operation mode 4).	50	40	35	L1
	SCK13_1 (SCL13_1)		204	-	-	-
Multi-Function Serial 14	SIN14_0	Multi-function serial interface ch 14 input pin	30	21	18	G3
	SIN14_1		201	-	-	-
	SOT14_0 (SDA14_0)	Multi-function serial interface ch 14 output pin. This pin operates as SOT14 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA14 when it is used in an I²C (operation mode 4).	31	22	19	G4
	SOT14_1 (SDA14_1)		200	-	-	-
	SCK14_0 (SCL14_0)	Multi-function serial interface ch 14 clock I/O pin. This pin operates as SCK14 when it is used in a CSIO (operation mode 2) and as SCL14 when it is used in an I²C (operation mode 4).	32	23	20	G5
	SCK14_1 (SCL14_1)		199	-	-	-
Multi-Function Serial 15	SIN15_0	Multi-function serial interface ch 15 input pin	59	49	41	L4
	SIN15_1		19	-	-	-
	SOT15_0 (SDA15_0)	Multi-function serial interface ch 15 output pin. This pin operates as SOT15 when it is used in a UART/CSIO/LIN (operation modes 0 to 3) and as SDA15 when it is used in an I²C (operation mode 4).	60	50	42	M4
	SOT15_1 (SDA15_1)		20	-	-	-
	SCK15_0 (SCL15_0)	Multi-function serial interface ch 15 clock I/O pin. This pin operates as SCK15 when it is used in a CSIO (operation mode 2) and as SCL15 when it is used in an I²C (operation mode 4).	61	51	43	N4
	SCK15_1 (SCL15_1)		21	-	-	-

Type	Circuit	Remarks
O		・CMOS level output ・CMOS level hysteresis input ・5 V tolerant ・Pull-up resistor control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・Available to control of PZR register (pseudo-open drain control) ・For PZR registers, refer to GPIO in the “FM4 Family Peripheral Manual Main Part (002-04856)”. ・For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856). ・
P		・CMOS level output ・CMOS level hysteresis input ・Pull-up resistor control ・Pull-up resistor: approximately 50 kΩ ・I_{OH} = -4 mA, I_{OL} = 4 mA ・For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).

Type	Circuit	Remarks
Q		It is possible to select the sub oscillation/GPIO function. When the sub oscillation is selected: ・ Oscillation feedback resistor: approximately 10 MΩ When the GPIO is selected: ・ CMOS level output. ・ CMOS level hysteresis input ・ Pull-up resistor control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA ・ For I/O setting, refer to VBAT Domain in the FM4 Family Peripheral Manual Main Part (002-04856).
R		・ CMOS level output ・ CMOS level hysteresis input ・ Analog output ・ Pull-up resistor control ・ Standby mode control ・ Pull-up resistor: approximately 50 kΩ ・ I_{OH} = -4 mA, I_{OL} = 4 mA (4.5V to 5.5V) ・ I_{OH} = -2 mA, I_{OL} = 2 mA (2.7V to 4.5V)

8. Block Diagram



12. Electrical Characteristics

12.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1,*2	V_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Power supply voltage (VBAT) *1 ,*3	V_{BAT}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog power supply voltage *1 ,*4	AV_{CC}	V_{SS} - 0.5	V_{SS} + 6.5	V	
Analog reference voltage *1 ,*4	AVRH	V_{SS} - 0.5	V_{SS} + 6.5	V	
Input voltage *1	V_I	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
		V_{SS} - 0.5	V_{SS} + 6.5	V	5V tolerant
Analog pin input voltage *1	V_{IA}	V_{SS} - 0.5	AV_{CC} + 0.5 (≤ 6.5 V)	V	
Output voltage *1	V_O	V_{SS} - 0.5	V_{CC} + 0.5 (≤ 6.5 V)	V	
L level maximum output current *5	I_{OL}	-	10	mA	4 mA type
			20	mA	8 mA type
			20	mA	10 mA type
			20	mA	12 mA type
			22.4	mA	I^2C Fm+
L level average output current *6	I_{OLAV}	-	4	mA	4 mA type
			8	mA	8 mA type
			10	mA	10 mA type
			12	mA	12 mA type
			20	mA	I^2C Fm+
L level total maximum output current	$\sum I_{OL}$	-	100	mA	
L level total maximum output current *7	$\sum I_{OLAV}$	-	50	mA	
H level maximum output current *5	I_{OH}	-	- 10	mA	4 mA type
			-20	mA	8 mA type
			- 20	mA	10 mA type
			- 20	mA	12 mA type
H level average output current *6	I_{OHAV}	-	- 4	mA	4 mA type
			-8	mA	8 mA type
			- 10	mA	10 mA type
			- 12	mA	12 mA type
H level total maximum output current	$\sum I_{OH}$	-	- 100	mA	
H level total average output current *7	$\sum I_{OHAV}$	-	- 50	mA	
Power consumption	P_D	-	200	mW	
Storage temperature	T_{STG}	- 55	+ 150	°C	

1: These parameters are based on the condition that $V_{SS} = AV_{SS} = 0.0$ V.

2: V_{CC} must not drop below V_{SS} - 0.5 V.

3: V_{BAT} must not drop below V_{SS} - 0.5 V.

4: Ensure that the voltage does not exceed V_{CC} + 0.5V, for example, when the power is turned on.

5: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

6: The average output current is defined as the average current value flowing through any one of the corresponding pins for a 100-ms period.

7: The total average output current is defined as the average current value flowing through all of corresponding pins for a 100-ms period.

WARNING:

- *Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.*

12.3 DC Characteristics

12.3.1 Current Rating

Table 12-1 Typical and Maximum Current Consumption in Normal Operation (PLL), Code Running from Flash Memory (Flash Accelerator Mode and Trace Buffer Function Enabled)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *7,*8 (PLL)	*5	200 MHz	117	224	mA	*3 When all peripheral clocks are on
					192 MHz	113	219	mA	
					180 MHz	106	211	mA	
				*6	160 MHz	95	197	mA	
					144 MHz	86	186	mA	
					120 MHz	73	169	mA	
					100 MHz	61	155	mA	
					80 MHz	50	140	mA	
					60 MHz	39	126	mA	
					40 MHz	27	112	mA	
					20 MHz	16	97	mA	
					8 MHz	8.7	88.9	mA	
					4 MHz	6.4	86.1	mA	
				*5	200 MHz	71	168	mA	*3 When all peripheral clocks are off
					192 MHz	68	165	mA	
					180 MHz	64	159	mA	
				*6	160 MHz	58	151	mA	
					144 MHz	52	144	mA	
					120 MHz	44	134	mA	
					100 MHz	38	126	mA	
					80 MHz	31	117	mA	
					60 MHz	24	109	mA	
					40 MHz	17	100	mA	
					20 MHz	10	91	mA	
					8 MHz	6.3	86.1	mA	
					4 MHz	5.0	84.5	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 11, FBFCR.BE = 1)

6: When stopping flash accelerator mode and trace buffer function (FRWTR.RWT = 10, FBFCR.BE = 1)

7: Firmware being executed during data collection for this table is not being accessed from the MainFlash memory."

8: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-3 Typical and Maximum Current Consumption in Normal Operation (PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6,*7 (PLL)	*5	72 MHz	71	161	mA	*3 When all peripheral clocks are on
					60 MHz	62	150	mA	
					48 MHz	51	138	mA	
					36 MHz	40	125	mA	
					24 MHz	29	112	mA	
					12 MHz	17	98	mA	
					8 MHz	13	93	mA	
					4 MHz	8.4	88.5	mA	
				*5	72 MHz	46	132	mA	*3 When all peripheral clocks are off
					60 MHz	41	125	mA	
					48 MHz	34	118	mA	
					36 MHz	27	110	mA	
					24 MHz	20	102	mA	
					12 MHz	12	93	mA	
					8 MHz	9.4	89.7	mA	
					4 MHz	6.5	86.4	mA	

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

Table 12-4 Typical and Maximum Current Consumption in Normal Operation (Other than PLL), Code with Data Accessing Running from Flash Memory (Flash 0 Wait-Cycle Mode and Read Access 0 Wait)

Parameter	Symbol	Pin Name	Conditions		Frequency*4	Value		Unit	Remarks
						Typ*1	Max*2		
Power supply current	I_{CC}	VCC	Normal operation *6, *7 (main oscillation)	*5	4 MHz	4.7	84.9	mA	*3 When all peripheral clocks are on
						3.9	83.8	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in High-speed CR)	*5	4 MHz	3.0	83.2	mA	*3 When all peripheral clocks are on
						2.1	82.0	mA	*3 When all peripheral clocks are off
			Normal operation *6, *8 (sub oscillation)	*5	32 kHz	0.78	80.37	mA	*3 When all peripheral clocks are on
						0.77	80.36	mA	*3 When all peripheral clocks are off
			Normal operation *6 (built-in low-speed CR)	*5	100 kHz	0.81	80.39	mA	*3 When all peripheral clocks are on
						0.78	80.38	mA	*3 When all peripheral clocks are off

1: T_A = +25 °C, V_{CC} = 3.3 V

2: T_J = +125 °C, V_{CC} = 5.5 V

3: When all ports are fixed

4: Frequency is a value of HCLK when PCLK0 = PCLK1 = PCLK2 = HCLK/2

5: When operating flash 0 wait-cycle mode and read access 0 wait (FRWTR.RWT = 00, FBFCR.SD = 000)

6: With data access to a MainFlash memory.

7: When using the crystal oscillator of 4 MHz (including the current consumption of the oscillation circuit)

8: When using the crystal oscillator of 32 kHz (including the current consumption of the oscillation circuit)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
L level output voltage	V_{OL}	4 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 2 mA					
		8 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 8 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 4 mA					
		10 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 10 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		12 mA type	$V_{CC} \geq 4.5$ V, I_{OL} = 12 mA	V_{SS}	-	0.4	V	
			$V_{CC} < 4.5$ V, I_{OL} = 8 mA					
		The pin doubled as I^2C Fm+	$V_{CC} \geq 4.5$ V, I_{OL} = 4 mA	V_{SS}	-	0.4	V	At GPIO
			$V_{CC} < 4.5$ V, I_{OL} = 3 mA					
			$V_{CC} \leq 4.5$ V, I_{OL} = 20 mA					At I2C Fm+
Input leak current	I_{IL}	-	-	- 5	-	+ 5	µA	
Pull-up resistor value	R_{PU}	Pull-up pin	$V_{CC} \geq 4.5$ V	25	50	100	kΩ	
			$V_{CC} < 4.5$ V	30	80	200		
Input capacitance	C_{IN}	Other than VCC, VBAT, VSS, AVCC, AVSS, AVRH	-	-	5	15	pF	

When Using High-Speed Synchronous Serial Chip Select (SCINV = 0, CSLVL = 1)

(V_{CC} = 2.7V to 5.5V, V_{SS} = 0V)

Parameter	Symbol	Conditions	V_{CC} < 4.5 V		V_{CC} ≥ 4.5 V		Unit
			Min	Max	Min	Max	
SCS↓→SCK↓ setup time	t_{CSSI}	Internal shift clock operation	(*1)-20	(*1)+0	(*1)-20	(*1)+0	ns
SCK↑→SCS↑ hold time	t_{CSHI}		(*2)+0	(*2)+20	(*2)+0	(*2)+20	ns
SCS deselect time	t_{CSDI}		(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	(*3)-20 +5t_{CYCP}	(*3)+20 +5t_{CYCP}	ns
SCS↓→SCK↓ setup time	t_{CSSE}	External shift clock operation	3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCK↑→SCS↑ hold time	t_{CSHE}		0	-	0	-	ns
SCS deselect time	t_{CSDE}		3t_{CYCP}+15	-	3t_{CYCP}+15	-	ns
SCS↓→SOT delay time	t_{DSE}		-	25	-	25	ns
SCS↑→SOT delay time	t_{DEE}		0	-	0	-	ns

(*1): CSSU bit value×serial chip select timing operating clock cycle [ns]

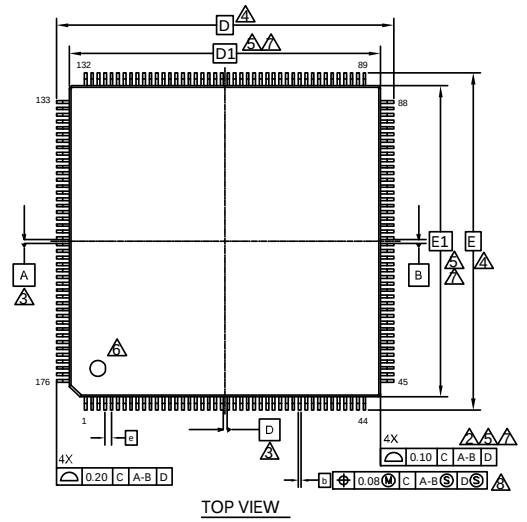
(*2): CSHD bit value×serial chip select timing operating clock cycle [ns]

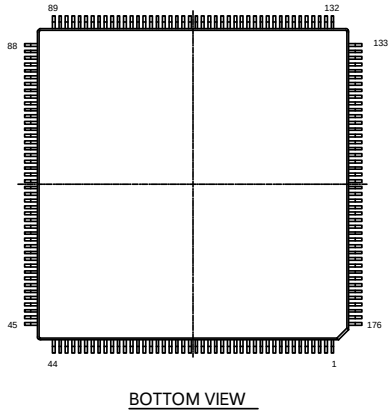
(*3): CSDS bit value×serial chip select timing operating clock cycle [ns]

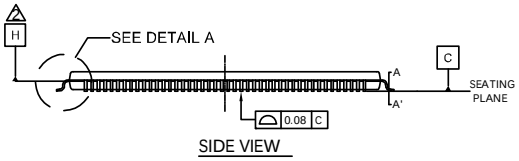
Notes:

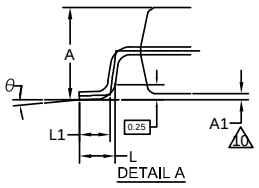
- *t_{CYCP} indicates the APB bus clock cycle time. For more information about the APB bus number to which the multi-function serial is connected, see 8. Block Diagram in this data sheet.*
- *For more information about CSSU, CSHD, CSDS, and the serial chip select timing operating clock, see FM4 Family Peripheral Manual Main Part (002-04856).*
- *When the external load capacitance C_L = 30 pF.*

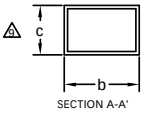
Package Type	Package Code
LQFP 176	LQP 176











SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	26.00 BSC		
D1	24.00 BSC		
e	0.50 BSC		
E	26.00 BSC		
E1	24.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15150 **

PACKAGE OUTLINE, 176 LEAD LQFP
24.0X24.0X1.7 MM LQP176 REV**