Infineon Technologies - XC2263N40F66LAAFXUMA1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	66MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	42K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2263n40f66laafxuma1

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1.3 Definition of Feature Variants

The XC226xN types are offered with several Flash memory sizes. **Table 3** and **Table 4** describe the location of the available Flash memory.

Table 3 Continuous Flash Memory Ranges

Total Flash Size	1st Range[1)]	2nd Range	3rd Range
320 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C4'FFFF_H$	n.a.
192 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C1'0000_H$ … $C1'FFFF_H$	$C4'0000_H$ … $C4'FFFF_H$
128 Kbytes	$C0'0000_H$ … $C0'EFFF_H$	$C4'0000_H$ … $C4'FFFF_H$	n.a.

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

Table 4 Flash Memory Module Allocation (in Kbytes)

Total Flash Size	Flash 0[1)]	Flash 1
320	256	64
192	128	64
128	64	64

1) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

The XC226xN types are offered with different interface options. **Table 5** lists the available channels for each option.

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
11 ADC0 channels	CH0, CH2 … CH5, CH8 … CH11, CH13, CH15
8 ADC0 channels	CH0, CH2 … CH4, CH8, CH10, CH13, CH15
5 ADC1 channels	CH0, CH2, CH4 … CH6
1 CAN node	CAN0 64 message objects
2 CAN nodes	CAN0, CAN1 64 message objects
3 CAN nodes	CAN0, CAN1, CAN2 64 message objects

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
6 CAN nodes	CAN0, CAN1, CAN2,CAN3, CAN4, CAN5 256 message objects
2 serial channels	U0C0, U0C1
4 serial channels	U0C0, U0C1, U1C0, U1C1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

The XC226xN types are offered with several SRAM memory sizes. **Figure 1** shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0’0000h-E0’1FFFh and 8 Kbytes of DSRAM will be at 00’C000h-00’DFFFh.

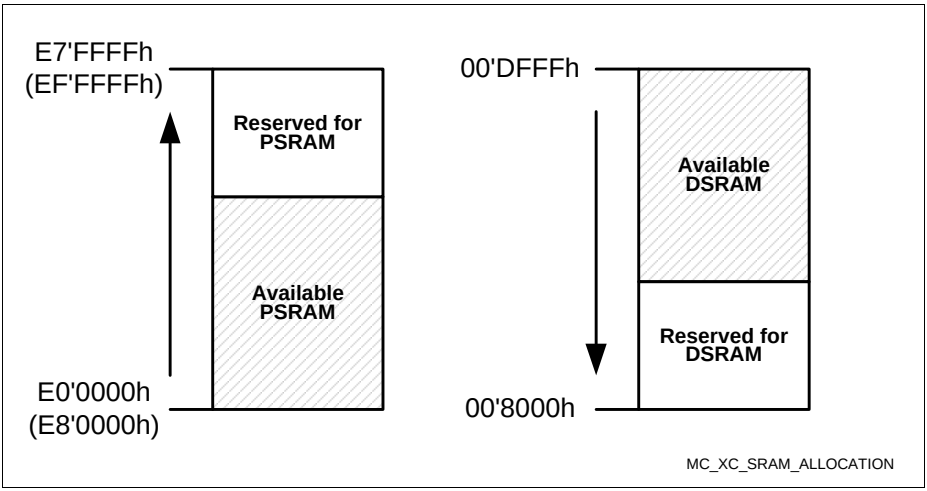

Figure 1 SRAM Allocation

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
6	P7.0	O0 / I	St/B	**Bit 0 of Port 7, General Purpose Input/Output**
	T3OUT	O1	St/B	**GPT12E Timer T3 Toggle Latch Output**
	T6OUT	O2	St/B	**GPT12E Timer T6 Toggle Latch Output**
	TDO_A	OH / IH	St/B	**JTAG Test Data Output / DAP1 Input/Output** If DAP pos. 0 or 2 is selected during start-up, an internal pull-down device will hold this pin low when nothing is driving it.
	ESR2_1	I	St/B	**ESR2 Trigger Input 1**
	RxDC4B	I	St/B	**CAN Node 4 Receive Data Input**
7	P7.3	O0 / I	St/B	**Bit 3 of Port 7, General Purpose Input/Output**
	EMUX1	O1	St/B	**External Analog MUX Control Output 1 (ADC1)**
	U0C1_DOUT	O2	St/B	**USIC0 Channel 1 Shift Data Output**
	U0C0_DOUT	O3	St/B	**USIC0 Channel 0 Shift Data Output**
	TMS_C	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. C is selected during start-up, an internal pull-up device will hold this pin low when nothing is driving it.
	U0C1_DX0F	I	St/B	**USIC0 Channel 1 Shift Data Input**
8	P7.1	O0 / I	St/B	**Bit 1 of Port 7, General Purpose Input/Output**
	EXTCLK	O1	St/B	**Programmable Clock Signal Output**
	TXDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	$\overline{\text{BRKIN\_C}}$	I	St/B	**OCDS Break Signal Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
33	P5.11	I	In/A	**Bit 11 of Port 5, General Purpose Input**
	ADC0_CH11	I	In/A	**Analog Input Channel 11 for ADC0**
	ADC1_CH11	I	In/A	**Analog Input Channel 11 for ADC1**
34	P5.13	I	In/A	**Bit 13 of Port 5, General Purpose Input**
	ADC0_CH13	I	In/A	**Analog Input Channel 13 for ADC0**
35	P5.15	I	In/A	**Bit 15 of Port 5, General Purpose Input**
	ADC0_CH15	I	In/A	**Analog Input Channel 15 for ADC0**
	RxDC2F	I	In/A	**CAN Node 2 Receive Data Input**
36	P2.12	O0 / I	St/B	**Bit 12 of Port 2, General Purpose Input/Output**
	U0C0_SELO 4	O1	St/B	**USIC0 Channel 0 Select/Control 4 Output**
	U0C1_SELO 3	O2	St/B	**USIC0 Channel 1 Select/Control 3 Output**
	TXDC2	O3	St/B	**CAN Node 2 Transmit Data Output**
	READY	IH	St/B	**External Bus Interface READY Input**
37	P2.11	O0 / I	St/B	**Bit 11 of Port 2, General Purpose Input/Output**
	U0C0_SELO 2	O1	St/B	**USIC0 Channel 0 Select/Control 2 Output**
	U0C1_SELO 2	O2	St/B	**USIC0 Channel 1 Select/Control 2 Output**
	$\overline{\text{BHE}}$/$\overline{\text{WRH}}$	OH	St/B	**External Bus Interf. High-Byte Control Output** Can operate either as Byte High Enable ($\overline{\text{BHE}}$) or as Write strobe for High Byte ($\overline{\text{WRH}}$).
39	P2.0	O0 / I	St/B	**Bit 0 of Port 2, General Purpose Input/Output**
	TxDC5	O1	St/B	**CAN Node 5 Transmit Data Output**
	AD13	OH / IH	St/B	**External Bus Interface Address/Data Line 13**
	RxDC0C	I	St/B	**CAN Node 0 Receive Data Input**
	T5INB	I	St/B	**GPT12E Timer T5 Count/Gate Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
82	P10.10	O0 / I	St/B	**Bit 10 of Port 10, General Purpose Input/Output**
	U0C0_SELO 0	O1	St/B	**USIC0 Channel 0 Select/Control 0 Output**
	CCU60_COU T63	O2	St/B	**CCU60 Channel 3 Output**
	AD10	OH / IH	St/B	**External Bus Interface Address/Data Line 10**
	U0C0_DX2C	I	St/B	**USIC0 Channel 0 Shift Control Input**
	U0C1_DX1A	I	St/B	**USIC0 Channel 1 Shift Clock Input**
	TDI_B	IH	St/B	**JTAG Test Data Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.
83	P10.11	O0 / I	St/B	**Bit 11 of Port 10, General Purpose Input/Output**
	U1C0_SCLK OUT	O1	St/B	**USIC1 Channel 0 Shift Clock Output**
	$\overline{\text{BRKOUT}}$	O2	St/B	**OCDS Break Signal Output**
	AD11	OH / IH	St/B	**External Bus Interface Address/Data Line 11**
	U1C0_DX1D	I	St/B	**USIC1 Channel 0 Shift Clock Input**
	RxDC2B	I	St/B	**CAN Node 2 Receive Data Input**
	TMS_B	IH	St/B	**JTAG Test Mode Selection Input** If JTAG pos. B is selected during start-up, an internal pull-up device will hold this pin high when nothing is driving it.

2.2 Identification Registers

The identification registers describe the current version of the XC226xN and of its modules.

Table 7 XC226xN Identification Registers

Short Name	Value	Address	Notes
SCU_IDMANUF	1820_H	$00'F07E_H$	
SCU_IDCHIP	3001_H	$00'F07C_H$	marking EES-AA or ES-AA
	3002_H	$00'F07C_H$	marking AA
SCU_IDMEM	$304F_H$	$00'F07A_H$	
SCU_IDPROG	1313_H	$00'F078_H$	
JTAG_ID	$0018'B083_H$	---	marking EES-AA or ES-AA
	$1018'B083_H$	---	marking AA

Table 8 XC226xN Memory Map (cont'd)[1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
Reserved for DSRAM	$00'8000_H$	$00'9FFF_H$	8 Kbytes	
External memory area	$00'0000_H$	$00'7FFF_H$	32 Kbytes	

1) Accesses to the shaded areas are reserved. In devices with external bus interface these accesses generate external bus accesses.

2) The areas marked with "<" are slightly smaller than indicated, see column "Notes".

3) The uppermost 4-Kbyte sector of the first Flash segment is reserved for internal use ($C0'F000_H$ to $C0'FFFF_H$).

4) Several pipeline optimizations are not active within the external IO area. This is necessary to control external peripherals properly.

This common memory space consists of 16 Mbytes organized as 256 segments of 64 Kbytes; each segment contains four data pages of 16 Kbytes. The entire memory space can be accessed bytewise or wordwise. Portions of the on-chip DPRAM and the register spaces (ESFR/SFR) additionally are directly bit addressable.

The internal data memory areas and the Special Function Register areas (SFR and ESFR) are mapped into segment 0, the system segment.

The Program Management Unit (PMU) handles all code fetches and, therefore, controls access to the program memories such as Flash memory and PSRAM.

The Data Management Unit (DMU) handles all data transfers and, therefore, controls access to the DSRAM and the on-chip peripherals.

Both units (PMU and DMU) are connected to the high-speed system bus so that they can exchange data. This is required if operands are read from program memory, code or data is written to the PSRAM, code is fetched from external memory, or data is read from or written to external resources. These include peripherals on the LXBus such as USIC or MultiCAN. The system bus allows concurrent two-way communication for maximum transfer performance.

Up to 16 Kbytes of on-chip Program SRAM (PSRAM) are provided to store user code or data. The PSRAM is accessed via the PMU and is optimized for code fetches. A section of the PSRAM with programmable size can be write-protected.

Note: The actual size of the PSRAM depends on the quoted device type.

With this hardware most XC226xN instructions are executed in a single machine cycle of 12.5 ns @ 80-MHz CPU clock. For example, shift and rotate instructions are always processed during one machine cycle, no matter how many bits are shifted. Also, multiplication and most MAC instructions execute in one cycle. All multiple-cycle instructions have been optimized so that they can be executed very fast; for example, a 32-/16-bit division is started within 4 cycles while the remaining cycles are executed in the background. Another pipeline optimization, the branch target prediction, eliminates the execution time of branch instructions if the prediction was correct.

The CPU has a register context consisting of up to three register banks with 16 word-wide GPRs each at its disposal. One of these register banks is physically allocated within the on-chip DPRAM area. A Context Pointer (CP) register determines the base address of the active register bank accessed by the CPU at any time. The number of these register bank copies is only restricted by the available internal RAM space. For easy parameter passing, a register bank may overlap others.

A system stack of up to 32 Kwords is provided for storage of temporary data. The system stack can be allocated to any location within the address space (preferably in the on-chip RAM area); it is accessed by the CPU with the stack pointer (SP) register. Two separate SFRs, STKOV and STKUN, are implicitly compared with the stack pointer value during each stack access to detect stack overflow or underflow.

The high performance of the CPU hardware implementation can be best utilized by the programmer with the highly efficient XC226xN instruction set. This includes the following instruction classes:

- Standard Arithmetic Instructions
- DSP-Oriented Arithmetic Instructions
- Logical Instructions
- Boolean Bit Manipulation Instructions
- Compare and Loop Control Instructions
- Shift and Rotate Instructions
- Prioritize Instruction
- Data Movement Instructions
- System Stack Instructions
- Jump and Call Instructions
- Return Instructions
- System Control Instructions
- Miscellaneous Instructions

The basic instruction length is either 2 or 4 bytes. Possible operand types are bits, bytes and words. A variety of direct, indirect or immediate addressing modes are provided to specify the required operands.

to a dedicated vector table location). The occurrence of a hardware trap is also indicated by a single bit in the trap flag register (TFR). Unless another higher-priority trap service is in progress, a hardware trap will interrupt any ongoing program execution. In turn, hardware trap services can normally not be interrupted by standard or PEC interrupts.

Depending on the package option up to 3 External Service Request (ESR) pins are provided. The ESR unit processes their input values and allows to implement user controlled trap functions (System Requests SR0 and SR1). In this way reset, wakeup and power control can be efficiently realized.

Software interrupts are supported by the 'TRAP' instruction in combination with an individual trap (interrupt) number. Alternatively to emulate an interrupt by software a program can trigger interrupt requests by writing the Interrupt Request (IR) bit of an interrupt control register.

3.7 On-Chip Debug Support (OCDS)

The On-Chip Debug Support system built into the XC226xN provides a broad range of debug and emulation features. User software running on the XC226xN can be debugged within the target system environment.

The OCDS is controlled by an external debugging device via the debug interface. This either consists of the 2-pin Device Access Port (DAP) or of the JTAG port conforming to IEEE-1149. The debug interface can be completed with an optional break interface.

The debugger controls the OCDS with a set of dedicated registers accessible via the debug interface (DAP or JTAG). In addition the OCDS system can be controlled by the CPU, e.g. by a monitor program. An injection interface allows the execution of OCDS-generated instructions by the CPU.

Multiple breakpoints can be triggered by on-chip hardware, by software, or by an external trigger input. Single stepping is supported, as is the injection of arbitrary instructions and read/write access to the complete internal address space. A breakpoint trigger can be answered with a CPU halt, a monitor call, a data transfer, or/and the activation of an external signal.

Tracing of data can be obtained via the debug interface, or via the external bus interface for increased performance.

Tracing of program execution is supported by the XC2000 Family emulation device. With this device the DAP can operate on clock rates of up to 20 MHz.

The DAP interface uses two interface signals, the JTAG interface uses four interface signals, to communicate with external circuitry. The debug interface can be amended with two optional break lines.

3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

Note: The number of CAN nodes and message objects depends on the selected device type.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

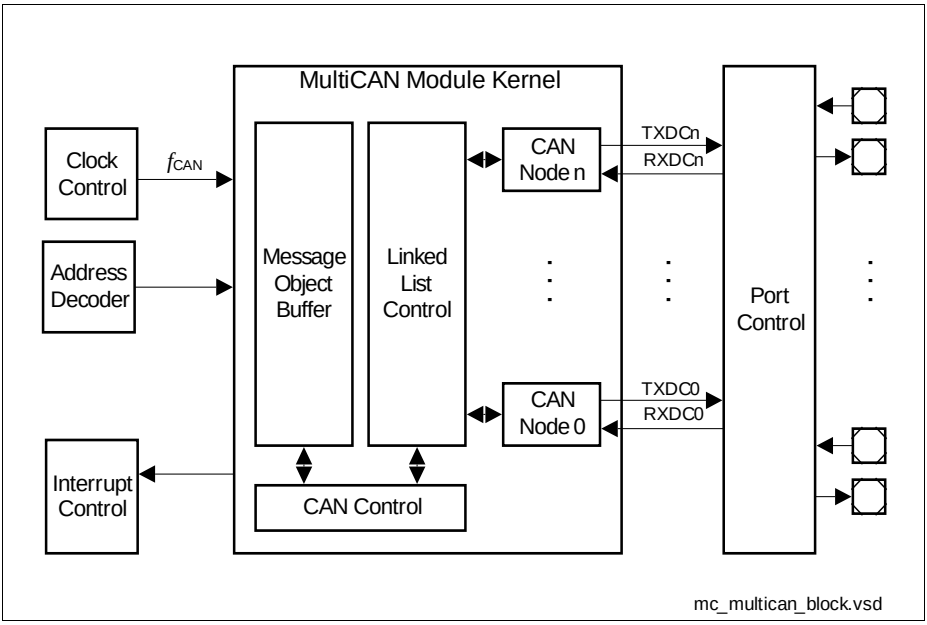

Figure 12 Block Diagram of MultiCAN Module

MultiCAN Features

- CAN functionality conforming to CAN specification V2.0 B active for each CAN node (compliant to ISO 11898)
- Independent CAN nodes
- Set of independent message objects (shared by the CAN nodes)
- Dedicated control registers for each CAN node
- Data transfer rate up to 1 Mbit/s, individually programmable for each node
- Flexible and powerful message transfer control and error handling capabilities
- Full-CAN functionality for message objects:
  - Can be assigned to one of the CAN nodes
  - Configurable as transmit or receive objects, or as message buffer FIFO
  - Handle 11-bit or 29-bit identifiers with programmable acceptance mask for filtering
  - Remote Monitoring Mode, and frame counter for monitoring
- Automatic Gateway Mode support
- 16 individually programmable interrupt nodes
- Analyzer mode for CAN bus monitoring

3.15 System Timer

The System Timer consists of a programmable prescaler and two concatenated timers (10 bits and 6 bits). Both timers can generate interrupt requests. The clock source can be selected and the timers can also run during power reduction modes.

Therefore, the System Timer enables the software to maintain the current time for scheduling functions or for the implementation of a clock.

3.16 Watchdog Timer

The Watchdog Timer is one of the fail-safe mechanisms which have been implemented to prevent the controller from malfunctioning for longer periods of time.

The Watchdog Timer is always enabled after an application reset of the chip. It can be disabled and enabled at any time by executing the instructions DISWDT and ENWDT respectively. The software has to service the Watchdog Timer before it overflows. If this is not the case because of a hardware or software failure, the Watchdog Timer overflows, generating a prewarning interrupt and then a reset request.

The Watchdog Timer is a 16-bit timer clocked with the system clock divided by 16,384 or 256. The Watchdog Timer register is set to a prespecified reload value (stored in WDTREL) in order to allow further variation of the monitored time interval. Each time it is serviced by the application software, the Watchdog Timer is reloaded and the prescaler is cleared.

Time intervals between 3.2 µs and 13.4 s can be monitored (@ 80 MHz).

The default Watchdog Timer interval after power-up is 6.5 ms (@ 10 MHz).

3.19 Power Management

The XC226xN provides the means to control the power it consumes either at a given time or averaged over a certain duration.
Three mechanisms can be used (and partly in parallel):

- **Supply Voltage Management** permits the temporary reduction of the supply voltage of major parts of the logic or even its complete disconnection. This drastically reduces the power consumed because it eliminates leakage current, particularly at high temperature.
  Several power reduction modes provide the best balance of power reduction and wake-up time.
- **Clock Generation Management** controls the frequency of internal and external clock signals. Clock signals for currently inactive parts of logic are disabled automatically. The user can drastically reduce the consumed power by reducing the XC226xN system clock frequency.
  External circuits can be controlled using the programmable frequency output EXTCLK.
- **Peripheral Management** permits temporary disabling of peripheral modules. Each peripheral can be disabled and enabled separately. The CPU can be switched off while the peripherals can continue to operate.

Wake-up from power reduction modes can be triggered either externally with signals generated by the external system, or internally by the on-chip wake-up timer. This supports intermittent operation of the XC226xN by generating cyclic wake-up signals. Full performance is available to quickly react to action requests while the intermittent sleep phases greatly reduce the average system power consumption.

Note: When selecting the supply voltage and the clock source and generation method, the required parameters must be carefully written to the respective bit fields, to avoid unintended intermediate states. Recommended sequences are provided which ensure the intended operation of power supply system and clock system. Please refer to the Programmer's Guide.

4 Electrical Parameters

The operating range for the XC226xN is defined by its electrical parameters. For proper operation the specified limits must be respected when integrating the device in its target environment.

4.1 General Parameters

These parameters are valid for all subsequent descriptions, unless otherwise noted.

Table 12 Absolute Maximum Rating Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output current on a pin when high value is driven	I_{OH} SR	-30	–	–	mA	
Output current on a pin when low value is driven	I_{OL} SR	–	–	30	mA	
Overload current	I_{OV} SR	-10	–	10	mA	1)
Absolute sum of overload currents	$\Sigma\|I_{OV}\|$ SR	–	–	100	mA	1)
Junction Temperature	T_J SR	-40	–	150	°C	
Storage Temperature	T_{ST} SR	-65	–	150	°C	
Digital supply voltage for IO pads and voltage regulators	V_{DDP} SR	-0.5	–	6.0	V	
Voltage on any pin with respect to ground (Vss)	V_{IN} SR	-0.5	–	V_{DDP} + 0.5	V	$V_{IN} \leq V_{DDP(max)}$

1) Overload condition occurs if the input voltage V_{IN} is out of the absolute maximum rating range. In this case the current must be limited to the listed values by design measures.

Note: Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for an extended time may affect device reliability.
During absolute maximum rating overload conditions ($V_{IN} > V_{DDP}$ or $V_{IN} < V_{SS}$) the voltage on V_{DDP} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Table 16 DC Characteristics for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output High voltage[7]	V_{OH} CC	V_{DDP} - 1.0	–	–	V	$I_{OH} \geq I_{OHmax}$
		V_{DDP} - 0.4	–	–	V	$I_{OH} \geq I_{OHnom}$ [8]
Output Low Voltage[7]	V_{OL} CC	–	–	0.4	V	$I_{OL} \leq I_{OLnom}$ [8]
		–	–	1.0	V	$I_{OL} \leq I_{OLmax}$

1) Because each double bond pin is connected to two pads (standard pad and high-speed pad), it has twice the normal value. For a list of affected pins refer to the pin definitions table in chapter 2.

2) Not subject to production test - verified by design/characterization. Hysteresis is implemented to avoid metastable states and switching due to internal ground bounce. It cannot suppress switching due to external system noise under all conditions.

3) If the input voltage exceeds the respective supply voltage due to ground bouncing ($V_{IN} < V_{SS}$) or supply ripple ($V_{IN} > V_{DDP}$), a certain amount of current may flow through the protection diodes. This current adds to the leakage current. An additional error current (I_{INJ}) will flow if an overload current flows through an adjacent pin. Please refer to the definition of the overload coupling factor K_{OV}.

4) The given values are worst-case values. In production test, this leakage current is only tested at 125 °C; other values are ensured by correlation. For derating, please refer to the following descriptions: Leakage derating depending on temperature (T_J = junction temperature [°C]): I_{OZ} = 0.05 x $e^{(1.5 + 0.028 \times TJ>)}$ [µA]. For example, at a temperature of 95 °C the resulting leakage current is 3.2 µA. Leakage derating depending on voltage level (DV = V_{DDP} - V_{PIN} [V]): I_{OZ} = $I_{OZtempmax}$ - (1.6 x DV) (µA]. This voltage derating formula is an approximation which applies for maximum temperature.

5) Drive the indicated minimum current through this pin to change the default pin level driven by the enabled pull device.

6) Limit the current through this pin to the indicated value so that the enabled pull device can keep the default pin level.

7) The maximum deliverable output current of a port driver depends on the selected output driver mode. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is determined by the external circuit.

8) As a rule, with decreasing output current the output levels approach the respective supply level (V_{OL}->V_{SS}, V_{OH}->V_{DDP}). However, only the levels for nominal output currents are verified.

During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA}.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6×f_{SYS} mA.

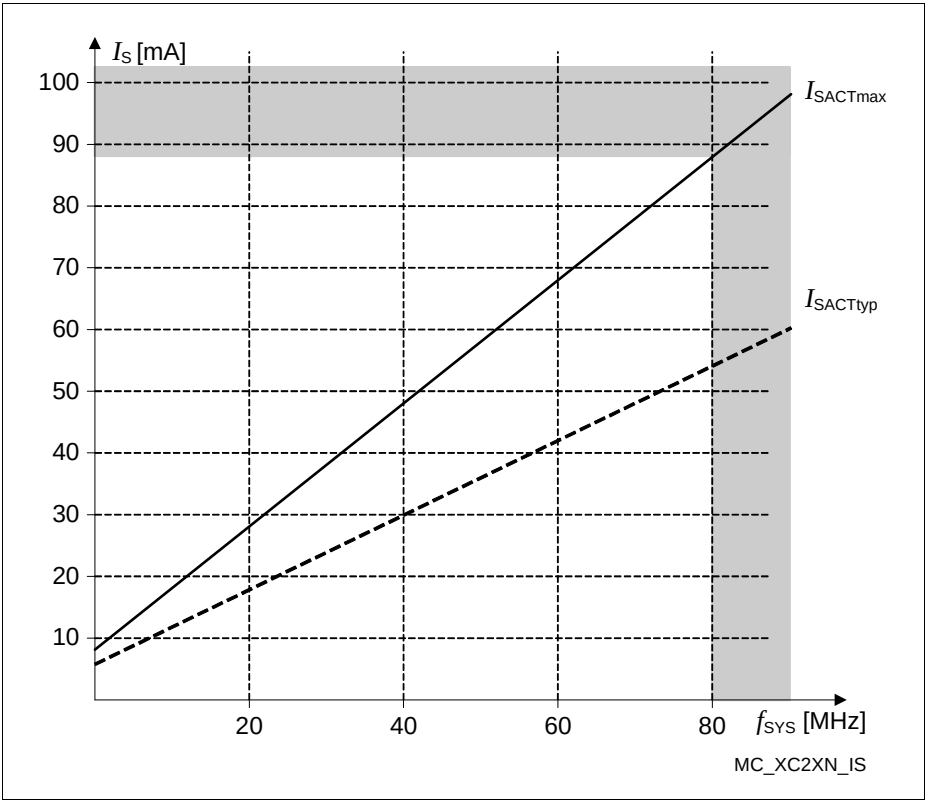

Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Sample time and conversion time of the XC226xN's A/D converters are programmable. The timing above can be calculated using **Table 21**.
The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 21 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time[1] t_S
000000_B	f_{SYS}	00_H	$t_{ADCI} \times 2$
000001_B	f_{SYS} / 2	01_H	$t_{ADCI} \times 3$
000010_B	f_{SYS} / 3	02_H	$t_{ADCI} \times 4$
:	f_{SYS} / (DIVA+1)	:	$t_{ADCI} \times$ (STC+2)
111110_B	f_{SYS} / 63	FE_H	$t_{ADCI} \times 256$
111111_B	f_{SYS} / 64	FF_H	$t_{ADCI} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: f_{SYS} = 80 MHz (i.e. t_{SYS} = 12.5 ns), DIVA = 03_H, STC = 00_H
Analog clock f_{ADCI} = f_{SYS} / 4 = 20 MHz, i.e. t_{ADCI} = 50 ns
Sample time t_S = $t_{ADCI} \times 2$ = 100 ns

Conversion 10-bit:

$t_{C10} = 13 \times t_{ADCI} + 2 \times t_{SYS} = 13 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.675\ \mu s$

Conversion 8-bit:

$t_{C8} = 11 \times t_{ADCI} + 2 \times t_{SYS} = 11 \times 50\text{ ns} + 2 \times 12.5\text{ ns} = 0.575\ \mu s$

Converter Timing Example B:

Assumptions: f_{SYS} = 40 MHz (i.e. t_{SYS} = 25 ns), DIVA = 02_H, STC = 03_H
Analog clock f_{ADCI} = f_{SYS} / 3 = 13.3 MHz, i.e. t_{ADCI} = 75 ns
Sample time t_S = $t_{ADCI} \times 5$ = 375 ns

Conversion 10-bit:

$t_{C10} = 16 \times t_{ADCI} + 2 \times t_{SYS} = 16 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.25\ \mu s$

Conversion 8-bit:

$t_{C8} = 14 \times t_{ADCI} + 2 \times t_{SYS} = 14 \times 75\text{ ns} + 2 \times 25\text{ ns} = 1.10\ \mu s$

Table 23 Coding of bit fields LEVxV in Register SWDCON0 (cont'd)

Code	Default Voltage Level	Notes[1)]
0010_B	3.1 V	
0011_B	3.2 V	
0100_B	3.3 V	
0101_B	3.4 V	
0110_B	3.6 V	
0111_B	4.0 V	
1000_B	4.2 V	
1001_B	4.5 V	LEV2V: no request
1010_B	4.6 V	
1011_B	4.7 V	
1100_B	4.8 V	
1101_B	4.9 V	
1110_B	5.0 V	
1111_B	5.5 V	

1) The indicated default levels are selected automatically after a power reset.

Table 24 Coding of bit fields LEVxV in Registers PVCyCONz

Code	Default Voltage Level	Notes[1)]
000_B	0.95 V	
001_B	1.05 V	
010_B	1.15 V	
011_B	1.25 V	
100_B	1.35 V	LEV1V: reset request
101_B	1.45 V	LEV2V: interrupt request[2)]
110_B	1.55 V	
111_B	1.65 V	

1) The indicated default levels are selected automatically after a power reset.

2) Due to variations of the tolerance of both the Embedded Voltage Regulators (EVR) and the PVC levels, this interrupt can be triggered inadvertently, even though the core voltage is within the normal range. It is, therefore, recommended not to use this warning level.

Variable Memory Cycles

External bus cycles of the XC226xN are executed in five consecutive cycle phases (AB, C, D, E, F). The duration of each cycle phase is programmable (via the TCONCSx registers) to adapt the external bus cycles to the respective external module (memory, peripheral, etc.).

The duration of the access phase can optionally be controlled by the external module using the READY handshake input.

This table provides a summary of the phases and the ranges for their length.

Table 31 Programmable Bus Cycle Phases (see timing diagrams)

Bus Cycle Phase	Parameter	Valid Values	Unit
Address setup phase, the standard duration of this phase (1 … 2 TCS) can be extended by 0 … 3 TCS if the address window is changed	tpAB	1 … 2 (5)	TCS
Command delay phase	tpC	0 … 3	TCS
Write Data setup/MUX Tristate phase	tpD	0 … 1	TCS
Access phase	tpE	1 … 32	TCS
Address/Write Data hold phase	tpF	0 … 3	TCS

Note: The bandwidth of a parameter (from minimum to maximum value) covers the whole operating range (temperature, voltage) as well as process variations. Within a given device, however, this bandwidth is smaller than the specified range. This is also due to interdependencies between certain parameters. Some of these interdependencies are described in additional notes (see standard timing).

Note: Operating Conditions apply.

Table 32 is valid under the following conditions: C_L= 20 pF; voltage_range= upper ; voltage_range= upper

Table 32 External Bus Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Output valid delay for $\overline{RD}$, $\overline{WR}$($\overline{L}$/$\overline{H}$)	t_{10} CC	–	7	13	ns	
Output valid delay for $\overline{BHE}$, ALE	t_{11} CC	–	7	14	ns	
Address output valid delay for A23 ... A0	t_{12} CC	–	8	14	ns	

4.7.6 Synchronous Serial Interface Timing

The following parameters are applicable for a USIC channel operated in SSC mode.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 34 is valid under the following conditions: C_L= 20 pF; *SSC*= master ; voltage_range= upper

Table 34 USIC SSC Master Mode Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Slave select output SELO active to first SCLKOUT transmit edge	t_1 CC	t_{SYS} - 8[1)]	–	–	ns	
Slave select output SELO inactive after last SCLKOUT receive edge	t_2 CC	t_{SYS} - 6[1)]	–	–	ns	
Data output DOUT valid time	t_3 CC	-6	–	9	ns	
Receive data input setup time to SCLKOUT receive edge	t_4 SR	31	–	–	ns	
Data input DX0 hold time from SCLKOUT receive edge	t_5 SR	-4	–	–	ns	

1) $t_{SYS} = 1 / f_{SYS}$

Table 35 is valid under the following conditions: C_L= 20 pF; *SSC*= master ; voltage_range= lower