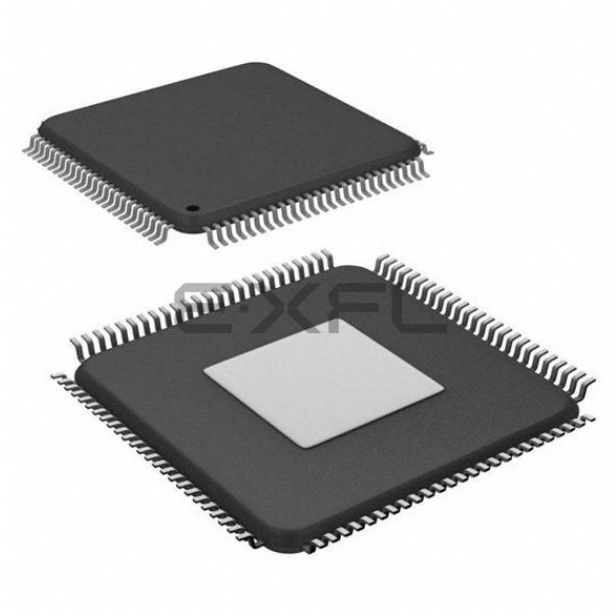
Infineon Technologies - XC2263N40F80LABKXUMA1 Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I²C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I²S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	42K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2263n40f80labkxuma1

2.1 Pin Configuration and Definition

The pins of the XC226xN are described in detail in **Table 6**, which includes all alternate functions. For further explanations please refer to the footnotes at the end of the table. The following figure summarizes all pins, showing their locations on the four sides of the package.

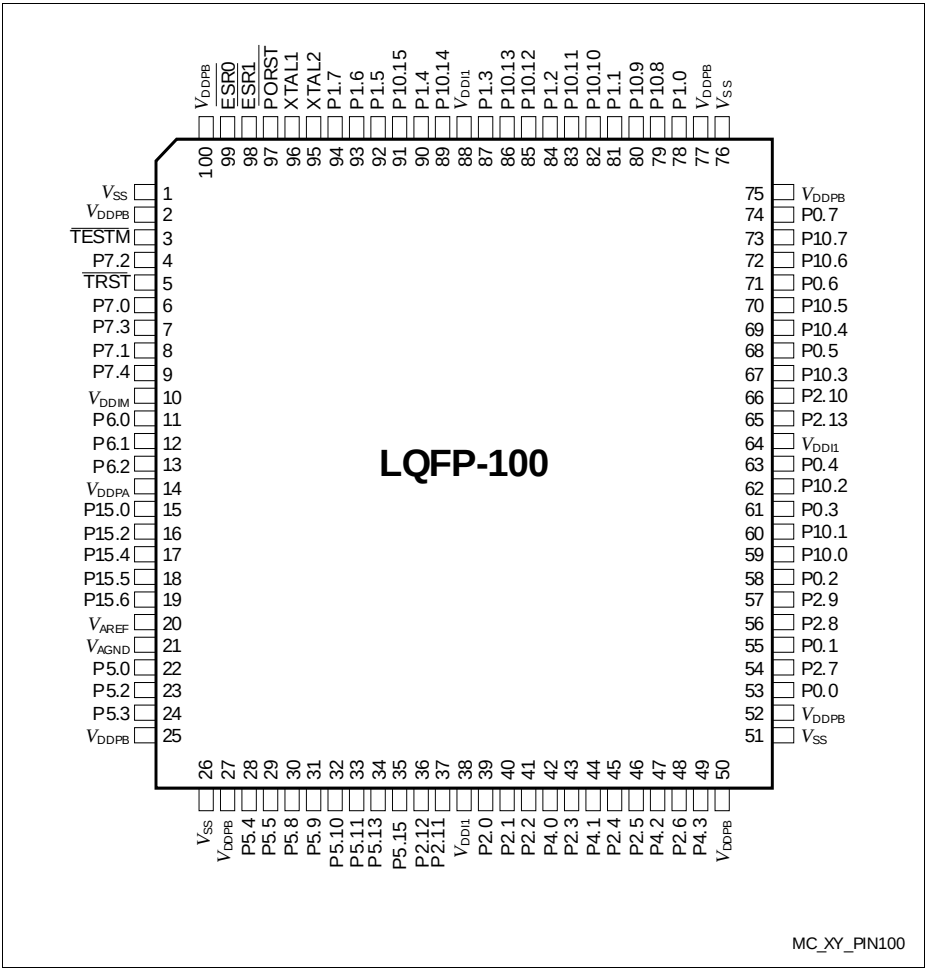

Figure 3 XC226xN Pin Configuration (top view)

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
72	P10.6	O0 / I	St/B	**Bit 6 of Port 10, General Purpose Input/Output**
	U0C0_DOUT	O1	St/B	**USIC0 Channel 0 Shift Data Output**
	TxDC4	O2	St/B	**CAN Node 4 Transmit Data Output**
	U1C0_SELO 0	O3	St/B	**USIC1 Channel 0 Select/Control 0 Output**
	AD6	OH / IH	St/B	**External Bus Interface Address/Data Line 6**
	U0C0_DX0C	I	St/B	**USIC0 Channel 0 Shift Data Input**
	U1C0_DX2D	I	St/B	**USIC1 Channel 0 Shift Control Input**
	CCU60_CTR APA	I	St/B	**CCU60 Emergency Trap Input**
73	P10.7	O0 / I	St/B	**Bit 7 of Port 10, General Purpose Input/Output**
	U0C1_DOUT	O1	St/B	**USIC0 Channel 1 Shift Data Output**
	CCU60_COU T63	O2	St/B	**CCU60 Channel 3 Output**
	AD7	OH / IH	St/B	**External Bus Interface Address/Data Line 7**
	U0C1_DX0B	I	St/B	**USIC0 Channel 1 Shift Data Input**
	CCU60_CCP OS0A	I	St/B	**CCU60 Position Input 0**
	RxDC4C	I	St/B	**CAN Node 4 Receive Data Input**
	T4INB	I	St/B	**GPT12E Timer T4 Count/Gate Input**
74	P0.7	O0 / I	St/B	**Bit 7 of Port 0, General Purpose Input/Output**
	U1C1_DOUT	O1	St/B	**USIC1 Channel 1 Shift Data Output**
	U1C0_SELO 3	O2	St/B	**USIC1 Channel 0 Select/Control 3 Output**
	TxDC3	O3	St/B	**CAN Node 3 Transmit Data Output**
	A7	OH	St/B	**External Bus Interface Address Line 7**
	U1C1_DX0B	I	St/B	**USIC1 Channel 1 Shift Data Input**
	CCU61_CTR APB	I	St/B	**CCU61 Emergency Trap Input**

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 25, 27, 50, 52, 75, 77, 100	V_{DDPB}	-	PS/B	**Digital Pad Supply Voltage for Domain B** Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. *Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.*
1, 26, 51, 76	V_{SS}	-	PS/--	**Digital Ground** All V_{SS} pins must be connected to the ground-line or ground-plane. *Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground.* *For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.*

1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

3.1 Memory Subsystem and Organization

The memory space of the XC226xN is configured in the von Neumann architecture. In this architecture all internal and external resources, including code memory, data memory, registers and I/O ports, are organized in the same linear address space.

Table 8 XC226xN Memory Map [1)]

Address Area	Start Loc.	End Loc.	Area Size[2)]	Notes
IMB register space	FF'FF00$_H$	FF'FFFF$_H$	256 Bytes	
Reserved	F0'0000$_H$	FF'FEFF$_H$	< 1 Mbyte	Minus IMB registers
Reserved for EPSRAM	E8'4000$_H$	EF'FFFF$_H$	496 Kbytes	Mirrors EPSRAM
Emulated PSRAM	E8'0000$_H$	E8'3FFF$_H$	up to 16 Kbytes	With Flash timing
Reserved for PSRAM	E0'4000$_H$	E7'FFFF$_H$	496 Kbytes	Mirrors PSRAM
PSRAM	E0'0000$_H$	E0'3FFF$_H$	up to 16 Kbytes	Program SRAM
Reserved for Flash	C5'0000$_H$	DF'FFFF$_H$	1,728 Kbytes	
Flash 1	C4'0000$_H$	C4'FFFF$_H$	64 Kbytes	
Flash 0	C0'0000$_H$	C3'FFFF$_H$	256 Kbytes[3)]	Minus res. seg.
External memory area	40'0000$_H$	BF'FFFF$_H$	8 Mbytes	
External IO area[4)]	21'0000$_H$	3F'FFFF$_H$	1,984 Kbytes	
Reserved	20'BC00$_H$	20'FFFF$_H$	17 Kbytes	
USIC0–2 alternate regs.	20'B000$_H$	20'BBFF$_H$	3 Kbytes	Accessed via EBC
MultiCAN alternate regs.	20'8000$_H$	20'AFFF$_H$	12 Kbytes	Accessed via EBC
Reserved	20'5800$_H$	20'7FFF$_H$	10 Kbytes	
USIC0–2 registers	20'4000$_H$	20'57FF$_H$	6 Kbytes	Accessed via EBC
Reserved	20'6800$_H$	20'7FFF$_H$	6 Kbytes	
MultiCAN registers	20'0000$_H$	20'3FFF$_H$	16 Kbytes	Accessed via EBC
External memory area	01'0000$_H$	1F'FFFF$_H$	1984 Kbytes	
SFR area	00'FE00$_H$	00'FFFF$_H$	0.5 Kbytes	
Dualport RAM (DPRAM)	00'F600$_H$	00'FDFF$_H$	2 Kbytes	
Reserved for DPRAM	00'F200$_H$	00'F5FF$_H$	1 Kbytes	
ESFR area	00'F000$_H$	00'F1FF$_H$	0.5 Kbytes	
XSFR area	00'E000$_H$	00'EFFF$_H$	4 Kbytes	
Data SRAM (DSRAM)	00'A000$_H$	00'DFFF$_H$	16 Kbytes	

3.2 External Bus Controller

All external memory access operations are performed by a special on-chip External Bus Controller (EBC). The EBC also controls access to resources connected to the on-chip LXBus (MultiCAN and the USIC modules). The LXBus is an internal representation of the external bus that allows access to integrated peripherals and modules in the same way as to external components.

The EBC can be programmed either to Single Chip Mode, when no external memory is required, or to an external bus mode with the following selections[1]:

- Address Bus Width with a range of 0 … 24-bit
- Data Bus Width 8-bit or 16-bit
- Bus Operation Multiplexed or Demultiplexed

The bus interface uses Port 10 and Port 2 for addresses and data. In the demultiplexed bus modes, the lower addresses are output separately on Port 0 and Port 1. The number of active segment address lines is selectable, restricting the external address space to 8 Mbytes … 64 Kbytes. This is required when interface lines shall be assigned to Port 2.

External $\overline{CS}$ signals (address windows plus default) can be generated and output on Port 4 in order to save external glue logic. External modules can be directly connected to the common address/data bus and their individual select lines.

Important timing characteristics of the external bus interface are programmable (with registers TCONCSx/FCONCSx) to allow the user to adapt it to a wide range of different types of memories and external peripherals.
Access to very slow memories or modules with varying access times is supported by a special ‘Ready’ function. The active level of the control input signal is selectable.

In addition, up to four independent address windows may be defined (using registers ADDRSELx) to control access to resources with different bus characteristics. These address windows are arranged hierarchically where window 4 overrides window 3, and window 2 overrides window 1. All accesses to locations not covered by these four address windows are controlled by TCONCS0/FCONCS0. The currently active window can generate a chip select signal.

The external bus timing is based on the rising edge of the reference clock output CLKOUT. The external bus protocol is compatible with that of the standard C166 Family.

1) Bus modes are switched dynamically if several address windows with different mode settings are used.

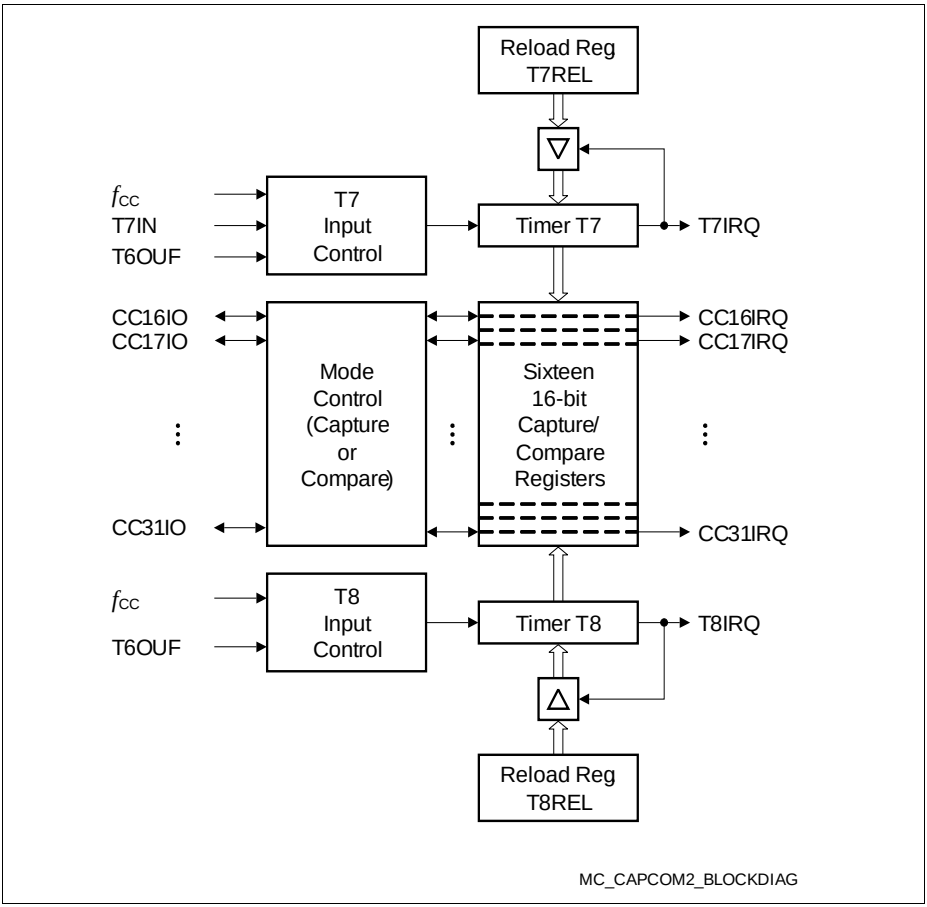

Figure 6 CAPCOM Unit Block Diagram

With its maximum resolution of 2 system clock cycles, the **GPT2 module** provides precise event control and time measurement. It includes two timers (T5, T6) and a capture/reload register (CAPREL). Both timers can be clocked with an input clock which is derived from the CPU clock via a programmable prescaler or with external signals. The counting direction (up/down) for each timer can be programmed by software or altered dynamically with an external signal on a port pin (TxEUD[1)]). Concatenation of the timers is supported with the output toggle latch (T6OTL) of timer T6, which changes its state on each timer overflow/underflow.

The state of this latch may be used to clock timer T5, and/or it may be output on pin T6OUT. The overflows/underflows of timer T6 can also be used to clock the CAPCOM2 timers and to initiate a reload from the CAPREL register.

The CAPREL register can capture the contents of timer T5 based on an external signal transition on the corresponding port pin (CAPIN); timer T5 may optionally be cleared after the capture procedure. This allows the XC226xN to measure absolute time differences or to perform pulse multiplication without software overhead.

The capture trigger (timer T5 to CAPREL) can also be generated upon transitions of GPT1 timer T3 inputs T3IN and/or T3EUD. This is especially advantageous when T3 operates in Incremental Interface Mode.

1) Exception: T5EUD is not connected to a pin.

3.11 Real Time Clock

The Real Time Clock (RTC) module of the XC226xN can be clocked with a clock signal selected from internal sources or external sources (pins).

The RTC basically consists of a chain of divider blocks:

- Selectable 32:1 and 8:1 dividers (on - off)
- The reloadable 16-bit timer T14
- The 32-bit RTC timer block (accessible via registers RTCH and RTCL) consisting of:
  - a reloadable 10-bit timer
  - a reloadable 6-bit timer
  - a reloadable 6-bit timer
  - a reloadable 10-bit timer

All timers count up. Each timer can generate an interrupt request. All requests are combined to a common node request.

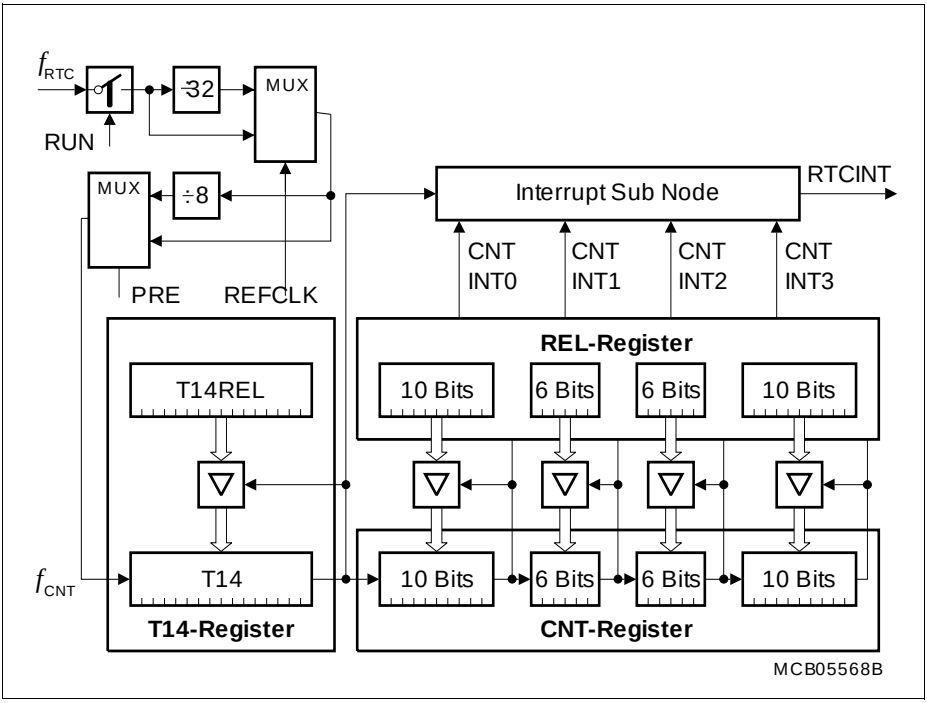

Figure 10 RTC Block Diagram

Note: The registers associated with the RTC are only affected by a power reset.

3.13 Universal Serial Interface Channel Modules (USIC)

The XC226xN features the USIC modules USIC0, USIC1, USIC2. Each module provides two serial communication channels.

The Universal Serial Interface Channel (USIC) module is based on a generic data shift and data storage structure which is identical for all supported serial communication protocols. Each channel supports complete full-duplex operation with a basic data buffer structure (one transmit buffer and two receive buffer stages). In addition, the data handling software can use FIFOs.

The protocol part (generation of shift clock/data/control signals) is independent of the general part and is handled by protocol-specific preprocessors (PPPs).

The USIC's input/output lines are connected to pins by a pin routing unit. The inputs and outputs of each USIC channel can be assigned to different interface pins, providing great flexibility to the application software. All assignments can be made during runtime.

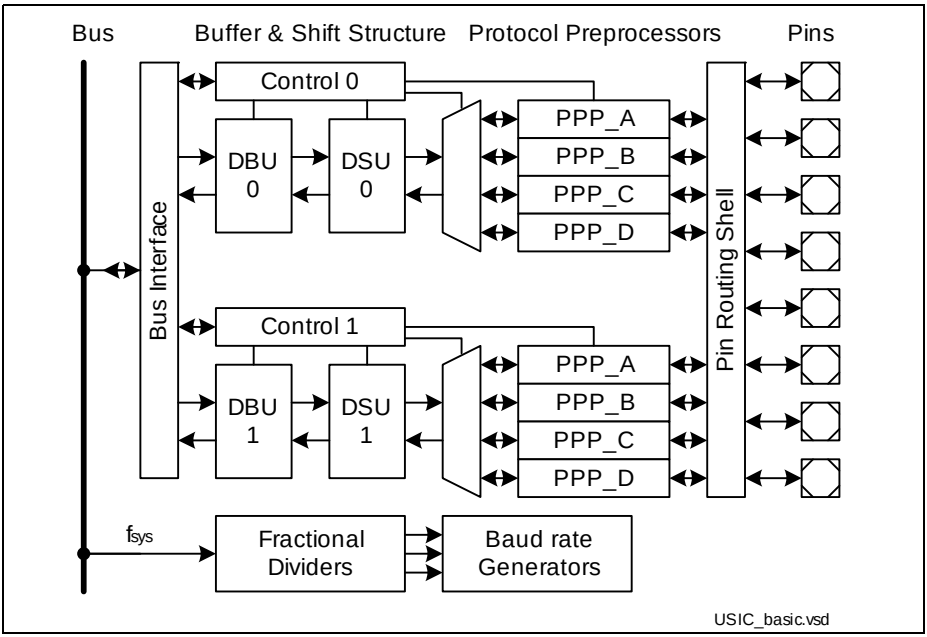

Figure 11 General Structure of a USIC Module

The regular structure of the USIC module brings the following advantages:

- Higher flexibility through configuration with same look-and-feel for data management
- Reduced complexity for low-level drivers serving different protocols
- Wide range of protocols with improved performances (baud rate, buffer handling)

3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

Note: The number of CAN nodes and message objects depends on the selected device type.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

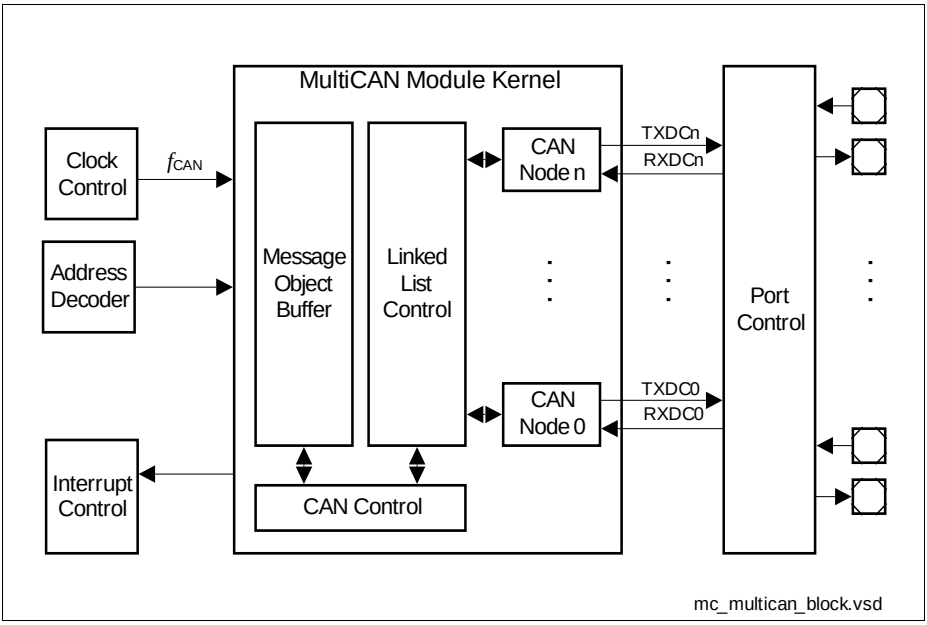

Figure 12 Block Diagram of MultiCAN Module

3.17 Clock Generation

The Clock Generation Unit can generate the system clock signal f_{SYS} for the XC226xN from a number of external or internal clock sources:

- External clock signals with pad voltage or core voltage levels
- External crystal or resonator using the on-chip oscillator
- On-chip clock source for operation without crystal/resonator
- Wake-up clock (ultra-low-power) to further reduce power consumption

The programmable on-chip PLL with multiple prescalers generates a clock signal for maximum system performance from standard crystals, a clock input signal, or from the on-chip clock source. See also **Section 4.7.2**.

The Oscillator Watchdog (OWD) generates an interrupt if the crystal oscillator frequency falls below a certain limit or stops completely. In this case, the system can be supplied with an emergency clock to enable operation even after an external clock failure.

All available clock signals can be output on one of two selectable pins.

4.3.3 Power Consumption

The power consumed by the XC226xN depends on several factors such as supply voltage, operating frequency, active circuits, and operating temperature. The power consumption specified here consists of two components:

- The switching current I_S depends on the device activity
- The leakage current I_{LK} depends on the device temperature

To determine the actual power consumption, always both components, switching current I_S and leakage current I_{LK} must be added:

$I_{DDP} = I_S + I_{LK}$.

Note: The power consumption values are not subject to production test. They are verified by design/characterization.
To determine the total power consumption for dimensioning the external power supply, also the pad driver currents must be considered.

The given power consumption parameters and their values refer to specific operating conditions:

- **Active mode**:
  Regular operation, i.e. peripherals are active, code execution out of Flash.
- **Stopover mode**:
  Crystal oscillator and PLL stopped, Flash switched off, clock in domain DMP_1 stopped.
- **Standby mode**:
  Voltage domain DMP_1 switched off completely, power supply control switched off. DMP_M domain is supplied by ultra low power electronic voltage regulator (ULPEVR). The alternate regulator EVR_M is switched off.

Note: The maximum values cover the complete specified operating range of all manufactured devices.
The typical values refer to average devices under typical conditions, such as nominal supply voltage, room temperature, application-oriented activity.
After a power reset, the decoupling capacitors for V_{DDIM} and V_{DDI1} are charged with the maximum possible current.

For additional information, please refer to **Section 5.2**, **Thermal Considerations**.

Note: Operating Conditions apply.

During operation domain A draws a maximum current of 1.5 mA for each active A/D converter module from V_{DDPA}.

In Fast Startup Mode (with the Flash modules deactivated), the typical current is reduced to 3 + 0.6×f_{SYS} mA.

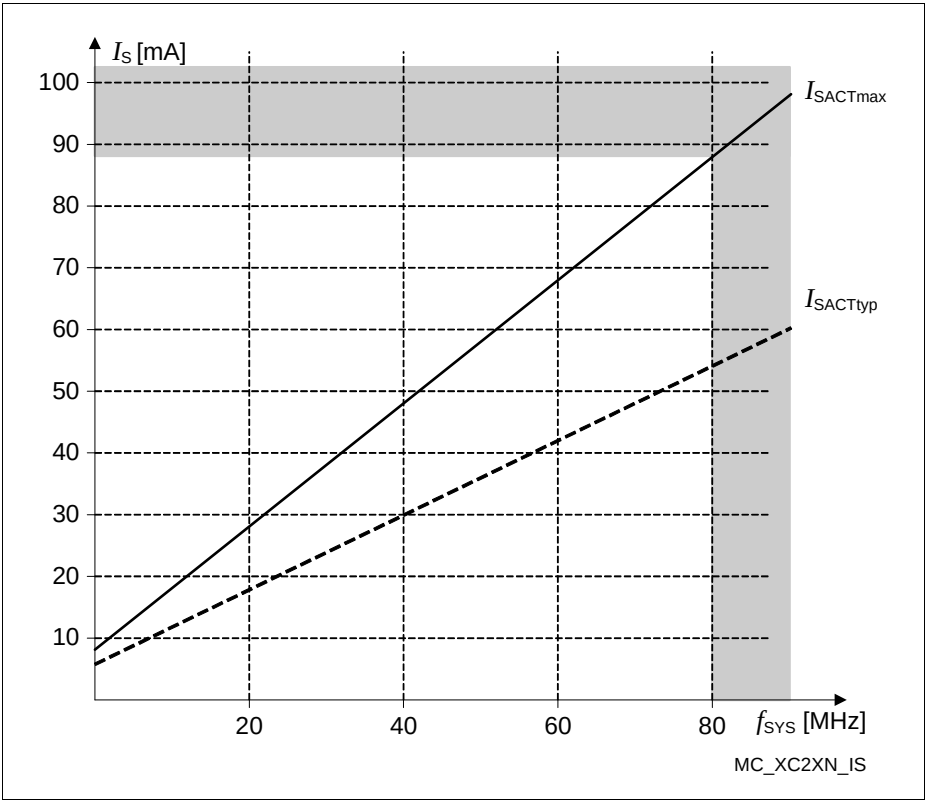

Figure 14 Supply Current in Active Mode as a Function of Frequency

Note: Operating Conditions apply.

Table 19 Leakage Power Consumption

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Leakage supply current (DMP_1 off)[1]	I_{LK0} CC	–	20	35	µA	T_J= 25 °C[2]
		–	115	330	µA	T_J= 85 °C[2]
		–	270	880	µA	T_J= 125 °C[2]
		–	420	1,450	µA	T_J= 150 °C[2]
Leakage supply current (DMP_1 powered)[1]	I_{LK1} CC	–	0.03	0.04	mA	T_J= 25 °C[2]
		–	0.5	1.2	mA	T_J= 85 °C[2]
		–	1.9	5.5	mA	T_J= 125 °C[2]
		–	3.9	12.2	mA	T_J= 150 °C[2]

1) The supply current caused by leakage depends mainly on the junction temperature and the supply voltage. The temperature difference between the junction temperature T_J and the ambient temperature T_A must be taken into account. As this fraction of the supply current does not depend on device activity, it must be added to other power consumption values.

2) All inputs (including pins configured as inputs) are set at 0 V to 0.1 V or at V_{DDP} - 0.1 V to V_{DDP} and all outputs (including pins configured as outputs) are disconnected.

Note: A fraction of the leakage current flows through domain DMP_A (pin V_{DDPA}). This current can be calculated as 7,000 $\times e^{-\alpha}$, with α = 5000 / (273 + 1.3 $\times T_J$). For T_J = 150°C, this results in a current of 160 µA.

Leakage Power Consumption Calculation

The leakage power consumption can be calculated according to the following formulas:

$I_{LK0} = 500{,}000 \times e^{-\alpha}$ with $\alpha = 3000 / (273 + B \times T_J)$

Parameter B must be replaced by

- 1.0 for typical values
- 1.6 for maximum values

$I_{LK1} = 530{,}000 \times e^{-\alpha}$ with $\alpha = 5000 / (273 + B \times T_J)$

Parameter B must be replaced by

- 1.0 for typical values
- 1.3 for maximum values

4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 20 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at an analog input	C_{AINSW} CC	–	–	4	pF	not subject to production test [1]
Total capacitance at an analog input	C_{AINT} CC	–	–	10	pF	not subject to production test [1]
Switched capacitance at the reference input	C_{AREFSW} CC	–	–	7	pF	not subject to production test [1]
Total capacitance at the reference input	C_{AREFT} CC	–	–	15	pF	not subject to production test [1]
Differential Non-Linearity Error	$\lvert EA_{DNL}\rvert$ CC	–	0.8	1	LSB	
Gain Error	$\lvert EA_{GAIN}\rvert$ CC	–	0.4	0.8	LSB	
Integral Non-Linearity	$\lvert EA_{INL}\rvert$ CC	–	0.8	1.2	LSB	
Offset Error	$\lvert EA_{OFF}\rvert$ CC	–	0.5	0.8	LSB	
Analog clock frequency	f_{ADCI} SR	0.5	–	16.5	MHz	voltage_range= lower
		0.5	–	20	MHz	voltage_range= upper
Input resistance of the selected analog channel	R_{AIN} CC	–	–	2	kOhm	not subject to production test [1]
Input resistance of the reference input	R_{AREF} CC	–	–	2	kOhm	not subject to production test [1]

Table 20 ADC Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Broken wire detection delay against VAGND[2]	t_{BWG} CC	–	–	50[3]		
Broken wire detection delay against VAREF[2]	t_{BWR} CC	–	–	50[4]		
Conversion time for 8-bit result[2]	t_{c8} CC	(11+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Conversion time for 10-bit result[2]	t_{c10} CC	(13+STC) x t_{ADCI} + 2 x t_{SYS}	–	–		
Total Unadjusted Error	|TUE| CC	–	1	2	LSB	[5]
Wakeup time from analog powerdown, fast mode	t_{WAF} CC	–	–	4	µs	
Wakeup time from analog powerdown, slow mode	t_{WAS} CC	–	–	15	µs	
Analog reference ground	V_{AGND} SR	V_{SS} - 0.05	–	1.5	V	
Analog input voltage range	V_{AIN} SR	V_{AGND}	–	V_{AREF}	V	[6]
Analog reference voltage	V_{AREF} SR	V_{AGND} + 1.0	–	V_{DDPA} + 0.05	V	

1) These parameter values cover the complete operating range. Under relaxed operating conditions (temperature, supply voltage) typical values can be used for calculation. At room temperature and nominal supply voltage the following typical values can be used: $C_{AINTtyp}$ = 12 pF, $C_{AINStyp}$ = 5 pF, R_{AINtyp} = 1.0 kOhm, $C_{AREFTtyp}$ = 15 pF, $C_{AREFStyp}$ = 10 pF, $R_{AREFtyp}$ = 1.0 kOhm.

2) This parameter includes the sample time (also the additional sample time specified by STC), the time to determine the digital result and the time to load the result register with the conversion result. Values for the basic clock t_{ADCI} depend on programming.

3) The broken wire detection delay against V_{AGND} is measured in numbers of consecutive precharge cycles at a conversion rate of not more than 500 µs. Result below 10% (66_H)

1) The amplitude voltage V_{AX1} refers to the offset voltage V_{OFF}. This offset voltage must be stable during the operation and the resulting voltage peaks must remain within the limits defined by V_{IX1}.
2) Overload conditions must not occur on pin XTAL1.

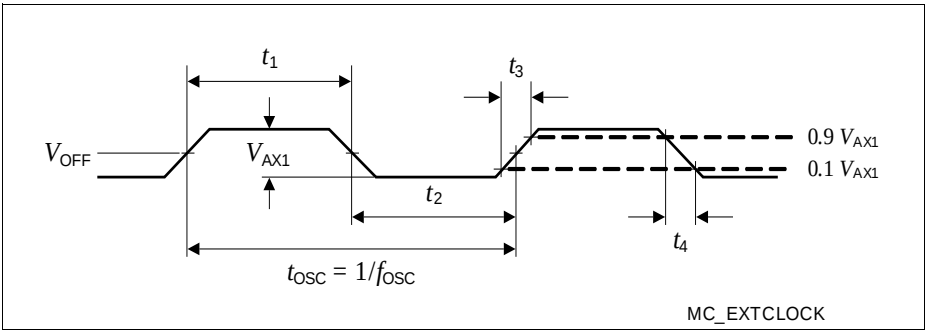

Figure 21 External Clock Drive XTAL1

Note: For crystal or ceramic resonator operation, it is strongly recommended to measure the oscillation allowance (negative resistance) in the final target system (layout) to determine the optimum parameters for oscillator operation.
The manufacturers of crystals and ceramic resonators offer an oscillator evaluation service. This evaluation checks the crystal/resonator specification limits to ensure a reliable oscillator operation.

Table 29 Standard Pad Parameters for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	–	–	37 + 0.65 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Medium
		–	–	24 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Medium
		–	–	6.2 + 0.24 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		–	–	34 + 0.3 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Strong ; Driver_Edge= Slow
		–	–	500 + 2.5 x C_L	ns	$C_L \geq$ 20 pF; $C_L \leq$ 100 pF; Driver_Strength = Weak

1) An output current above $|I_{OXnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and Σ-I_{OH}) must remain below 50 mA.

Table 32 External Bus Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Address output valid delay for AD15 ... AD0 (MUX mode)	t_{13} CC	–	8	15	ns	
Output valid delay for $\overline{CS}$	t_{14} CC	–	7	13	ns	
Data output valid delay for AD15 ... AD0 (write data, MUX mode)	t_{15} CC	–	8	15	ns	
Data output valid delay for D15 ... D0 (write data, DEMUX mode)	t_{16} CC	–	8	15	ns	
Output hold time for $\overline{RD}$, $\overline{WR}$($\overline{L}$/$\overline{H}$)	t_{20} CC	-2	6	8	ns	
Output hold time for $\overline{BHE}$, ALE	t_{21} CC	-2	6	10	ns	
Address output hold time for AD15 ... AD0	t_{23} CC	-3	6	8	ns	
Output hold time for $\overline{CS}$	t_{24} CC	-3	6	11	ns	
Data output hold time for D15 ... D0 and AD15 ... AD0	t_{25} CC	-3	6	8	ns	
Input setup time for READY, D15 ... D0, AD15 ... AD0	t_{30} SR	25	15	–	ns	
Input hold time READY, D15 ... D0, AD15 ... AD0[1)]	t_{31} SR	0	-7	–	ns	

1) Read data are latched with the same internal clock edge that triggers the address change and the rising edge of RD. Address changes before the end of RD have no impact on (demultiplexed) read cycles. Read data can change after the rising edge of RD.

Table 33 is valid under the following conditions: C_L= 20 pF; voltage_range= lower ; voltage_range= lower

Table 41 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	–	–	ns	
TDO valid from TCK falling edge (propagation delay)[1]	t_8 CC	–	32	36	ns	
TDO high impedance to valid output from TCK falling edge[2)1]	t_9 CC	–	32	36	ns	
TDO valid output to high impedance from TCK falling edge[1]	t_{10} CC	–	32	36	ns	
TDO hold after TCK falling edge[1]	t_{18} CC	5	–	–	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

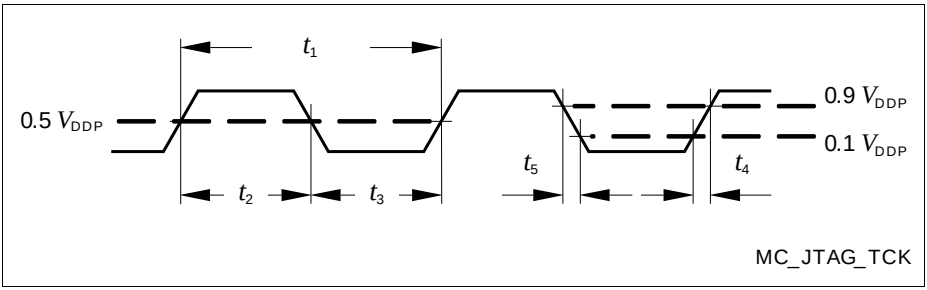

Figure 30 Test Clock Timing (TCK)