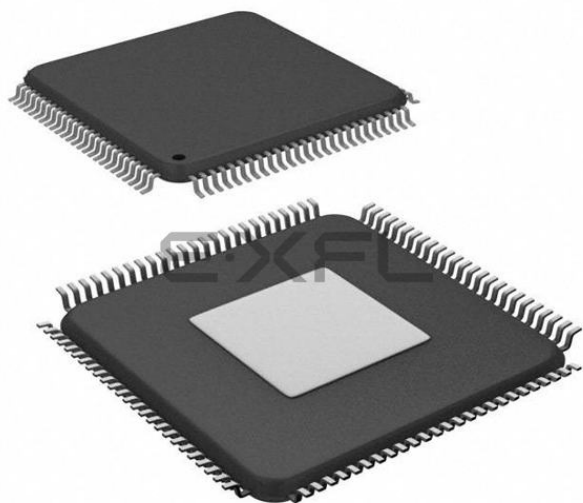




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	C166SV2
Core Size	16/32-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, I ² C, LINbus, SPI, SSC, UART/USART, USI
Peripherals	I ² S, POR, PWM, WDT
Number of I/O	76
Program Memory Size	320KB (320K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	42K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 16x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP Exposed Pad
Supplier Device Package	PG-LQFP-100-8
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/xc2268n40f80labkxuma1

1.2 Special Device Types

Special device types are only available for high-volume applications on request.

Table 2 Synopsis of XC226xN Special Device Types

Derivative¹⁾	Flash Memory²⁾	PSRAM DSRAM³⁾	Capt./Comp. Modules	ADC⁴⁾ Chan.	Interfaces⁴⁾
XC2261N-24FxL	192 Kbytes	4 Kbytes 4 Kbytes	CC2 CCU60/1	11 + 0	1 CAN Node, 2 Serial Chan.
XC2263N-16FxL	128 Kbytes	4 Kbytes 4 Kbytes	CC2 CCU60/1	11 + 5	1 CAN Node, 4 Serial Chan.
XC2263N-24FxL	192 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60/1	11 + 5	1 CAN Node, 4 Serial Chan.
XC2263N-40FxL	320 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1	11 + 5	1 CAN Node, 4 Serial Chan.
XC2264N-16FxL	128 Kbytes	4 Kbytes 4 Kbytes	CC2 CCU60/1	8 + 0	2 CAN Node, 4 Serial Chan.
XC2264N-24FxL	192 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60/1	8 + 0	2 CAN Node, 4 Serial Chan.
XC2264N-40FxL	320 Kbytes	16 Kbytes 16 Kbytes	CC2 CCU60/1	8 + 0	2 CAN Node, 4 Serial Chan.
XC2265N-16FxL	128 Kbytes	4 Kbytes 4 Kbytes	CC2 CCU60/1	11 + 5	3 CAN Node, 6 Serial Chan.
XC2265N-24FxL	192 Kbytes	8 Kbytes 8 Kbytes	CC2 CCU60/1	11 + 5	3 CAN Node, 6 Serial Chan.
XC2265N-40FxL	320 Kbytes	8 Kbytes 16 Kbytes	CC2 CCU60/1	11 + 5	3 CAN Node, 6 Serial Chan.

1) x is a placeholder for available speed grade in MHz. Can be 20, 40, 66 or 80.

2) Specific information about the on-chip Flash memory in [Table 3](#).

3) All derivatives additionally provide 8 Kbytes SBRAM and 2 Kbytes DPRAM.

4) Specific information about the available channels in [Table 5](#).

Analog input channels are listed for each Analog/Digital Converter module separately (ADC0 + ADC1).

Summary of Features

Table 5 Interface Channel Association

Total Number	Available Channels / Message Objects
6 CAN nodes	CAN0, CAN1, CAN2, CAN3, CAN4, CAN5 256 message objects
2 serial channels	U0C0, U0C1
4 serial channels	U0C0, U0C1, U1C0, U1C1
6 serial channels	U0C0, U0C1, U1C0, U1C1, U2C0, U2C1

The XC226xN types are offered with several SRAM memory sizes. [Figure 1](#) shows the allocation rules for PSRAM and DSRAM. Note that the rules differ:

- PSRAM allocation starts from the **lower** address
- DSRAM allocation starts from the **higher** address

For example 8 Kbytes of PSRAM will be allocated at E0'0000h-E0'1FFFh and 8 Kbytes of DSRAM will be at 00'C000h-00'DFFFh.

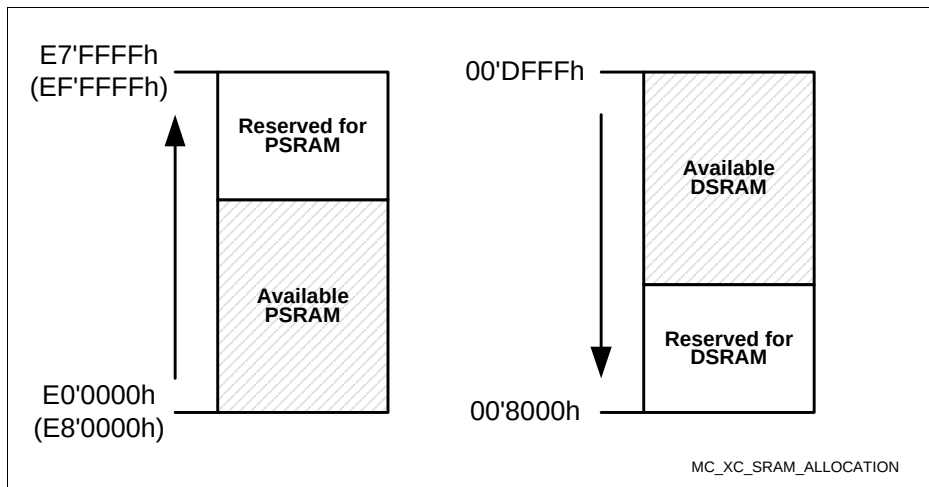


Figure 1 SRAM Allocation

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
24	P5.3	I	In/A	Bit 3 of Port 5, General Purpose Input
	ADC0_CH3	I	In/A	Analog Input Channel 3 for ADC0
	T3INA	I	In/A	GPT12E Timer T3 Count/Gate Input
28	P5.4	I	In/A	Bit 4 of Port 5, General Purpose Input
	ADC0_CH4	I	In/A	Analog Input Channel 4 for ADC0
	T3EUDA	I	In/A	GPT12E Timer T3 External Up/Down Control Input
	TMS_A	I	In/A	JTAG Test Mode Selection Input
29	P5.5	I	In/A	Bit 5 of Port 5, General Purpose Input
	ADC0_CH5	I	In/A	Analog Input Channel 5 for ADC0
	CCU60_T12 HRB	I	In/A	External Run Control Input for T12 of CCU60
30	P5.8	I	In/A	Bit 8 of Port 5, General Purpose Input
	ADC0_CH8	I	In/A	Analog Input Channel 8 for ADC0
	ADC1_CH8	I	In/A	Analog Input Channel 8 for ADC1
	CCU6x_T12H RC	I	In/A	External Run Control Input for T12 of CCU60/1
	CCU6x_T13H RC	I	In/A	External Run Control Input for T13 of CCU60/1
	U2C0_DX0F	I	In/A	USIC2 Channel 0 Shift Data Input
31	P5.9	I	In/A	Bit 9 of Port 5, General Purpose Input
	ADC0_CH9	I	In/A	Analog Input Channel 9 for ADC0
	ADC1_CH9	I	In/A	Analog Input Channel 9 for ADC1
	CC2_T7IN	I	In/A	CAPCOM2 Timer T7 Count Input
32	P5.10	I	In/A	Bit 10 of Port 5, General Purpose Input
	ADC0_CH10	I	In/A	Analog Input Channel 10 for ADC0
	ADC1_CH10	I	In/A	Analog Input Channel 10 for ADC1
	BRKIN_A	I	In/A	OCDS Break Signal Input
	U2C1_DX0F	I	In/A	USIC2 Channel 1 Shift Data Input
	CCU61_T13 HRA	I	In/A	External Run Control Input for T13 of CCU61

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
69	P10.4	O0 / I	St/B	Bit 4 of Port 10, General Purpose Input/Output
	U0C0_SELO3	O1	St/B	USIC0 Channel 0 Select/Control 3 Output
	CCU60_COUT61	O2	St/B	CCU60 Channel 1 Output
	AD4	OH / IH	St/B	External Bus Interface Address/Data Line 4
	U0C0_DX2B	I	St/B	USIC0 Channel 0 Shift Control Input
	U0C1_DX2B	I	St/B	USIC0 Channel 1 Shift Control Input
	ESR1_9	I	St/B	ESR1 Trigger Input 9
70	P10.5	O0 / I	St/B	Bit 5 of Port 10, General Purpose Input/Output
	U0C1_SCLKOUT	O1	St/B	USIC0 Channel 1 Shift Clock Output
	CCU60_COUT62	O2	St/B	CCU60 Channel 2 Output
	U2C0_DOUT	O3	St/B	USIC2 Channel 0 Shift Data Output
	AD5	OH / IH	St/B	External Bus Interface Address/Data Line 5
	U0C1_DX1B	I	St/B	USIC0 Channel 1 Shift Clock Input
71	P0.6	O0 / I	St/B	Bit 6 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	TxDC1	O2	St/B	CAN Node 1 Transmit Data Output
	CCU61_COUT63	O3	St/B	CCU61 Channel 3 Output
	A6	OH	St/B	External Bus Interface Address Line 6
	U1C1_DX0A	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTRAPA	I	St/B	CCU61 Emergency Trap Input
	U1C1_DX1B	I	St/B	USIC1 Channel 1 Shift Clock Input

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
72	P10.6	O0 / I	St/B	Bit 6 of Port 10, General Purpose Input/Output
	U0C0_DOUT	O1	St/B	USIC0 Channel 0 Shift Data Output
	TxDC4	O2	St/B	CAN Node 4 Transmit Data Output
	U1C0_SELO0	O3	St/B	USIC1 Channel 0 Select/Control 0 Output
	AD6	OH / IH	St/B	External Bus Interface Address/Data Line 6
	U0C0_DX0C	I	St/B	USIC0 Channel 0 Shift Data Input
	U1C0_DX2D	I	St/B	USIC1 Channel 0 Shift Control Input
	CCU60_CTR APA	I	St/B	CCU60 Emergency Trap Input
73	P10.7	O0 / I	St/B	Bit 7 of Port 10, General Purpose Input/Output
	U0C1_DOUT	O1	St/B	USIC0 Channel 1 Shift Data Output
	CCU60_COUT63	O2	St/B	CCU60 Channel 3 Output
	AD7	OH / IH	St/B	External Bus Interface Address/Data Line 7
	U0C1_DX0B	I	St/B	USIC0 Channel 1 Shift Data Input
	CCU60_CCP OS0A	I	St/B	CCU60 Position Input 0
	RxDC4C	I	St/B	CAN Node 4 Receive Data Input
	T4INB	I	St/B	GPT12E Timer T4 Count/Gate Input
74	P0.7	O0 / I	St/B	Bit 7 of Port 0, General Purpose Input/Output
	U1C1_DOUT	O1	St/B	USIC1 Channel 1 Shift Data Output
	U1C0_SELO3	O2	St/B	USIC1 Channel 0 Select/Control 3 Output
	TxDC3	O3	St/B	CAN Node 3 Transmit Data Output
	A7	OH	St/B	External Bus Interface Address Line 7
	U1C1_DX0B	I	St/B	USIC1 Channel 1 Shift Data Input
	CCU61_CTR APB	I	St/B	CCU61 Emergency Trap Input

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
97	PORST	I	In/B	Power On Reset Input A low level at this pin resets the XC226xN completely. A spike filter suppresses input pulses <10 ns. Input pulses >100 ns safely pass the filter. The minimum duration for a safe recognition should be 120 ns. An internal pull-up device will hold this pin high when nothing is driving it.
98	ESR1	O0 / I	St/B	External Service Request 1 After power-up, an internal weak pull-up device holds this pin high when nothing is driving it.
	RxDC0E	I	St/B	CAN Node 0 Receive Data Input
	U1C0_DX0F	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2C	I	St/B	USIC1 Channel 0 Shift Control Input
	U1C1_DX0C	I	St/B	USIC1 Channel 1 Shift Data Input
	U1C1_DX2B	I	St/B	USIC1 Channel 1 Shift Control Input
	U2C1_DX2C	I	St/B	USIC2 Channel 1 Shift Control Input
99	ESR0	O0 / I	St/B	External Service Request 0 After power-up, ESR0 operates as open-drain bidirectional reset with a weak pull-up.
	U1C0_DX0E	I	St/B	USIC1 Channel 0 Shift Data Input
	U1C0_DX2B	I	St/B	USIC1 Channel 0 Shift Control Input
10	V _{DDIM}	-	PS/M	Digital Core Supply Voltage for Domain M Decouple with a ceramic capacitor, see Data Sheet for details.
38, 64, 88	V _{DDI1}	-	PS/1	Digital Core Supply Voltage for Domain 1 Decouple with a ceramic capacitor, see Data Sheet for details. All V _{DDI1} pins must be connected to each other.
14	V _{DDPA}	-	PS/A	Digital Pad Supply Voltage for Domain A Connect decoupling capacitors to adjacent V _{DDP} /V _{SS} pin pairs as close as possible to the pins. <i>Note: The A/D Converters and ports P5, P6 and P15 are fed from supply voltage V_{DDPA}.</i>

General Device Information

Table 6 Pin Definitions and Functions (cont'd)

Pin	Symbol	Ctrl.	Type	Function
2, 25, 27, 50, 52, 75, 77, 100	V_{DDPB}	-	PS/B	Digital Pad Supply Voltage for Domain B Connect decoupling capacitors to adjacent V_{DDP}/V_{SS} pin pairs as close as possible to the pins. <i>Note: The on-chip voltage regulators and all ports except P5, P6 and P15 are fed from supply voltage V_{DDPB}.</i>
1, 26, 51, 76	V_{SS}	-	PS/--	Digital Ground All V_{SS} pins must be connected to the ground-line or ground-plane. <i>Note: Also the exposed pad is connected internally to V_{SS}. To improve the EMC behavior, it is recommended to connect the exposed pad to the board ground. For thermal aspects, please refer to the Data Sheet. Board layout examples are given in an application note.</i>

- 1) To generate the reference clock output for bus timing measurement, f_{SYS} must be selected as source for EXTCLK and P2.8 must be selected as output pin. Also the high-speed clock pad must be enabled. This configuration is referred to as reference clock output signal CLKOUT.

Functional Description

Memory Content Protection

The contents of on-chip memories can be protected against soft errors (induced e.g. by radiation) by activating the parity mechanism or the Error Correction Code (ECC).

The parity mechanism can detect a single-bit error and prevent the software from using incorrect data or executing incorrect instructions.

The ECC mechanism can detect and automatically correct single-bit errors. This supports the stable operation of the system.

It is strongly recommended to activate the ECC mechanism wherever possible because this dramatically increases the robustness of an application against such soft errors.

Functional Description

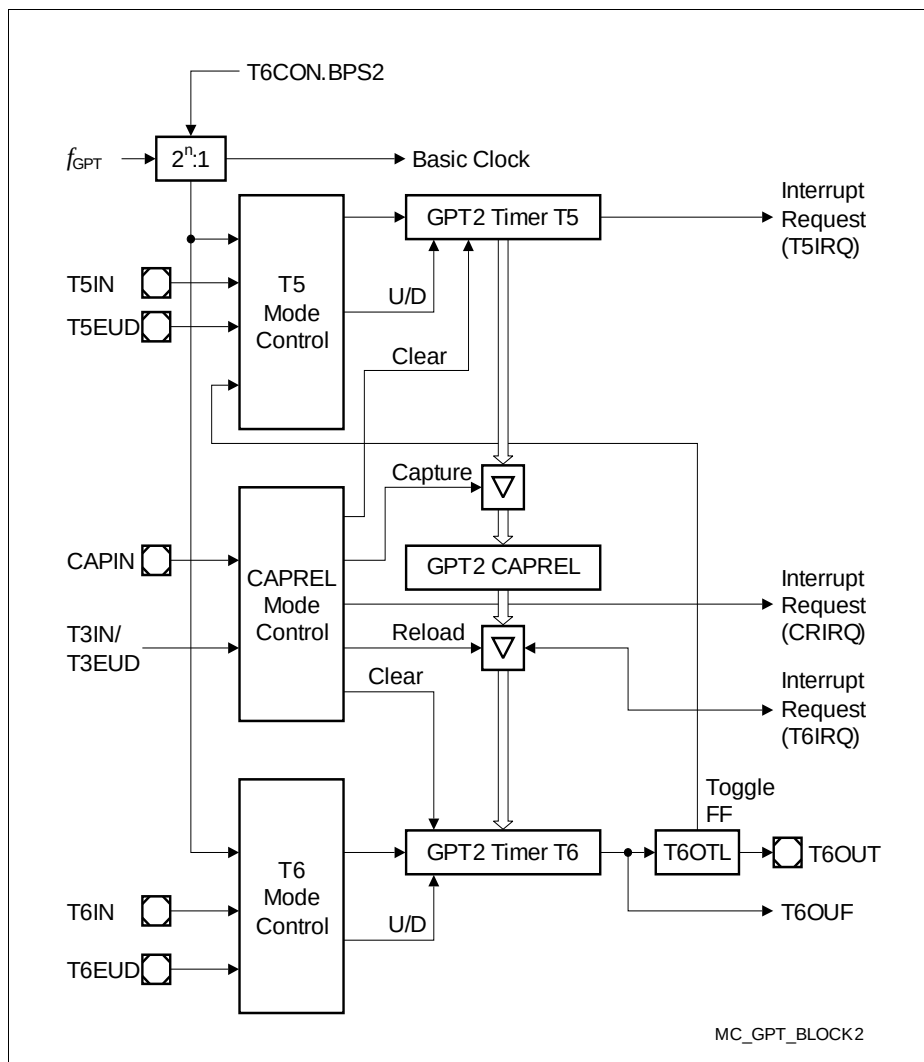


Figure 9 Block Diagram of GPT2

Functional Description

3.14 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality which are able to exchange Data and Remote Frames using a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

Note: The number of CAN nodes and message objects depends on the selected device type.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to its own message object list and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

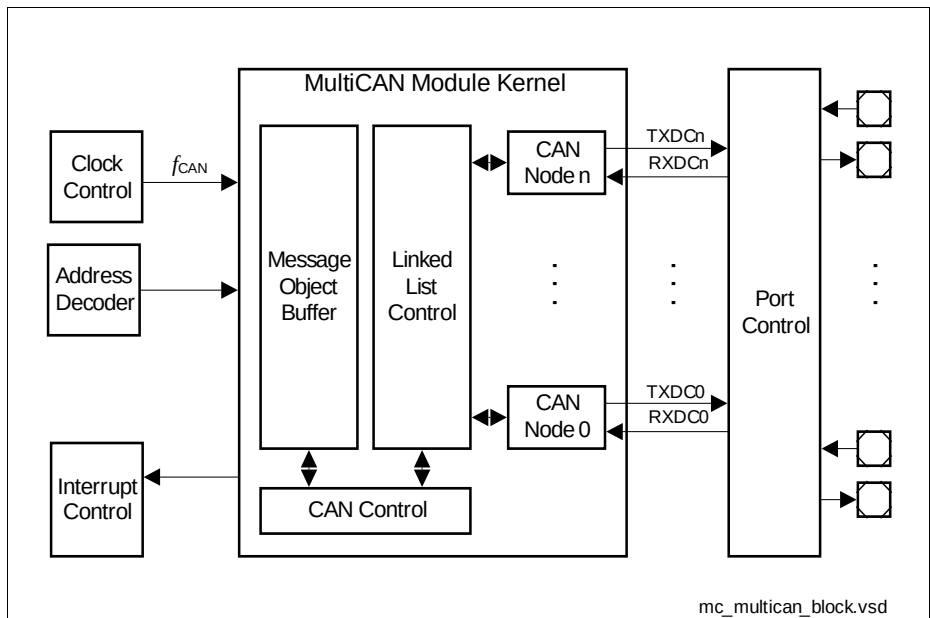


Figure 12 Block Diagram of MultiCAN Module

Electrical Parameters

4.3.2 DC Parameters for Lower Voltage Area

Keeping signal levels within the limits specified in this table ensures operation without overload conditions. For signal levels outside these specifications, also refer to the specification of the overload current I_{OV} .

Note: Operating Conditions apply.

Table 17 is valid under the following conditions: $V_{DDP} \geq 3.0 \text{ V}$; $V_{DDP} \text{ typ. } 3.3 \text{ V}$; $V_{DDP} \leq 4.5 \text{ V}$

Table 17 DC Characteristics for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Pin capacitance (digital inputs/outputs). To be doubled for double bond pins. ¹⁾	$C_{IO} \text{ CC}$	–	–	10	pF	not subject to production test
Input Hysteresis ²⁾	$HYS \text{ CC}$	$0.07 \times V_{DDP}$	–	–	V	$R_S = 0 \text{ Ohm}$
Absolute input leakage current on pins of analog ports ³⁾	$ I_{OZ1} \text{ CC}$	–	10	200	nA	$V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Absolute input leakage current for all other pins. To be doubled for double bond pins. ³⁾¹⁾⁴⁾	$ I_{OZ2} \text{ CC}$	–	0.2	2.5	μA	$T_J \leq 110 \text{ }^\circ\text{C}$; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
		–	0.2	8	μA	$T_J \leq 150 \text{ }^\circ\text{C}$; $V_{IN} > V_{SS}$; $V_{IN} < V_{DDP}$
Pull Level Force Current ⁵⁾	$ I_{PLF} \text{ SR}$	150	–	–	μA	$V_{IN} \geq V_{IHmin}(\text{pull down})$; $V_{IN} \leq V_{ILmax}(\text{pull up})$
Pull Level Keep Current ⁶⁾	$ I_{PLK} \text{ SR}$	–	–	10	μA	$V_{IN} \geq V_{IHmin}(\text{pull up})$; $V_{IN} \leq V_{ILmax}(\text{pull down})$
Input high voltage (all except XTAL1)	$V_{IH} \text{ SR}$	$0.7 \times V_{DDP}$	–	$V_{DDP} + 0.3$	V	
Input low voltage (all except XTAL1)	$V_{IL} \text{ SR}$	-0.3	–	$0.3 \times V_{DDP}$	V	

4.4 Analog/Digital Converter Parameters

These parameters describe the conditions for optimum ADC performance.

Note: Operating Conditions apply.

Table 20 ADC Parameters

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Switched capacitance at an analog input	C_{AINSW} CC	–	–	4	pF	not subject to production test ¹⁾
Total capacitance at an analog input	C_{AINT} CC	–	–	10	pF	not subject to production test ¹⁾
Switched capacitance at the reference input	C_{AREFSW} CC	–	–	7	pF	not subject to production test ¹⁾
Total capacitance at the reference input	C_{AREFT} CC	–	–	15	pF	not subject to production test ¹⁾
Differential Non-Linearity Error	$ EA_{DNL} $ CC	–	0.8	1	LSB	
Gain Error	$ EA_{GAIN} $ CC	–	0.4	0.8	LSB	
Integral Non-Linearity	$ EA_{INL} $ CC	–	0.8	1.2	LSB	
Offset Error	$ EA_{OFF} $ CC	–	0.5	0.8	LSB	
Analog clock frequency	f_{ADCI} SR	0.5	–	16.5	MHz	voltage_range=lower
		0.5	–	20	MHz	voltage_range=upper
Input resistance of the selected analog channel	R_{AIN} CC	–	–	2	kOhm	not subject to production test ¹⁾
Input resistance of the reference input	R_{AREF} CC	–	–	2	kOhm	not subject to production test ¹⁾

Electrical Parameters

Sample time and conversion time of the XC226xN's A/D converters are programmable. The timing above can be calculated using [Table 21](#).

The limit values for f_{ADCI} must not be exceeded when selecting the prescaler value.

Table 21 A/D Converter Computation Table

GLOBCTR.5-0 (DIVA)	A/D Converter Analog Clock f_{ADCI}	INPCRx.7-0 (STC)	Sample Time¹⁾ t_s
000000 _B	f_{SYS}	00 _H	$t_{\text{ADCI}} \times 2$
000001 _B	$f_{\text{SYS}} / 2$	01 _H	$t_{\text{ADCI}} \times 3$
000010 _B	$f_{\text{SYS}} / 3$	02 _H	$t_{\text{ADCI}} \times 4$
:	$f_{\text{SYS}} / (\text{DIVA}+1)$	:	$t_{\text{ADCI}} \times (\text{STC}+2)$
111110 _B	$f_{\text{SYS}} / 63$	FE _H	$t_{\text{ADCI}} \times 256$
111111 _B	$f_{\text{SYS}} / 64$	FF _H	$t_{\text{ADCI}} \times 257$

1) The selected sample time is doubled if broken wire detection is active (due to the presampling phase).

Converter Timing Example A:

Assumptions: $f_{\text{SYS}} = 80 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 12.5 \text{ ns}$), DIVA = 03_H, STC = 00_H

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 4 = 20 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 50 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 2 = 100 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 13 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 13 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.675 \text{ } \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 11 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 11 \times 50 \text{ ns} + 2 \times 12.5 \text{ ns} = 0.575 \text{ } \mu\text{s}$$

Converter Timing Example B:

Assumptions: $f_{\text{SYS}} = 40 \text{ MHz}$ (i.e. $t_{\text{SYS}} = 25 \text{ ns}$), DIVA = 02_H, STC = 03_H

Analog clock $f_{\text{ADCI}} = f_{\text{SYS}} / 3 = 13.3 \text{ MHz}$, i.e. $t_{\text{ADCI}} = 75 \text{ ns}$

Sample time $t_s = t_{\text{ADCI}} \times 5 = 375 \text{ ns}$

Conversion 10-bit:

$$t_{\text{C10}} = 16 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 16 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.25 \text{ } \mu\text{s}$$

Conversion 8-bit:

$$t_{\text{C8}} = 14 \times t_{\text{ADCI}} + 2 \times t_{\text{SYS}} = 14 \times 75 \text{ ns} + 2 \times 25 \text{ ns} = 1.10 \text{ } \mu\text{s}$$

Electrical Parameters

Table 25 Flash Parameters (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Number of erase cycles	N_{ER} SR	—	—	15.000	cycles	$t_{RET} \geq 5$ years; Valid for up to 64 user selected sectors (data storage)
		—	—	1.000	cycles	$t_{RET} \geq 20$ years

- 1) The unused Flash module(s) can be erased/programmed while code is executed and/or data is read from only one Flash module or from PSRAM. The Flash module that delivers code/data can, of course, not be erased/programmed.
- 2) Flash module 1 can be erased/programmed while code is executed and/or data is read from Flash module 0.
- 3) Value of IMB_IMBCTRL.WSFLASH.
- 4) Programming and erase times depend on the internal Flash clock source. The control state machine needs a few system clock cycles. This increases the stated durations noticeably only at extremely low system clock frequencies.

Access to the XC226xN Flash modules is controlled by the IMB. Built-in prefetch mechanisms optimize the performance for sequential access.

Flash access waitstates only affect non-sequential access. Due to prefetch mechanisms, the performance for sequential access (depending on the software structure) is only partially influenced by waitstates.

Electrical Parameters

Table 28 **Standard Pad Parameters for Upper Voltage Range** (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Rise and Fall times (10% - 90%)	t_{RF} CC	—	—	23 + 0.6 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Medium
		—	—	11.6 + 0.22 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Medium
		—	—	4.2 + 0.14 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Sharp
		—	—	20.6 + 0.22 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Strong ; Driver_Edge= Slow
		—	—	212 + 1.9 x C_L	ns	$C_L \geq 20$ pF; $C_L \leq 100$ pF; Driver_Strength = Weak

1) An output current above $|I_{Oxnom}|$ may be drawn from up to three pins at the same time. For any group of 16 neighboring output pins, the total output current in each direction (ΣI_{OL} and $\Sigma -I_{OH}$) must remain below 50 mA.

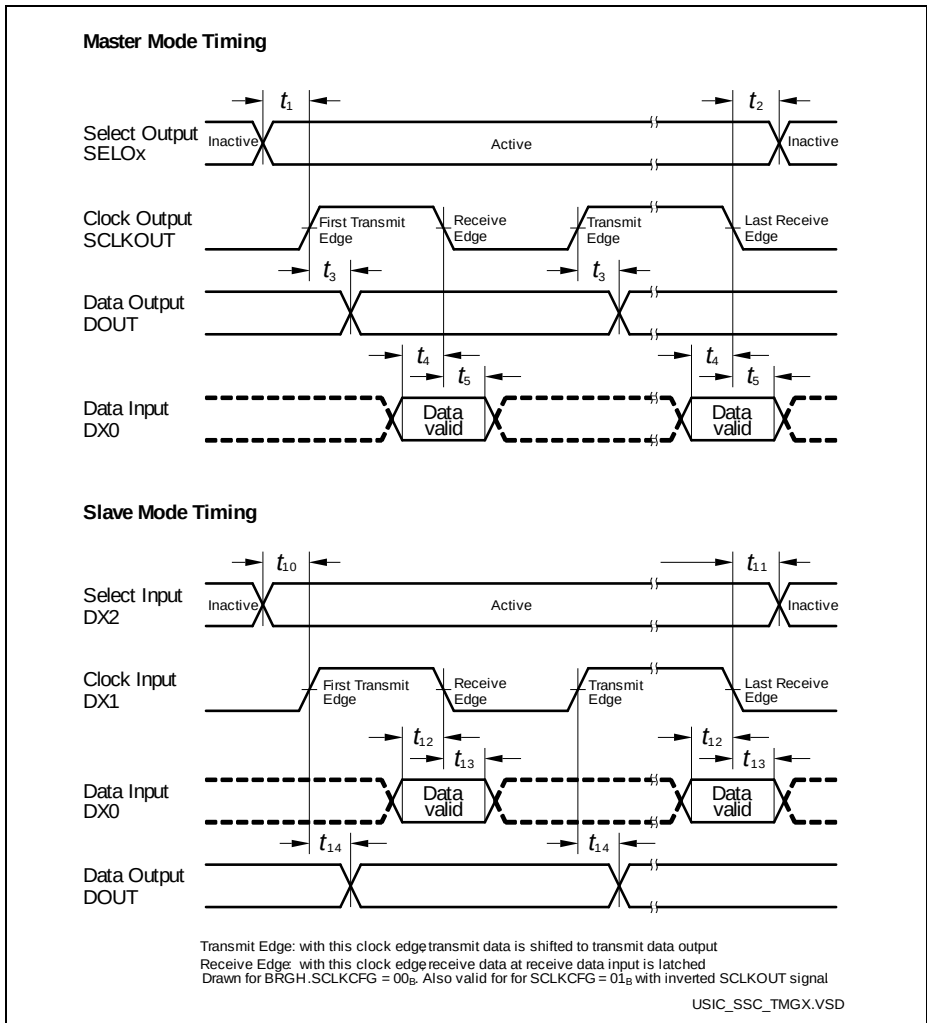


Figure 26 USIC - SSC Master/Slave Mode Timing

Note: This timing diagram shows a standard configuration where the slave select signal is low-active and the serial clock signal is not shifted and not inverted.

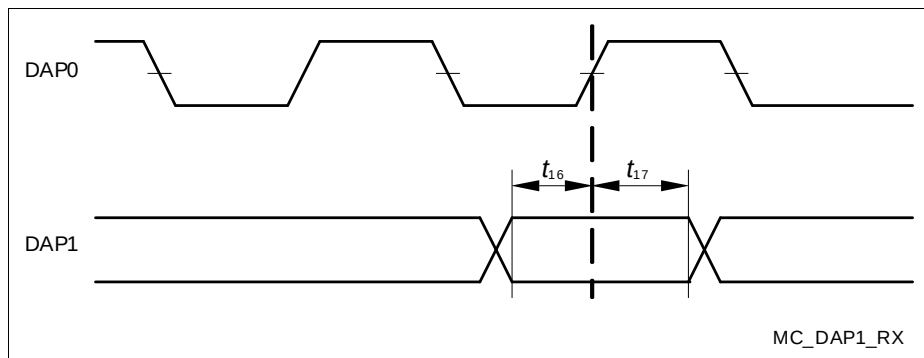


Figure 28 DAP Timing Host to Device

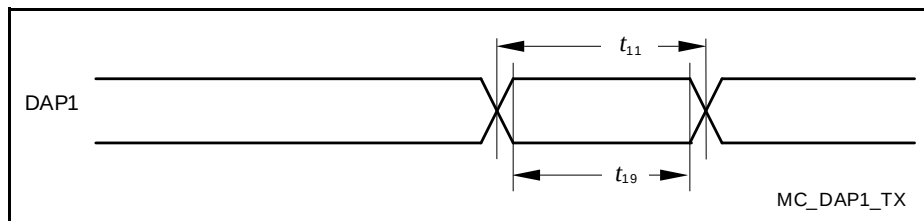


Figure 29 DAP Timing Device to Host

Note: The transmission timing is determined by the receiving debugger by evaluating the sync-request synchronization pattern telegram.

Debug via JTAG

The following parameters are applicable for communication through the JTAG debug interface. The JTAG module is fully compliant with IEEE1149.1-2000.

Note: These parameters are not subject to production test but verified by design and/or characterization.

Note: Operating Conditions apply.

Table 40 is valid under the following conditions: $C_L = 20$ pF; voltage_range= upper

Table 40 JTAG Interface Timing for Upper Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	—	—	ns	1)
TCK high time	t_2 SR	16	—	—	ns	

Electrical Parameters

Table 40 JTAG Interface Timing for Upper Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK low time	t_3 SR	16	—	—	ns	
TCK clock rise time	t_4 SR	—	—	8	ns	
TCK clock fall time	t_5 SR	—	—	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	—	—	ns	
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	
TDO valid from TCK falling edge (propagation delay) ²⁾	t_8 CC	—	25	29	ns	
TDO high impedance to valid output from TCK falling edge ³⁾²⁾	t_9 CC	—	25	29	ns	
TDO valid output to high impedance from TCK falling edge ²⁾	t_{10} CC	—	25	29	ns	
TDO hold after TCK falling edge ²⁾	t_{18} CC	5	—	—	ns	

1) Under typical conditions, the JTAG interface can operate at transfer rates up to 20 MHz.

2) The falling edge on TCK is used to generate the TDO timing.

3) The setup time for TDO is given implicitly by the TCK cycle time.

Table 41 is valid under the following conditions: $C_L = 20$ pF; voltage_range= lower

Table 41 JTAG Interface Timing for Lower Voltage Range

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TCK clock period	t_1 SR	50	—	—	ns	
TCK high time	t_2 SR	16	—	—	ns	
TCK low time	t_3 SR	16	—	—	ns	
TCK clock rise time	t_4 SR	—	—	8	ns	
TCK clock fall time	t_5 SR	—	—	8	ns	
TDI/TMS setup to TCK rising edge	t_6 SR	6	—	—	ns	

Electrical Parameters

Table 41 JTAG Interface Timing for Lower Voltage Range (cont'd)

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
TDI/TMS hold after TCK rising edge	t_7 SR	6	—	—	ns	
TDO valid from TCK falling edge (propagation delay) ¹⁾	t_8 CC	—	32	36	ns	
TDO high impedance to valid output from TCK falling edge ²⁾¹⁾	t_9 CC	—	32	36	ns	
TDO valid output to high impedance from TCK falling edge ¹⁾	t_{10} CC	—	32	36	ns	
TDO hold after TCK falling edge ¹⁾	t_{18} CC	5	—	—	ns	

1) The falling edge on TCK is used to generate the TDO timing.

2) The setup time for TDO is given implicitly by the TCK cycle time.

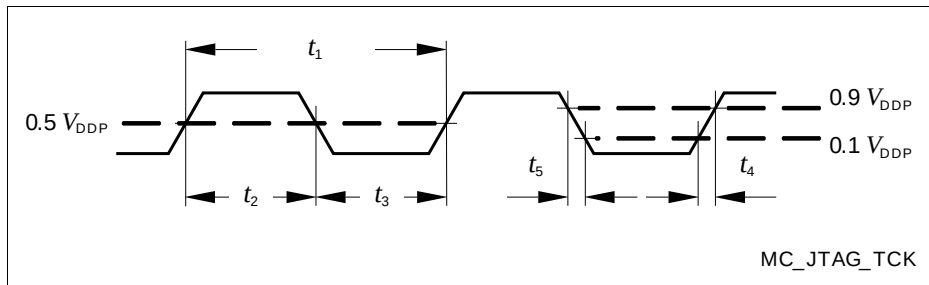


Figure 30 Test Clock Timing (TCK)

Package Outlines

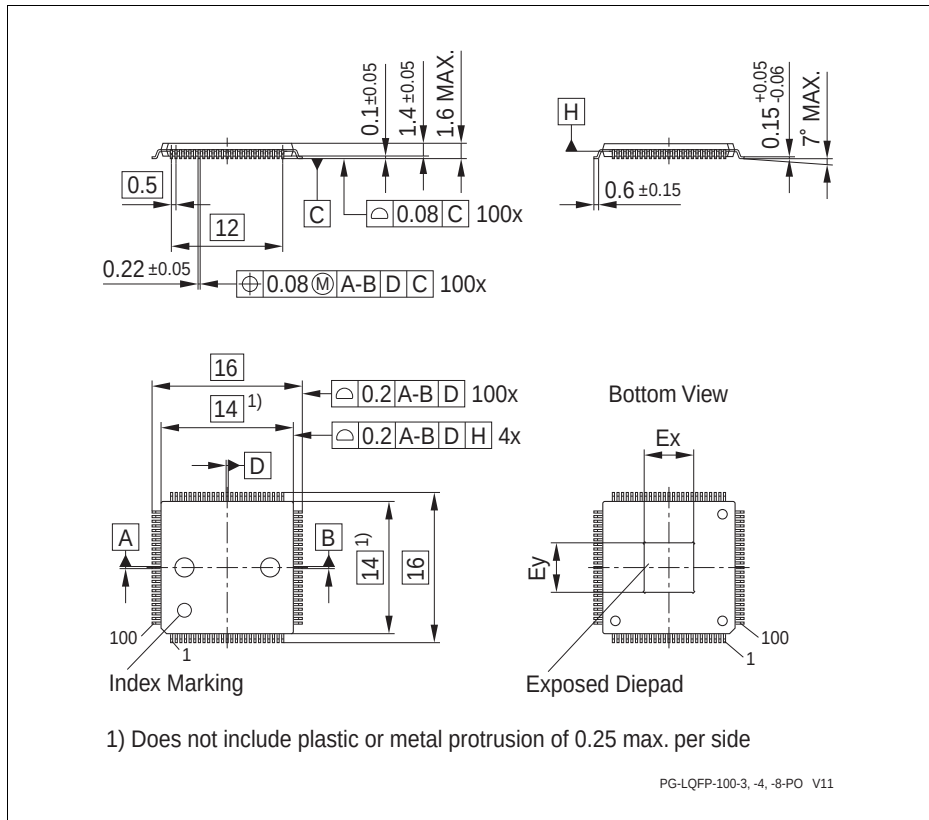


Figure 32 PG-LQFP-100-8 (Plastic Green Thin Quad Flat Package)

All dimensions in mm.

You can find complete information about Infineon packages, packing and marking in our Infineon Internet Page "Packages": <http://www.infineon.com/packages>